

PESD5V0X1BT-Q

Ultra low capacitance bidirectional ESD protection diode 29 August 2022 Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a small SOT23 Surface-Mounted Device (SMD) plastic package, designed to protect one signal line from the damage caused by ESD and other transients.

The device may also be used for unidirectional ESD protection of up to two signal lines.

2. Features and benefits

- Bidirectional ESD protection of one line
- Unidirectional ESD protection of up to two lines
- Ultra low diode capacitance: C_d = 0.9 pF
- Very low leakage current: I_{RM} = 1 nA
- · ESD protection up to 9 kV
- IEC 61000-4-2; level 4 (ESD)
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- USB interfaces
- Antenna protection
- · Radio Frequency (RF) protection
- 10/100/1000 Mbit/s Ethernet
- FireWire
- Asymmetric Digital Subscriber Line (ADSL)
- · High-speed data lines
- Subscriber Identity Module (SIM) card protection
- · Computers, peripherals and printers
- · Cellular handsets and accessories
- Portable electronics
- Communication systems
- · Audio and video equipment

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	5	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[1]	-	0.9	1.3	pF
			[2]	-	2	2.6	pF

- [1] Bidirectional configuration: measured from pin 1 to 2 or pin 2 to 1.
- [2] Unidirectional configuration: measured from pin 1 to 3 or pin 2 to 3.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	3	3
2	K2	cathode (diode 2)		
3	CA	common anode	1 2 SOT23	1 2 006aaa 154

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0X1BT-Q	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD5V0X1BT-Q	U3%

[1] % = placeholder for manufacturing site code

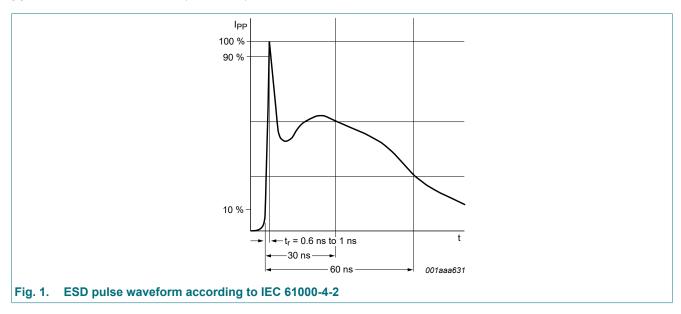
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximum	ratings		'			
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge; T _{amb} = 25 °C	[1]	-	9	kV
		MIL-STD-883; human body model (HBM); T _{amb} = 25 °C		-	10	kV

[1] Device stressed with ten non-repetitve ESD pulses.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	5	V
V_{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		5.8	7.5	9.5	V
I _{RM}	reverse leakage current	V _{RWM} = 5 V; T _{amb} = 25 °C		-	1	100	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[1]	-	0.9	1.3	pF
			[2]	-	2	2.6	pF
		f = 1 MHz; V _R = 5 V; T _{amb} = 25 °C	[1]	-	0.8	1.2	pF
			[2]	-	1.7	2.3	pF
R _{diff}	differential resistance	I _R = 1 mA; T _{amb} = 25 °C		-	-	100	Ω

- [1] Bidirectional configuration: measured from pin 1 to 2 or pin 2 to 1.
- [2] Unidirectional configuration: measured from pin 1 to 3 or pin 2 to 3.

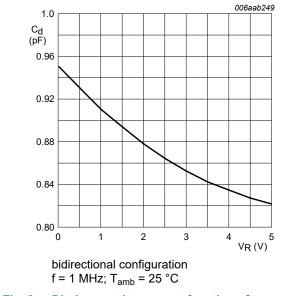


Fig. 2. Diode capacitance as a function of reverse voltage; typical values

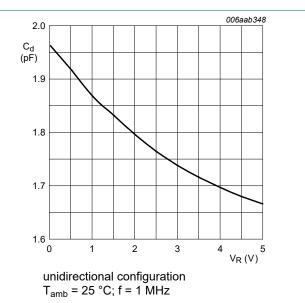
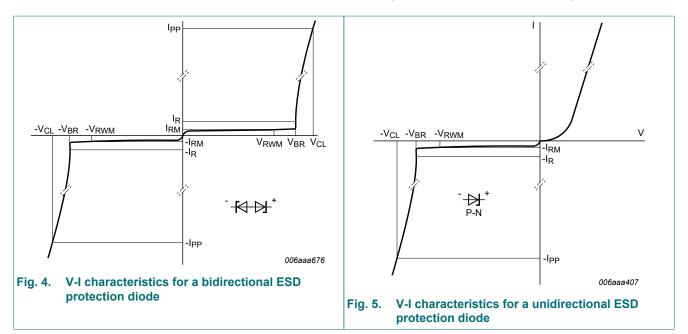
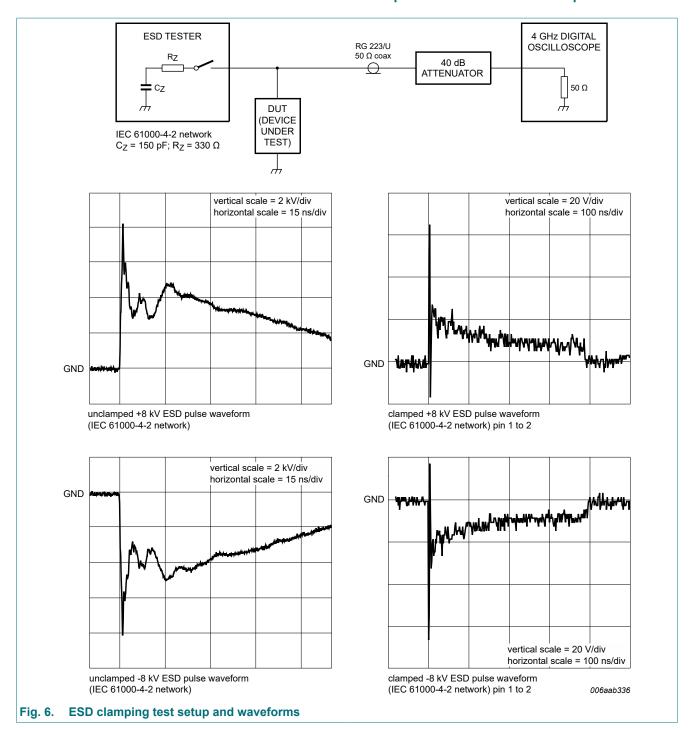


Fig. 3. Diode capacitance as a function of reverse voltage; typical values

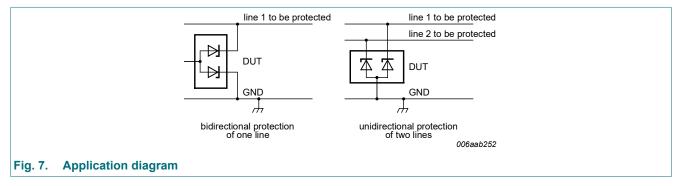




10. Application information

The device is designed for the protection of one bidirectional data or signal line from the damage caused by ESD. The device may be used on lines where the signal polarities are both, positive and negative with respect to ground.

The device may also be used for the protection of two unidirectional data or signal lines, which have positive signal polarities with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. The path length between the device and the protected line should be minimized.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

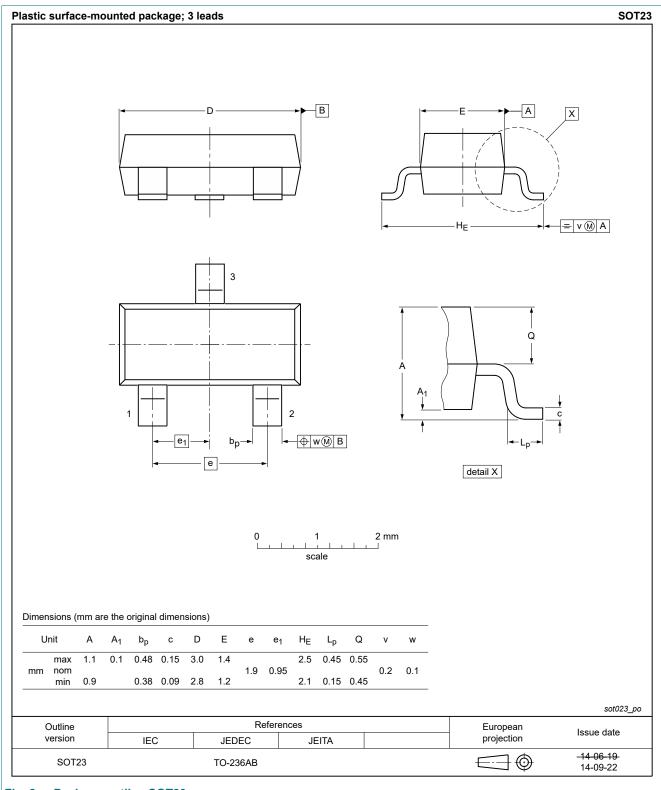
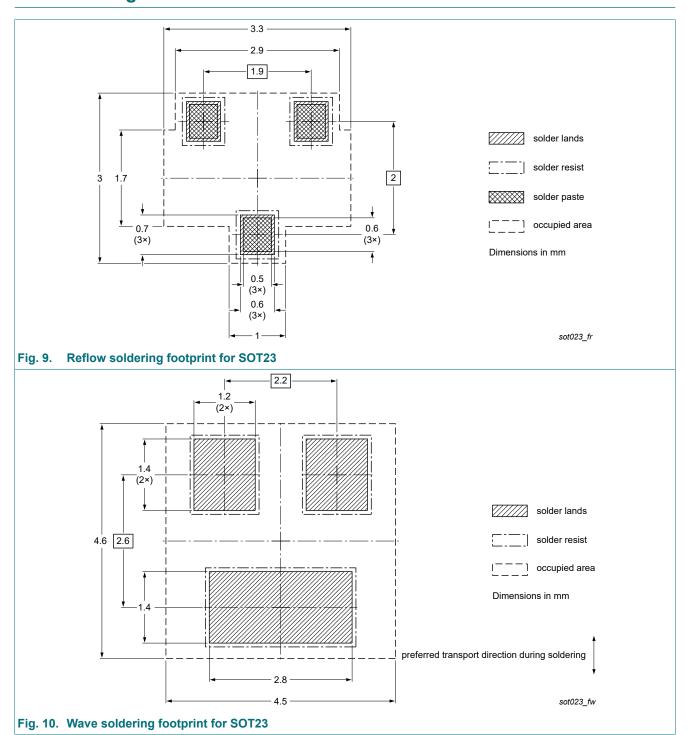


Fig. 8. Package outline SOT23

13. Soldering



14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0X1BT-Q v.1	20220829	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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