74ABT657

Octal transceiver with parity generator/checker; 3-state

Rev. 03 — 15 March 2010

Product data sheet

1. General description

The 74ABT657 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 64 mA. The Transmit/Receive input (pin T/\overline{R}) determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

When Output Enable input (pin \overline{OE}) is HIGH, both A and B ports are high-impedance. The parity select input (pin ODD/ \overline{EVEN}) allows the user to generate either an odd or even parity output, depending on the system. Pin PARITY is an output from the generator/checker when transmitting from port A to port B (pin $T/\overline{R} = HIGH$) and an input when receiving from port B to port A port (pin $T/\overline{R} = LOW$).

In transmit mode (pin $T/\overline{R} = HIGH$) port A is polled to determine the number of HIGH inputs on port A. Pin PARITY output goes to the logic state determined by the setting of pin ODD/ \overline{EVEN} and by the number of HIGH inputs on port A. For example, if pin ODD/ \overline{EVEN} is set LOW (even parity) and the number of HIGH inputs on port A is odd, pin PARITY output goes HIGH, transmitting even parity. If the number of HIGH inputs on port A is even, pin PARITY output goes LOW, keeping even parity.

In receive mode (pin $T/\overline{R} = LOW$) port B is polled to determine the number of HIGH inputs on port B. If pin ODD/ \overline{EVEN} is LOW (even parity) and the number of HIGH inputs on port B is:

- Odd and pin PARITY input is HIGH, pin ERROR is HIGH, indicating no error
- Even and pin PARITY input is HIGH, pin ERROR goes LOW, indicating an error

2. Features and benefits

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64 mA and -32 mA
- Power-up 3-state
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V



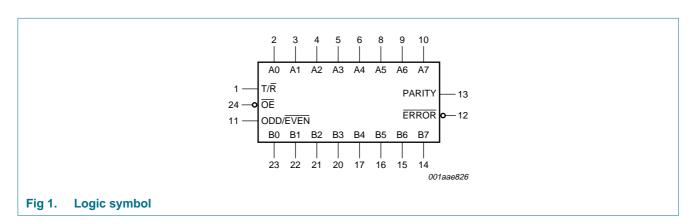
Octal transceiver with parity generator/checker; 3-state

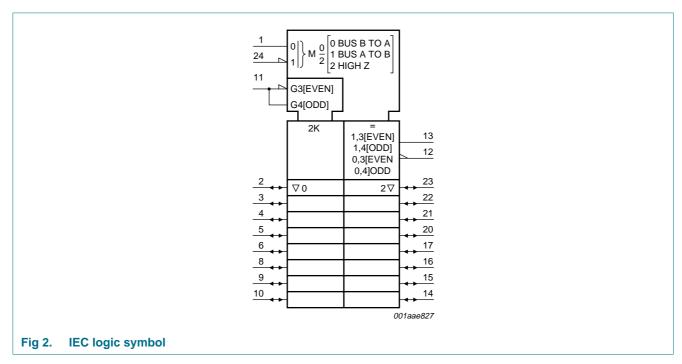
3. Ordering information

Table 1. Ordering information

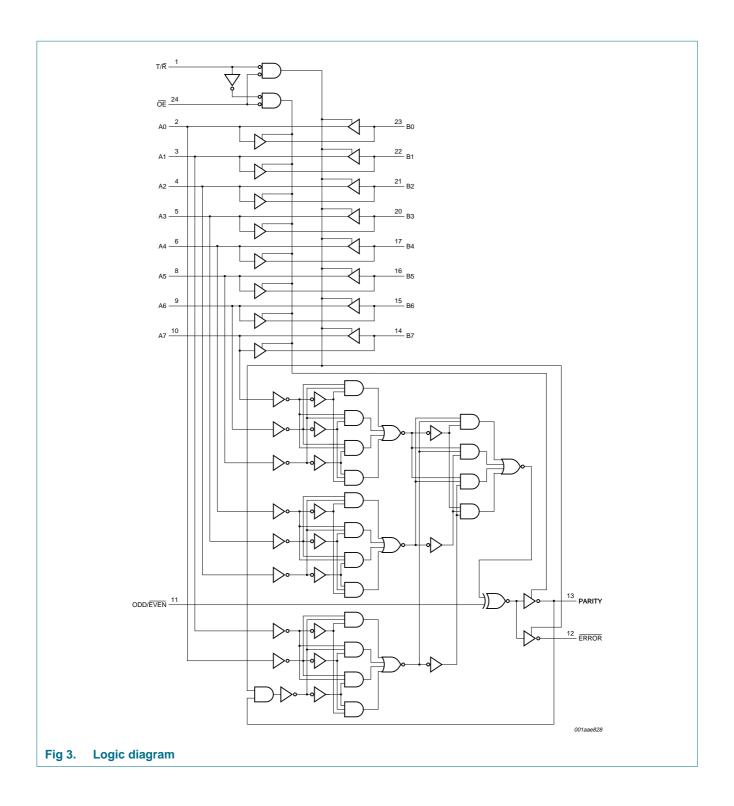
Type number	Package	Package										
	Temperature range	Name	Description	Version								
74ABT657D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1								
74ABT657DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1								
74ABT657PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1								

4. Functional diagram





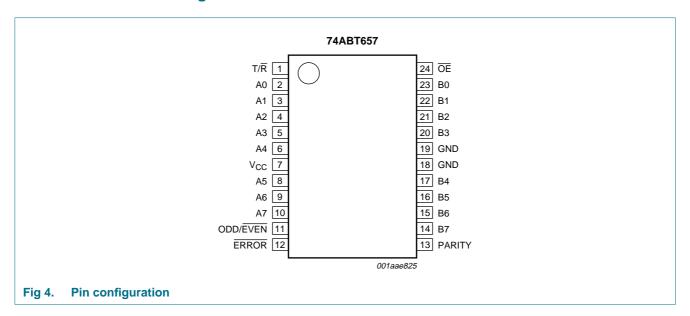
Octal transceiver with parity generator/checker; 3-state



Octal transceiver with parity generator/checker; 3-state

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
T/R	1	transmit/receive input
A0 to A7	2, 3, 4, 5, 6, 8, 9, 10	A port input/3-state output
V _{CC}	7	positive supply voltage
ODD/EVEN	11	parity select input
ERROR	12	error output in receive mode
PARITY	13	parity output in transmit mode/input in receive mode
B0 to B7	23, 22, 21, 20, 17, 16, 15, 14	B port input/3-state output
GND	18, 19	ground (0 V)
ŌE	24	output enable input (active LOW)

Octal transceiver with parity generator/checker; 3-state

6. Functional description

6.1 Function selection

Table 3. Function selection[1]

Number of	Inputs			Data I/O	Data I/O Output		
inputs HIGH	OE	T/R	ODD/EVEN	PARITY	ERROR	Mode	
0, 2, 4, 6 and 8	L	Н	Н	Н	Z	transmit	
(even)	L	Н	L	L	Z	transmit	
	L	L	Н	Н	Н	receive	
	L	L	Н	L	L	receive	
	L	L	L	Н	L	receive	
	L	L	L	L	Н	receive	
1, 3, 5 and 7	L	Н	Н	L	Z	transmit	
(odd)	L	Н	L	Н	Z	transmit	
	L	L	Н	Н	L	receive	
	L	L	Н	L	Н	receive	
	L	L	L	Н	Н	receive	
	L	L	L	L	L	receive	
Don't care	Н	X	Χ	Z	Z	3-state	

^[1] H = HIGH voltage level;

L = LOW voltage level;

X = don't care;

Z = high-impedance OFF-state.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		<u>[1]</u> –1.2	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	<u>[1]</u> –0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V	-18	-	mA
I_{OK}	output clamping current	V _O < 0 V	-50	-	mA
Io	output current	output in LOW-state	-	128	mA
Tj	junction temperature		[2] _	150	°C
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{I}	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

Octal transceiver with parity generator/checker; 3-state

9. Static characteristics

Table 6. Static characteristics

Table 6.	Static characteristics	1							
Symbol	Parameter	Conditions			25 °C		-40 °C t	o +85 °C	Unit
				Min	Тур	Max	Min	Max	
V_{IK}	input clamping voltage	$V_{CC} = 4.5 \text{ V}; I_{IK} = -18 \text{ mA}$		-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output	$V_I = V_{IL}$ or V_{IH}							
	voltage	$V_{CC} = 4.5 \text{ V}; I_{OH} = -3 \text{ mA}$		2.5	3.5	-	2.5	-	V
		$V_{CC} = 5.0 \text{ V}; I_{OH} = -3 \text{ mA}$		3.0	4.0	-	3.0	-	V
		$V_{CC} = 4.5 \text{ V}; I_{OH} = -32 \text{ mA}$		2.0	2.6	-	2.0	-	V
V _{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_{I} = V_{IL} or V_{IH}		-	0.42	0.55	-	0.55	V
l _l	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V							
		control pins		-	±0.01	±1.0	-	±1.0	μΑ
		data pins		-	±5	±100	-	±100	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; \text{ V}_{I} \text{ or } \text{V}_{O} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μΑ
I _{O(pu/pd)}	power-up/power-down output current	$V_{CC} = 2.0 \text{ V}; V_O = 0.5 \text{ V};$ $V_I = \text{GND or } V_{CC}; \overline{\text{OE}} \text{ HIGH}$	<u>[1]</u>	-	±5.0	±50	-	±50	μΑ
l _{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
		$V_0 = 2.7 \text{ V}$		-	5.0	50	-	50	μΑ
		V _O = 0.5 V		-	-5.0	-50	-	-50	μΑ
I_{LO}	output leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$		-	5.0	50	-	50	μΑ
lo	output current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	[2]	-180	-100	-50	-180	-50	mΑ
I _{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	0.5	250	-	250	μΑ
		outputs LOW-state		-	20	30	-	30	mΑ
		outputs disabled		-	0.5	250	-	250	μΑ
Δl _{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[3]						
		outputs enabled		-	0.5	1.5	-	1.5	mΑ
		outputs 3-state, one data input		-	50	250	-	250	μΑ
		outputs 3-state; one enable input		-	0.5	1.5	-	1.5	mΑ
Cı	input capacitance	$V_I = 0 \text{ V or } V_{CC}$		-	4	-	-	-	pF
C _{I/O}	input/output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$		-	7	-	-	-	pF

^[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For V_{CC} = 2.1 V to V_{CC} = 5 V \pm 10 %, a transition time of up to 100 μ s is permitted.

^[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

^[3] This is the increase in supply current for each input at 3.4 V.

Octal transceiver with parity generator/checker; 3-state

10. Dynamic characteristics

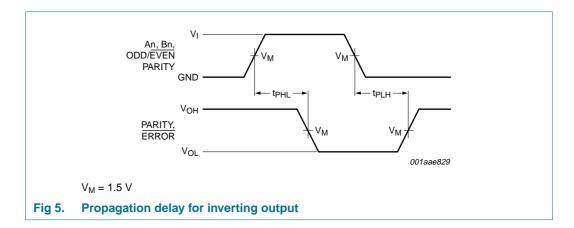
Table 7. Dynamic characteristics *GND = 0 V; for test circuit, see Figure 9.*

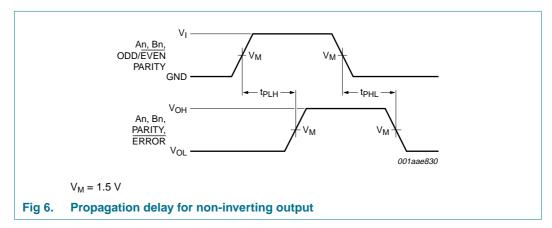
Symbol	Parameter	Conditions		25 °C;	V _{CC} =	5.0 V	-40 °C to V _{CC} = 5.0		Unit
				Min	Тур	Max	Min	Max	
t_{PLH}	LOW to HIGH	An to Bn or Bn to An; see Figure 6		1.1	2.5	4.1	1.1	4.6	ns
	propagation delay	An to PARITY; see Figure 5 and 6		2.5	5.1	6.7	2.5	8.1	ns
		ODD/ $\overline{\text{EVEN}}$ to PARITY and $\overline{\text{ERROR}}$; see $\underline{\text{Figure 5}}$ and $\underline{\text{6}}$		1.7	3.5	4.6	1.7	5.3	ns
		Bn to ERROR; see Figure 5 and 6		3.9	7.3	10.2	3.9	12.3	ns
		PARITY to ERROR; see Figure 5 and 6		2.7	4.5	5.9	2.7	7.7	ns
t _{PHL}	HIGH to LOW	An to Bn or Bn to An; see Figure 6		1.2	3.0	3.9	1.2	4.3	ns
	propagation delay	An to PARITY; see Figure 5 and 6		2.8	5.0	7.4	2.8	8.9	ns
		ODD/EVEN to PARITY and ERROR; see Figure 5 and 6		1.9	3.7	5.1	1.9	5.8	ns
		Bn to ERROR; see Figure 5 and 6		4.0	7.9	10.5	4.0	12.9	ns
		PARITY to ERROR; see Figure 5 and 6		3.2	5.2	6.7	3.2	8.1	ns
t _{PZH}	OFF-state to HIGH propagation delay	see Figure 7 and 8	<u>[1]</u>	1.3	3.6	5.5	1.3	6.5	ns
t _{PZL}	OFF-state to LOW propagation delay	see Figure 7 and 8	<u>[1]</u>	1.9	4.2	5.3	1.9	6.5	ns
t _{PHZ}	HIGH to OFF-state propagation delay	see Figure 7 and 8		2.4	3.6	5.6	2.4	6.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	see Figure 7 and 8		2.2	3.4	7.3	2.2	7.8	ns

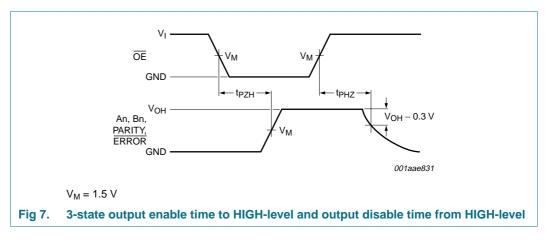
^[1] These delay times reflect the 3-state recovery time only and do not include the delay through the buffers and the parity check circuitry which affect the ERROR output. To ensure **valid** information at the ERROR pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the ERROR output. **Valid** data at the ERROR pin ≥ (B to A) + (A to PARITY).

Octal transceiver with parity generator/checker; 3-state

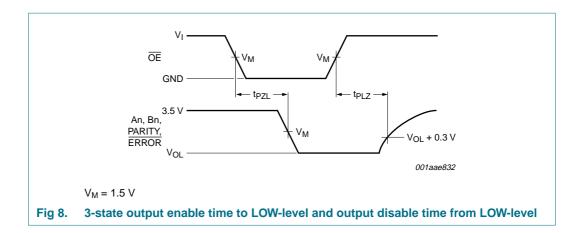
11. Waveforms



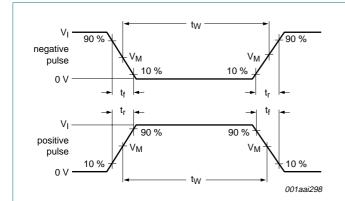


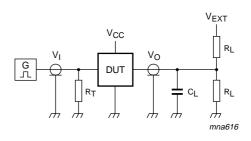


Octal transceiver with parity generator/checker; 3-state



b. Test circuit





a. Input pulse definition

Test data and V_{EXT} levels are given in Table 8.

 R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

 V_{EXT} = Test voltage for switching times.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

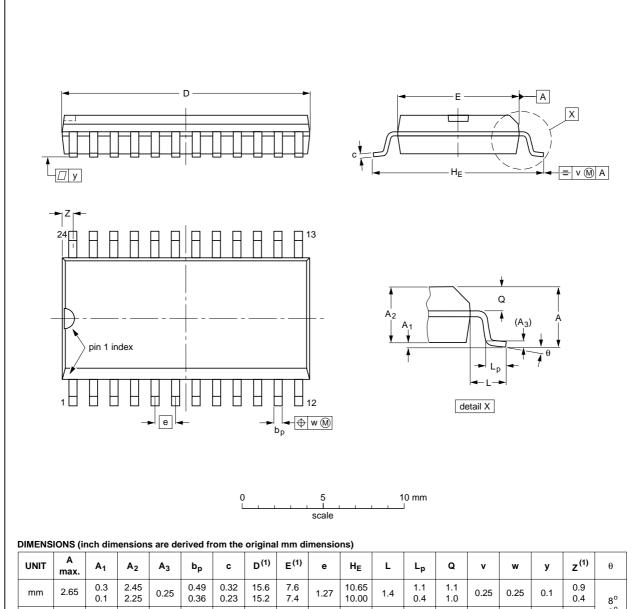
Input				Load		V _{EXT}			
VI	f _l	t _W	t _r , t _f	CL	R_L	t _{PHL} , t _{PLH}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}	
3.0 V	1 MHz	500 ns	\leq 2.5 ns	50 pF	$500~\Omega$	open	open	7.0 V	

Octal transceiver with parity generator/checker; 3-state

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT137-1	075E05	MS-013				99-12-27 03-02-19

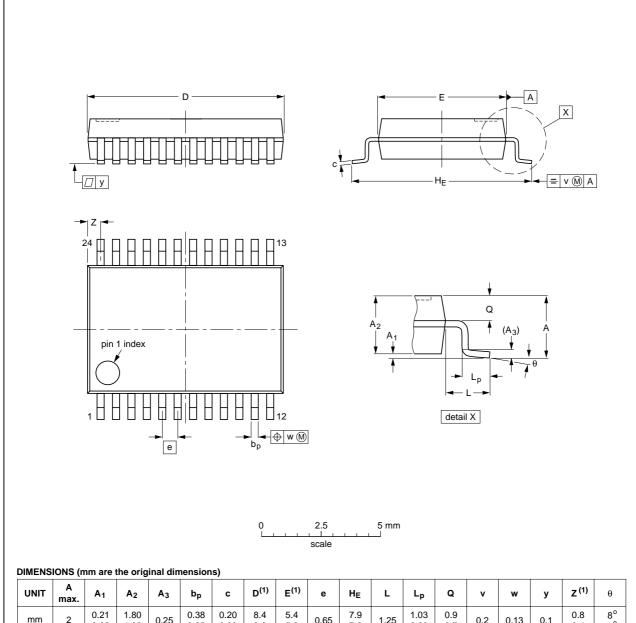
Fig 10. Package outline SOT137-1 (SO24)

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Octal transceiver with parity generator/checker; 3-state

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	ø	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT340-1		MO-150				99-12-27 03-02-19

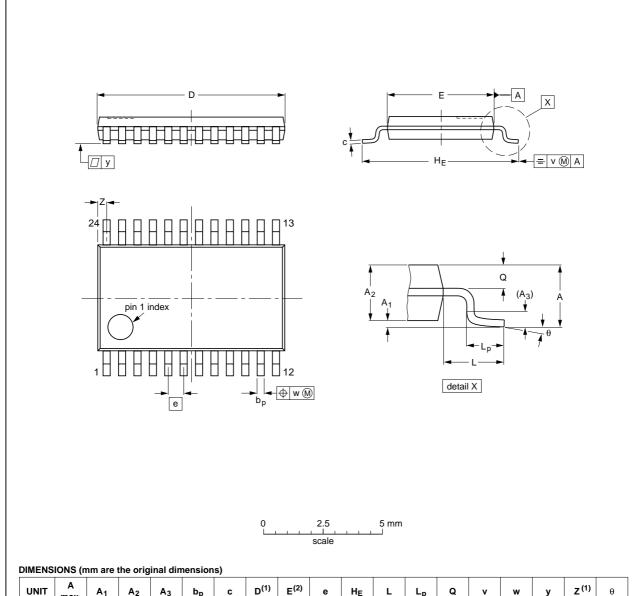
Fig 11. Package outline SOT340-1 (SSOP24)

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Octal transceiver with parity generator/checker; 3-state

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

VERSION IEC JEDEC JEITA PROJECTION ISSUE DATE SOT355-1 MO-153 IIII IIII IIIII IIII IIII IIII IIII I	OUTLINE		REFER	EUROPEAN	ISSUE DATE			
SOT355-1 MO-153 99-12-27 03-02-19	VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
	SOT355-1		MO-153					

Fig 12. Package outline SOT355-1 (TSSOP24)

74ABT657_3

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Octal transceiver with parity generator/checker; 3-state

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT657_3	20100315	Product data sheet	-	74ABT657_2
Modifications:	 The format of to of NXP Semicon 		lesigned to comply with	n the new identity guidelines
	 Legal texts have 	e been adapted to the new	company name where	appropriate.
	 DIP 24 (SOT2) "Package outling" 	22-1) package removed from ne".	Section 3 "Ordering in	nformation" and Section 12
74ABT657_2	20041027	Product specification	-	74ABT657
74ABT657	19951211	Product specification	-	-

Octal transceiver with parity generator/checker; 3-state

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contact information

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