2.5V, 3.3V LVCMOS 1:18 Clock Fanout Buffer
AK8180E

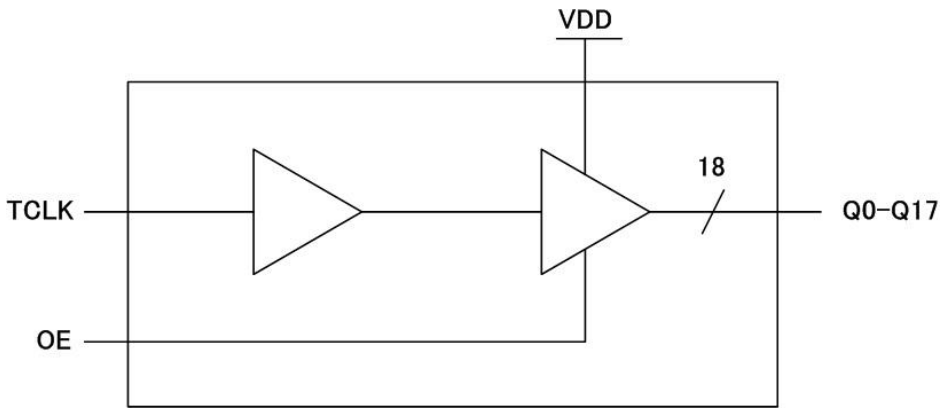
Features

- 18 LVCMOS outputs enable to drive up to 36 clock lines
- LVCMOS/LVTTL input
- 2.5V or 3.3V power supply
- Clock output frequency up to 200MHz
- Output-to-output skew: 85ps (typical)
- Output enable control
- Operating Temperature Range: -40 to +85℃
- Package: 32-pin LQFP (Pb free)
- Pin compatible with CY29942, MPC942C

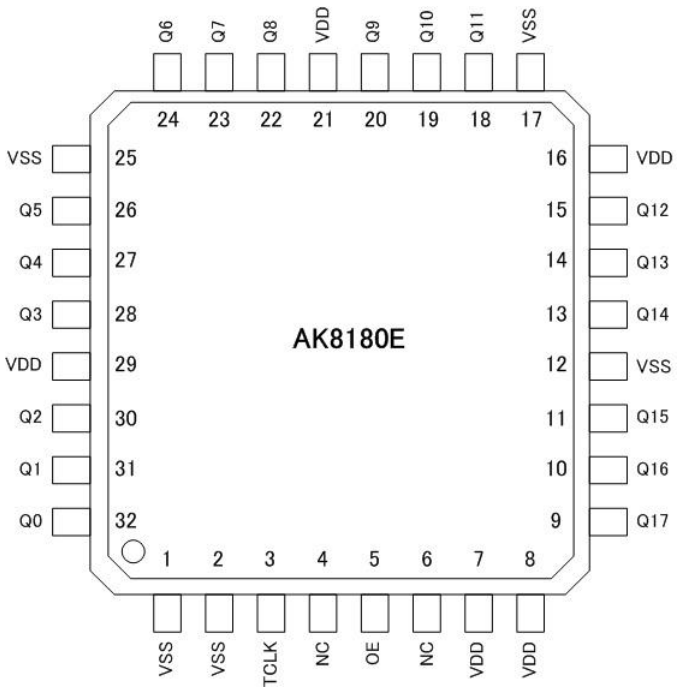
Description

The AK8180E is a member of AKM's LVCMOS clock fanout buffer family designed for telecom, networking and computer applications, requiring a range of clocks with high performance and low skew. The AK8180E distributes 18 buffered clocks up to 200MHz. The 18 outputs can drive terminated 50 Ω clock lines. AK8180E are derived from AKM's long-term-experienced clock device technology, and enable clock output to perform low skew and to operate with very low current consumption. The AK8180E is available in a 7mm x 7mm 32-pin LQFP package.

Block Diagram



Pin Descriptions



Package: 32-Pin LQFP(Top View)

Pin No.	Pin Name	Pin Type	pullup /down	Description
1	VSS	PWR		Ground
2	VSS	PWR		Ground
3	TCLK	IN	PD	Clock Input (LVCMOS/LVTTL)
4	NC	--	PD	It should be connected to VSS or opened
5	OE	IN	PU	Clock Output Enable High (open): clock outputs follow clock input Low: clock outputs become high impedance
6	NC	--	PD	It should be connected to VSS or opened
7	VDD	PWR		Power Supply
8	VDD	PWR		Power Supply
9	Q17	OUT		Clock Output
10	Q16	OUT		Clock Output
11	Q15	OUT		Clock Output
12	VSS	PWR		Ground
13	Q14	OUT		Clock Output
14	Q13	OUT		Clock Output
15	Q12	OUT		Clock Output
16	VDD	PWR		Power Supply

(continue on next page)

Pin No.	Pin Name	Pin Type	Pullup /down	Description
17	VSS	PWR		Ground
18	Q11	OUT		Clock Output
19	Q10	OUT		Clock Output
20	Q9	OUT		Clock Output
21	VDD	PWR		Power Supply
22	Q8	OUT		Clock Output
23	Q7	OUT		Clock Output
24	Q6	OUT		Clock Output
25	VSS	PWR		Ground
26	Q5	OUT		Clock Output
27	Q4	OUT		Clock Output
28	Q3	OUT		Clock Output
29	VDD	PWR		Power Supply
30	Q2	OUT		Clock Output
31	Q1	OUT		Clock Output
32	Q0	OUT		Clock Output

PWR: Power pin, IN: Input pin, OUT: Output pin
PU: Pull up, PD: Pull down

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8180E	AK8180E	Tape and Reel	32-pin LQFP	-40 to 85 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Ground level	VSS	0	V
Input voltage	Vin	VSS-0.5 to VDD+0.5	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-55 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	VDD±5%	2.375	2.5	2.625	V
			3.135	3.3	3.465	

(1) Power of 2.5V or 3.3V requires to be supplied from a single source. A decoupling capacitor of 0.1μF for power supply line should be located close to each VDD pin.

General Specification

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Termination Voltage	VTT			VDD/2		V
Input Capacitance	C_{IN}			4.0		pF
Input Pullup Resistor	R_{PU}			51		kΩ
Input Pulldown Resistor	R_{PD}			51		kΩ

DC Characteristics

VDD = 3.3V±5% or 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input High Voltage	V_{IH}	Pin: TCLK, OE	2.0		VDD+0.3	V
Input Low Voltage	V_{IL}	Pin: TCLK, OE	VSS-0.3		0.8	V
Input Current (1), (2)	I_{IN}	Pin: TCLK, OE	-200		200	μA
Output High Voltage	V_{OH}	I_{OH}= -20mA (2), (3), VDD=3.3V I_{OH}= -16mA (2), (3), VDD=2.5V	2.4 2.0			V
Output Low Voltage	V_{OL}	I_{OL}= +20mA (2), (3)			0.5	V
Quiescent Supply Current	I_{DDQ}	OE=VSS, TCLK=H/L		0.1	7	mA
Dynamic Supply Current	I_{DD}	VDD=3.3V, Outputs at 150MHz C_L=15pF		285		mA
		VDD=3.3V, Outputs at 200MHz C_L=15pF		335		mA
		VDD=2.5V, Outputs at 150MHz C_L=15pF		200		mA
		VDD=2.5V, Outputs at 200MHz C_L=15pF		240		mA
Output Impedance	Z_{OUT}		7		22	Ω

(1) Inputs have pull-up / pull down resistors that effect input current.

(2) Polarity (-): Outgoing current from device.
Polarity (+): Incoming current to device.

(3) Driving series or parallel terminated 50Ω (or 50Ω to VTT) transmission lines.

AC Characteristics <3.3V>

VDD = 3.3V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency	f_{IN}				200	MHz
Propagation Delay	t_{pd}	TCLK to any Q (1), (2)	0.9		2.5	ns
Output Duty Cycle	DC_{OUT}	Measured at VTT (1), (2), (3)	45		55	%
Output-to-Output Skew	t_{skpp}	(1), (2),		85	200	ps
Part-to-Part Skew (4)	t_{skD1}				1.6	ns
Part-to-Part Skew (5)	t_{skD2}				600	ps
Output Rise/Fall Time	t_r, t_f	0.8V to 2.0V (1), (2)	0.08		0.6	ns

(1) Outputs driving 50Ω transmission lines.
(2) See Figure 1.
(3) 50% input duty cycle.
(4) Across temperature and voltage ranges, includes output skew.
(5) For a specific temperature and voltage, includes output skew.

AC Characteristics <2.5V>

VDD = 2.5V±5%, Ta: -40 to +85℃, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Frequency	f_{IN}				200	MHz
Propagation Delay	t_{pd}	TCLK to any Q (1), (2)	1.0		3.0	ns
Output Duty Cycle	DC_{OUT}	Measured at VTT (1), (2), (3)	45		55	%
Output-to-Output Skew	t_{skpp}	(1), (2),		85	200	ps
Part-to-Part Skew (4)	t_{skD1}				2.0	ns
Part-to-Part Skew (5)	t_{skD2}				600	ps
Output Rise/Fall Time	t_r, t_f	0.5V to 1.8V (1), (2)	0.15		1.0	ns

(1) Outputs driving 50Ω transmission lines.
(2) See Figure 1.
(3) 50% input duty cycle.
(4) Across temperature and voltage ranges, includes output skew.
(5) For a specific temperature and voltage, includes output skew.

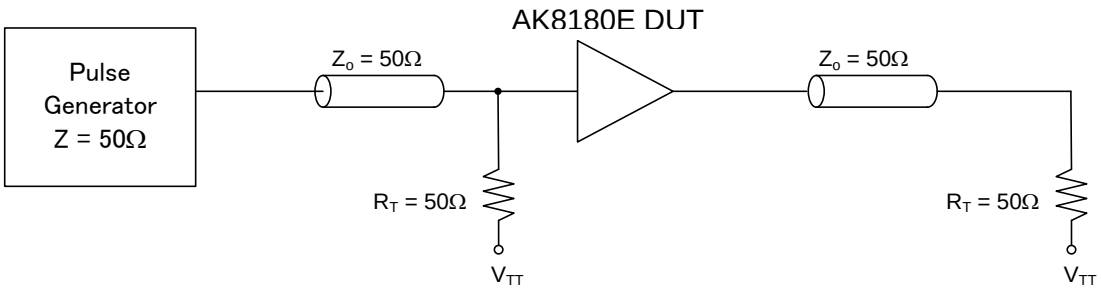


Figure 1. LVCMOS_CLK Test Reference

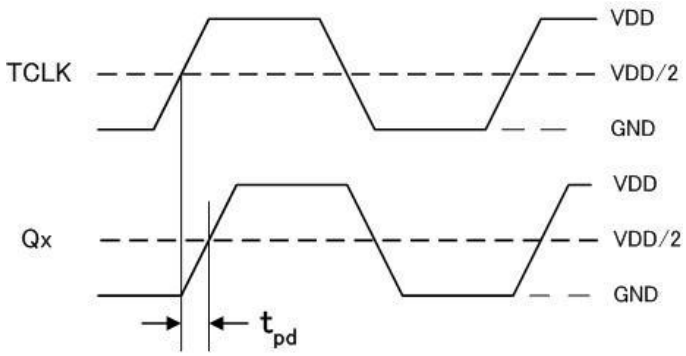


Figure 2. LVCMOS Propagation Delay (t_{pd}) Test Reference

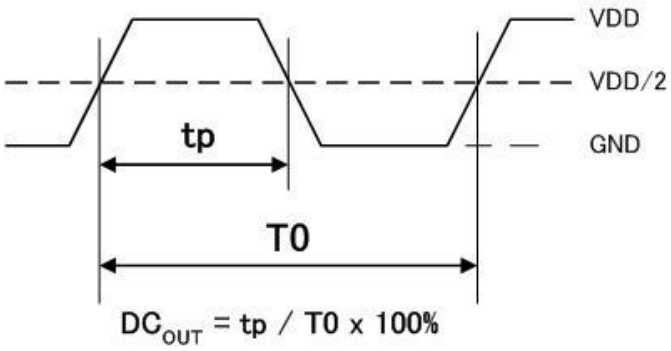


Figure 3. Output Duty Cycle (DC_{OUT})

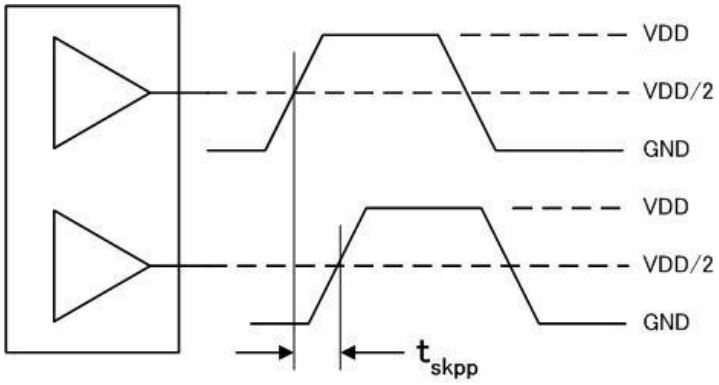


Figure 4. Output-to-Output Skew (t_{skpp})

Function Table

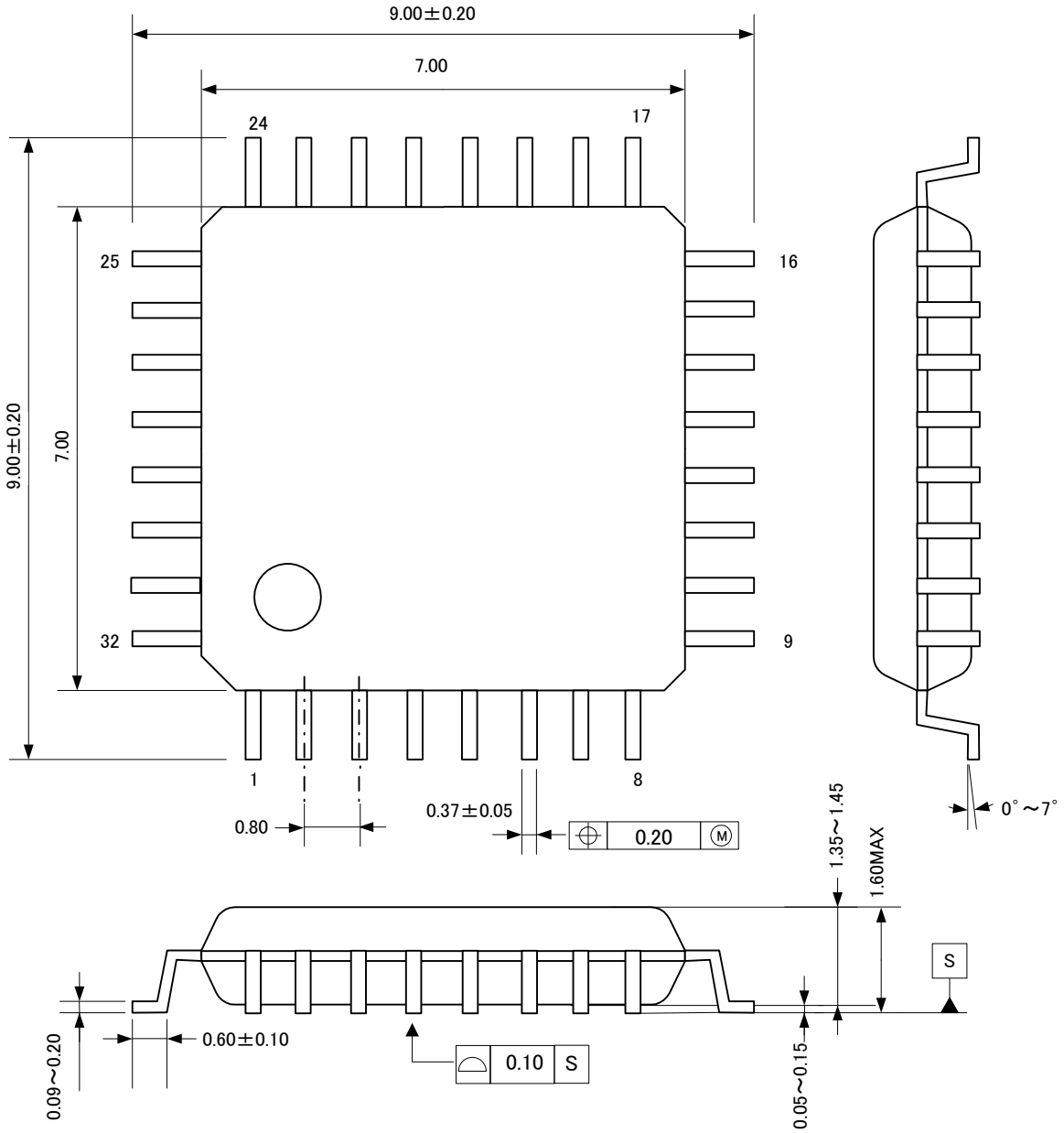
The following table shows the inputs/outputs clock state configured through the control pins.

Table 1: Control Input Function Table

Input	Output
OE	**Q0:Q17**
L	Disabled (high impedance)
H	Enabled

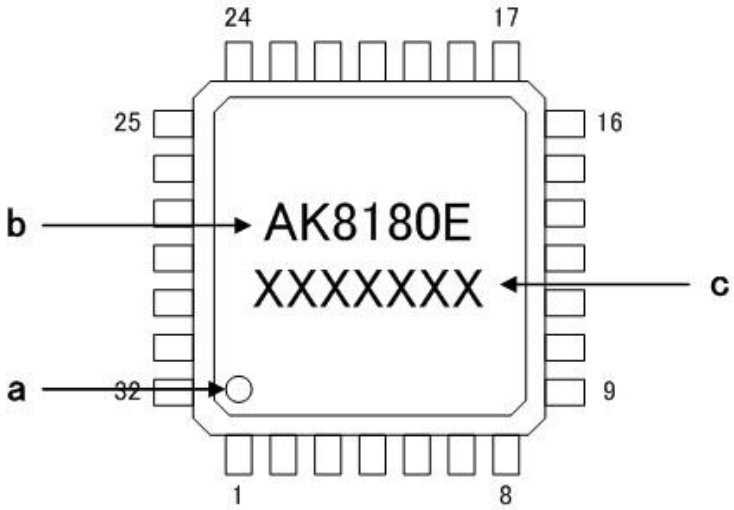
Package Information

- **Mechanical data : 32-lead LQFP**



- **Marking**

a: #1 Pin Index
b: Part number
c: Date code (7 digits)



(1) **AKM** is the brand name of AKM's IC's.

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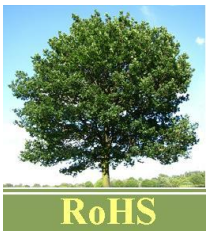
- **RoHS Compliance**



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(*) RoHS compliant products from AKM are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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