LC74735YW

CMOS LSI On-Screen Display Controller



Overview

The LC74735YW is an on-screen display CMOS IC that displays characters and patterns on a TV screen. For QVGA display, the LC74735YW supports the use of both a 12×18 dot character font and a 12×18 dot graphics font with 16 colors with a total of 512 characters and glyphs. For WVGA display, the LC74735YW supports the use of both a 24×32 dot character font and a 12×16 dot graphics font with 16 colors with a total of 512 characters and glyphs. The LC74735YW can also implement extremely varied displays by the use of an external ROM. The LC74735YW supports both QVGA (480×234) and WVGA (800×480).

Features

- Screen structure
- Main :

QVGA mode: 40 characters \times 13 lines (up to 520 characters) on a QVGA panel

- WVGA mode: 33 characters \times 15 lines (up to 495 characters) on a WVGA panel
- Wallpaper display screen: Permanent repetition of a 2×2 (horizontal \times vertical) character pattern
- Character structure
- -QVGA mode :
 - 12 dots (horizontal) \times 18 dots (vertical) : Character display
 - 12 dots (horizontal) × 18 dots (vertical) : Graphic glyph display
- WVGA mode:
 - 24 dots (horizontal) × 32 dots (vertical) : Character display
- 12 dots (horizontal) \times 16 dots (vertical) : Graphic glyph display (1 pixel : 2 \times 2 dots)
- Character display clock:
 - About 9 MHz QVGA with an LC oscillator 33.2 MHz (maximum: 40 MHz)
- WVGA with an external clock signal input *: The ROM image is known when QVGA or WVGA mode is specified.
- Number of characters: 512 (internal)
- Up to 2048 characters when an external 16-bit 4M ROM is used.
- Character sizes: Four horizontal sizes $(1 \times, 2 \times, 3 \times, and 4 \times)$
 - Four vertical sizes $(1\times, 2\times, 3\times, \text{ and } 4\times)$
 - (The character size is specified in line units.)
- Display start positions : 512 positions in the horizontal direction and 256 positions in the vertical direction.

QVGA mode WVGA mode Setting units : Horizontal : 1 dot 2 dots (In screen units)

Vertical: 1 dot 2 dots (In screen units)

- Display functions
- Blinking specification (in character units)
 Period : 1/64, 1/32, and 1/16 of the vertical sync signal (in screen units)
 Duty : Fixed at 50%
- Box (raised or recessed) display
- Raised/recessed specification (in character units)
- Left : Off/on specification (in character units)
- Right : Off/on specification (in character units)
- Top : Off/on specification (in character units)
- Bottom : Off/on specification (in character units)
- Border specification (in line units) :
- Only valid with glyphs from the character font.
- Color specification
- Character
- Character color (in character units) : 1 of 16 colors can be specified.
- Character background color (in character units) : 1 of 16 colors can be specified.
- Border color (in line units) : 1 of 16 colors can be specified.



SQFP80(12X12)

• Graphic

- 16 types can be specified by ROM data
- Box color (line units) : 1/16 colors
- Background color (screen units) : 1/16 colors
- Color table (palette)
- Sixteen colors can be selected from a set of 512 colors (One of which is specified to be transparent.)
- Number of color tables: 2. This allows up to 32 colors to be displayed at the same time.
- Wallpaper screen (Graphics glyphs only)
 - Wallpaper display : Repeated display under the main screen (2 characters horizontally by 2 characters vertically)

Sprite character display : Displayed above the main screen (2 characters horizontally by 2 characters vertically)

• Output

- QVGA
 - Analog RGB output
 - BLK (OSD display period signal)
- WVGA

Digital RGB output (3 bits per color)

- BLK (OSD display period signal)
- Package : SQFP80
- Voltage : 3.3 V

Package Dimensions

unit : mm



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

No.A2330-2/52

VDD3 VSS3 VDD3 VSS3 A10 A12 A11 A13 A14 A15 AO A5 A6 A7 A8 A9 Ą A2 A3 A4 80 74 73 72 71 70 69 79 78 77 76 75 68 67 66 65 64 63 62 61 VSS1 60 A16 1 OSCin 2 59 A17 OSCout 3 58 CE 57 OE CTRL1 4 SCLK 5 56 VDD3 55 VSS3 SIN 6 CS 7 54 D0 VDD1 8 53 D1 VSYNC 9 52 D2 VBLK 10 51 D3 HSYNC 11 50 D4 HBLK 12 49 D5 TEST1 13 48 D6 TEST2 14 47 D7 46 VDD1 RST 15 VSS1 16 45 VSS1 VDD1 17 44 D8 CLKOUT 18 43 D9 VSS1 19 42 D10 VDD1 20 41 D11

BD0 BLK VSS1

BD1

26 27 28 29 30 31 32 33 34 35

GD0 BD2

GD1

21 22 23 24 25

RD2

RD1

RD0 GD2 36 37

OUTR ROUT GOUT BOUT

VDD2

CCOMP

CVREF

38 39 40

RREF VSS2

Top view

Pin Assignments

Pin Functions

Pin No.	Symbol	Туре	Functional description						
1	V _{SS} 1	Ground	Connect a ground to this pin. (Digital system ground)						
2	OSCin		Connect to the character output dot clock generator oscillator coil and capacitor.						
3	OSCout	LC oscillator	May also be used for external clock input.						
4	CTRL1	OSCin oscillator input control	Switches between external clock input mode and LC oscillator mode. Low: LC oscillator, high: external clock input MORE+						
5	SCLK	Clock input	Clock input for the serial data input system MORE+ (This input has hysteresis characteristics.)						
6	SIN	Data input	Serial data input MORE+ (This input has hysteresis characteristics.)						
7	CS	Enable input	Enable input for the serial data input system. Serial data input is enabled when this pin is set low. MORE+ (This input has hysteresis characteristics.)						
8	V _{DD} 1	Power supply (+3.3 V)	Digital system power supply: +3.3 V						
9	VSYNC	Vertical sync signal input	Vertical sync signal input MORE+ (This input has hysteresis characteristics.)						
10	VBLK	Vertical blanking signal input	Vertical blanking signal input MORE+ (This input has hysteresis characteristics.)						
11	HSYNC	Horizontal sync signal input	Horizontal sync signal input MORE+ (This input has hysteresis characteristics.)						
12	HBLK	Horizontal blanking signal input	Horizontal blanking signal input MORE+ (This input has hysteresis characteristics.)						
13	TEST1	Test mode control 1	Test mode control 1 Low: normal operation, high: test mode MORE+						
14	TEST2	Test mode control 2	Test mode control 2 Low: normal operation, high: test mode (scan mode) MORE+						
15	RST	Reset input	System reset input MORE+ (This input has hysteresis characteristics.)						
16	V _{SS} 1	Ground	Connect a ground to this pin. (Digital system ground)						
17	V _{DD} 1	Power supply (+3.3 V)	Power supply: (+3.3 V: Digital system)						
18	CLKOUT	Clock output	Clock output						
19	V _{SS} 1	Ground	Connect a ground to this pin. (Digital system ground)						
20	V _{DD} 1	Power supply (+3.3 V)	Power supply: (+3.3 V: Digital system)						
21	RD2	Rout output: bit 2	Pout output						
22	RD1	Rout output: bit 1	Rout output This is a 3-bit digital output with values from 000 to 111.						
23	RD0	Rout output: bit 0							
24	GD2	Gout output: bit 2	Quit estant						
25	GD1	Gout output: bit 1	Gout output This is a 3-bit digital output with values from 000 to 111.						
26	GD0	Gout output: bit 0							
27	BD2	Bout output: bit 2	David suidavid						
28	BD1	Bout output: bit 1	Bout output This is a 3-bit digital output with values from 000 to 111.						
29	BD0	Bout output: bit 0							
30	BLK	Blanking signal output	This signal indicates the OSD display period.						
31	V _{SS} 1	Ground	Connect a ground to this pin. (Digital system ground)						
32	V _{DD} 2	Power supply (+3.3 V)	Power supply: (+3.3 V: D/A converter)						
33	OUTR	Outr output: analog	Output. Connect a resistor Ro (68 Ω) to this pin.						
34	Rout	Rout output: analog	D/A converter (3 bits) output. Connect a resistor Ro to this pin.						
35	Gout	Gout output: analog	D/A converter (3 bits) output. Connect a resistor Ro to this pin.						
36	Bout	Bout output: analog	D/A converter (3 bits) output. Connect a resistor Ro to this pin.						
37	CCOMP	Phase correction capacitor connection	Capacitor connection: 1.5 µF						
38	CVREF	Reference voltage output	Capacitor connection: 0.1 µF						
39	RREF	Reference resistor connection	Connect a reference register to this pin.						
	V _{SS} 2	Ground	Connect a ground to this pin. (D/A converter ground)						

Continued on next page.

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Pin No.	Symbol	Туре	Functional description						
41	D11	Data input 11	ROM data input 11. MORE+						
42	D10	Data input 10	ROM data input 10. MORE+						
43	D9	Data input 9	ROM data input 9. MORE+						
44	D8	Data input 8	ROM data input 8. MORE+						
45	V _{SS} 1	Ground	Connect a ground to this pin. (Digital system ground)						
46	V _{DD} 1	Power supply (+3.3 V)	Power supply: (+3.3 V: Digital system)						
47	D7	Data input 7	ROM data input 7. MORE+						
48	D6	Data input 6	ROM data input 6. MORE+						
49	D5	Data input 5	ROM data input 5. MORE+						
50	D4	Data input 4	ROM data input 4. MORE+						
51	D3	Data input 3	ROM data input 3. MORE+						
52	D2	Data input 2	ROM data input 2. MORE+						
53	D1	Data input 1	ROM data input 1. MORE+						
54	D0	Data input 0	ROM data input 0. MORE+						
55	V _{SS} 3	Ground	Connect a ground to this pin. (External ROM output system ground)						
56	V _{DD} 3	Power supply (+3.3 or +5.5 V)	Power supply (External ROM output system power supply)						
57	ŌE	Output enable	ROM output enable output. This is an active low output.						
58	CE	Chip enable	ROM chip enable output. This is an active low output.						
59	A17	Address output 17	ROM address output 17						
60	A16	Address output 16	ROM address output 16						
61	A15	Address output 15	ROM address output 15						
62	A14	Address output 14	ROM address output 14						
63	A13	Address output 13	ROM address output 13						
64	A12	Address output 12	ROM address output 12						
65	A11	Address output 11	ROM address output 11						
66	A10	Address output 10	ROM address output 10						
67	A9	Address output 9	ROM address output 9						
68	A8	Address output 8	ROM address output 8						
69	V _{SS} 3	Ground	Connect a ground to this pin. (External ROM output system ground)						
70	V _{DD} 3	Power supply (+3.3 or +5.5 V)	Power supply (External ROM output system power supply)						
71	A7	Address output 7	ROM address output 7						
72	A6	Address output 6	ROM address output 6						
73	A5	Address output 5	ROM address output 5						
74	A4	Address output 4	ROM address output 4						
75	A3	Address output 3	ROM address output 3						
76	A2	Address output 2	ROM address output 2						
77	A1	Address output 1	ROM address output 1						
78	A0	Address output 0	ROM address output 0						
79	V _{SS} 3	Ground	Connect a ground to this pin. (External ROM output system ground)						
80	V _{DD} 3	Power supply (+3.3 or +5.5 V)	Power supply (External ROM output system power supply)						

Specifications Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{DD} 1	V _{DD} 1, V _{DD} 2	V_{SS} – 0.3 to V_{SS} + 4.6	V
Supply voltage	V _{DD} 3	V _{DD} 3	$V_{\rm SS}$ – 0.3 to $V_{\rm SS}$ + 6.0	V
Input voltage	V _{IN}	All input pins	$V_{SS} - 0.3$ to $V_{DD}1 + 0.3$	V
Output voltage	V _{OUT} 1	RD2 to 0, GD2 to 0, BD2 to 0, and BLK outputs	$V_{SS} - 0.3$ to $V_{DD}1 + 0.3$	V
Output voltage	V _{OUT} 2	A0 to A17, CE, OE outputs	$V_{SS} - 0.3$ to $V_{DD}1 + 0.3$	V
Maximum power dissipation	Pdmax		230	mW
Operating temperature	Торд		-30 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

Recommended Operating Conditions

Deremeter	Cumhal	Conditions		Ratings		Unit
Parameter	Symbol	Conditions	min	min typ max		Unit
Supply voltage	V _{DD} 1	V _{DD} 1, V _{DD} 2	3.0	3.3	3.6	V
Supply voltage	V _{DD} 3	V _{DD} 3	3.0	3.3	5.5	V
	V _{IH} 1	CTRL1, TEST1, TEST2	0.7 V _{DD} 1	—	5.5	V
Input high-level voltage	V _{IH} 2	SCLK, SIN, CS, VSYNC, HSYNC, RST	0.8 V _{DD} 1	—	5.5	V
	V _{IH} 3	D0 to D11	0.7 V _{DD} 1	—	5.5	V
	V _{IL} 1	CTRL1, TEST1, TEST2	V _{SS} – 0.3	—	0.3 V _{DD} 1	V
Input low-level voltage	V _{IL} 2	SCLK, SIN, CS, VSYNC, HSYNC, RST	V _{SS} – 0.3	—	0.2 V _{DD} 1	V
	V _{IL} 3	D0 to D11	V _{SS} – 0.3	—	0.3 V _{DD} 1	V
Oscillator frequency	F _{OSC1}	OSCin and OSCout oscillator pins (LC oscillator)	_	10	_	MHz
	F _{OSC2}	OSCin, V _{DD} 1 = 3.3 V	_	33	40	MHz
External clock input	V _{IN} 1	V _{DD} 1 = 3.3 V, CTRL1 = high	0.5	—	3.3	Vp-p
	Vrefda	Reference voltage	_	1.1	_	V
D/A converter (3 bit, 3 ch)	Rfda	Output load resistance ROUT, GOUT, and BOUT	120	—	225	Ω
When maximum output voltage = 0.7 V	Rfbda	Output load resistance OUTR	40	—	75	Ω
	Rref	Reference load resistance, RREF	1232	_	2310	Ω

Electrical Characteristics at Ta = –30 to +70 $^{\circ}C,$ V_{DD} = 3.3 V unless otherwise specified.

Parameter	Symbol	Pin	Conditions		Ratings		Unit
Parameter	Symbol	Pin	Conditions	min	typ	max	Unit
	V _{OH} 1	RD2 to 0, GD2 to 0, BD2 to 0, and BLK outputs	V _{DD} 1 = 3.0 V I _{OH} 1 = -8 mA	V _{DD} 1 - 0.8	_	_	V
Output high-level voltage	V _{OH} 2	A0 to 17, \overline{CE} , and \overline{OE}	V _{DD} 3 = 3.0 V I _{OH} 2 = -8 mA	V _{DD} 3 - 0.8	_	_	V
	V _{OH} 3	A0 to 17, \overline{CE} , and \overline{OE}	V _{DD} 3 = 4.5 V I _{OH} 3 = -8 mA	V _{DD} 3 – 0.8	_	_	V
	V _{OL} 1	RD2 to 0, GD2 to 0, BD2 to 0, and BLK outputs	V _{DD} 1 = 3.0 V I _{OL} 1 = 8 mA	-	_	0.4	V
Output low-level voltage	V _{OL} 2	A0 to 17, \overline{CE} , and \overline{OE}	V _{DD} 3 = 3.0 V I _{OL} 2 = 8 mA	_	_	0.4	V
	V _{OL} 3	A0 to 17, \overline{CE} , and \overline{OE}	V _{DD} 3 = 4.5 V I _{OL} 3 = 8 mA	_	_	0.4	V
	I _{IH} 1	CTRL1, TEST1, TEST2, SCLK, SIN, CS, VSYNC, HSYNC, RST	$V_{IN} = V_{DD} 1$	_	_	10	μA
Input current	I _{IH} 2	D0 to 11	$V_{IN} = V_{DD}3$	—	—	10	μΑ
input current	I _{IL} 1	CTRL1, TEST1, TEST2, SCLK, SIN, \overline{CS} , VSYNC, HSYNC	V _{IN} = V _{SS}	-10	_	_	μA
	I _{IL} 2	D0 to 11	V _{IN} = V _{SS}	-10	—	_	μA
	I _{DD} 1	V _{DD} 1	All outputs open OSCin: 40 MHz	_	_	37	mA
Operating current drain	I _{DD} 2	V _{DD} 2	D/A on	—	—	22	mA
	I _{DD} 3	V _{DD} 3		—	—	20	mA
	CLK	Clock frequency			—	20	MHz
D/A converter	Vmax	Maximum output voltage	V _{DD} 2 = 3.3 V	0.25	—	1.5	V
	Vmin	Minimum output voltage	V _{DD} 2 = 3.3 V	_	0		V

Timing Characteristics OSD Write (See figure 1.) at Ta = -30 to +70 $^{\circ}C,$ $V_{DD}1$ = 3.3 \pm 0.3 V

Parameter	Symbol	Conditions		Unit		
Falalleter	Symbol			typ	max	Unit
Minimum input pulse width	t _w (sclk)	SCLK	200	_	_	ns
	t _w (cs)	\overline{CS} (The period \overline{CS} is high)	1	_	_	μs
Data setup time	t _{su} (cs)	CS	200	_	_	ns
	t _{su} (sin)	SIN	200	_	_	ns
Data hold time	t _h (cs)	CS	2	_	_	μs
	t _h (sin)	SIN	200	_	_	ns
One word write time	t _{word}	The time to write 8 bits of data	4.2	—	_	μs
	t _{wt}	RAM data write time	1	_	_	μs

Supplementary Materials





System Block Diagram



Display Control Commands

The display control commands have serial input format that consists of 8-bit units transmitted LSB first. A commands consists of a command identification code in the first byte and data in the second and following bytes. Both a first byte and a second byte (16 bits) must be transmitted for each command. Commands 10, 11, and 71 set the IC to continuous write mode. (Continuous write mode is cleared by setting the \overline{CS} pin high.)

Display Control Command Table

CommandQl (Write address) 1 0 0 0 0 V2 V1 V0 H6 H4 H3 H2 H1 H CommandQl (Write address) 1 0 0 0 1 0			First byte							Second byte							
CommandO (Write address) 1 0 0 0 0 V3 V2 V1 V0 H5 H4 H1 H1 CommandO1 (Write address) 1 0 0 1 0 0 1 0 0 SUB (Wallspeer) 1 0 0 1 0 0 1 0 0 SUB (Wallspeer) 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0<	Command	Comm	hand ide	entificati	on code		1	ata					Da	ata			
Main Image:		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Sub (Wallpaper) 1 0		1	0	0	0	0	0	V3	V2	V1	V0	H5	H4	H3	H2	H1	H0
Command 10 (Charactor wite) Main Image: Charactor wite) Main		1	0	0	0	0	1	0	0	0	SV0	0	0	0	0	0	SH0
Main Image: Second of the construction of the		1	0	0	1	0	0	RM2	RM1(1)	0	0	at	BXS	BXL	BXR	BXU	BXD
Image: Second and the setering thesetering the setting the setting the setting the setti	Command 10 (Character write)								(2)	CB3	CB2	CB1	CB0	CC3	CC2	CC1	CC0
Command 11 (Character write) 1 0 0 1 0 1 0 1 RM2 RM1(1) 0	Main								(3)	0	0	CT0	I/E	M/G	C10	C9	C8
Command 11 (Character write) Sub (Walipaper) Image: Command 20 (System control) Image: Command 20 (System control) <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>(4)</td> <td>C7</td> <td>C6</td> <td>C5</td> <td>C4</td> <td>C3</td> <td>C2</td> <td>C1</td> <td>C0</td>									(4)	C7	C6	C5	C4	C3	C2	C1	C0
Sub (Walpaper) Image: Command 20 (System control) 1 0 1 0 0 0 0 CTO LE M/G C10 C2 C11 C10 C10 C11 C10 C10 <thc10< td="" th<=""><td></td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>RM2</td><td>RM1(1)</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></thc10<>		1	0	0	1	0	1	RM2	RM1(1)	0	0	0	0	0	0	0	0
Command20 (System control) 1 0 1 0 </td <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td></td> <td>0</td> <td>0</td> <td>0</td> <td>0</td>										0	0	0		0	0	0	0
Command20 (System control) 1 0 1 0 1 0 </td <td>Sub (Wallpaper)</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>(3)</td> <td>0</td> <td>0</td> <td>CT0</td> <td>I/E</td> <td>M/G</td> <td>C10</td> <td>C9</td> <td>C8</td>	Sub (Wallpaper)								(3)	0	0	CT0	I/E	M/G	C10	C9	C8
Command21 (Display control) 1 0 1 0 0 0 0 1 LSSF BK1 BK0 SBG1 SBG0 DSPB6 DSPB6 <thdspb6< th=""> DSPB6 DSPB6</thdspb6<>									(4)	C7	C6	C5	C4	C3	C2	C1	C0
Command22 (UO polarity control 1) 1 0 1 0 0 0 1 0 BLD1 BLO0 BLO1 BLO0 CKP VIP HI Command22 (Green background olor) 1 0 1 0 0 1 1 0 0 0 1 0 0 0 0 1 0 <td>Command20 (System control)</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>TSTMD2</td> <td>TSTMD1</td> <td>Q/W2</td> <td>Q/W1</td> <td>SYSRST</td> <td>CTERS</td> <td>SRMERS</td> <td>MRMERS</td>	Command20 (System control)	1	0	1	0	0	0	0	0	TSTMD2	TSTMD1	Q/W2	Q/W1	SYSRST	CTERS	SRMERS	MRMERS
Command23 (Steen badgiound color) 1 0 1 0 0 1 1 0 0 0 1 1 0	Command21 (Display control)	1	0	1	0	0	0	0	1	LCSOFF	BK1	BK0	SBG1	SBG0	DSPBG	DSPGS	DSPGM
Command24 (I/O polarity control 2) 1 0 0 VPM7 VPM6 VPM5 VPM4 VPM3 VPM2 VPM1	Command22 (I/O polarity control 1)	1	0	1	0	0	0	1	0	BLD1	BLO0	BLOP	BLO1	BLO0	CKP	VIP	HIP
Command2E Countrol 1 0 1 0 1 0 1 0 1 Censurand30 Command26 (Vertical display start position: main) 1 0 1 1 0 0 0 VPM7 VPM6 VPM5 VPM3 VPM2 VPM1	Command23 (Screen background color)	1	0	1	0	0	0	1	1	-	-						BGC0
Command30 (Vertical display start position: main) 1 0 1 1 0 0 0 0 VPM7 VPM6 VPM3 VPM2 VPM1 VPM1 VPM3 Command31 (Horizontal display start position: main) 1 0 1 1 0 0 1 HPM8 HPM7 HPM6 HPM4 HPM3 HPM2 HPM1 HPM2 HPM3 HPM2 HPM1 HPM1 HPM4 HPM3 HPM2 HPM1 HPM1 HPM3 HPM3 HPM2 HPM1 HPM1 HPM3 HPM2 HPM1 HPM1 HPM1 HPM3 HPM2 HPM1 HPM1 HPM3 HPM2 HPM1 HPM1 HPM1 HPM3 HPM2 HPM1 HPM1 HPM3 HPM2 HPM1 HPM1 HPM3 HPM3 HPM2 HPM1 HPM1 HPM3 HPM2 HPM1 HP1 Command33 (Morizontal display start position: screen) 1 0 1 1 0 0 0 0 0 0 <td>Command24 (I/O polarity control 2)</td> <td>1</td> <td>-</td> <td></td> <td>0</td> <td>0</td> <td>1</td> <td>-</td> <td>0</td> <td>-</td> <td></td> <td>-</td> <td>-</td> <td>-</td> <td></td> <td></td> <td>HBP</td>	Command24 (I/O polarity control 2)	1	-		0	0	1	-	0	-		-	-	-			HBP
(Vertical display start position: main) 1 0 1 1 0 0 VPM7 VPM5 VPM4 VPM2 VPM2 VPM1 VPM1 VPM4 VPM2 VPM1		1	0	1	0	0	1	0	1	CEHSL	TOKSL	VIPSL	OTM2	OTM1	OTM0	QRM1	QRM0
(Horizontal display start position: main) 1 0 1 1 0 0 1 HPM8 HPM7 HPM6 HPM6 HPM4 HPM2 HPM1 HPM1 HPM2 HPM1 HPM1 HPM1 HPM3 HPM3 <td< td=""><td></td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>VPM7</td><td>VPM6</td><td>VPM5</td><td>VPM4</td><td>VPM3</td><td>VPM2</td><td>VPM1</td><td>VPM0</td></td<>		1	0	1	1	0	0	0	0	VPM7	VPM6	VPM5	VPM4	VPM3	VPM2	VPM1	VPM0
(Vertical display start position: sub) 1 0 1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 1 1 0 0 VPS7 VPS6 VPS5 VPS4 VPS3 VPS2 VPS1 VPS1 VPS1 VPS1 VPS1 VPS1 VPS1 VPS1 VPS3 VPS2 VPS1 VPS1 <td< td=""><td></td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>HPM8</td><td>HPM7</td><td>HPM6</td><td>HPM5</td><td>HPM4</td><td>HPM3</td><td>HPM2</td><td>HPM1</td><td>HPM0</td></td<>		1	0	1	1	0	0	1	HPM8	HPM7	HPM6	HPM5	HPM4	HPM3	HPM2	HPM1	HPM0
(Horizontal display start position: sub) 1 0 1 1 0 1 <td></td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>VPS7</td> <td>VPS6</td> <td>VPS5</td> <td>VPS4</td> <td>VPS3</td> <td>VPS2</td> <td>VPS1</td> <td>VPS0</td>		1	0	1	1	0	1	0	0	VPS7	VPS6	VPS5	VPS4	VPS3	VPS2	VPS1	VPS0
(Vertical display start position: screen) 1 0 1 1 0 0 VPG7 VPG6 VPG3		1	0	1	1	0	1	1	HPS8	HPS7	HPS6	HPS5	HPS4	HPS3	HPS2	HPS1	HPS0
(Horizontal display start position: screen) 1 0 1 1 0 1 1 0 1 HPG8 HPG7 HPG8 HPG3 HPG		1	0	1	1	1	0	0	0	VPG7	VPG6	VPG5	VPG4	VPG3	VPG2	VPG1	VPG0
(Character size control) 1 1 0 </td <td></td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>HPG8</td> <td>HPG7</td> <td>HPG6</td> <td>HPG5</td> <td>HPG4</td> <td>HPG3</td> <td>HPG2</td> <td>HPG1</td> <td>HPG0</td>		1	0	1	1	1	0	1	HPG8	HPG7	HPG6	HPG5	HPG4	HPG3	HPG2	HPG1	HPG0
(Character size control: line setting U) 1 1 0 0 1 0 0 1 0 0 1 1 0 0 1 0 0 1 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 0 1 1 1 1 0 <td></td> <td>1</td> <td>1</td> <td>0</td> <td>SZV1</td> <td>SZV0</td> <td>SZH1</td> <td>SZH0</td>		1	1	0	0	0	0	0	0	0	0	0	0	SZV1	SZV0	SZH1	SZH0
(Character size control: line setting D) 1 1 0 0 1 0 0 0 1 1 1 0 1 0 0 0 1 1 1 1 0 0 0 0 0 1 1 1 1 0 1 0 <td></td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>LSZ7</td> <td>LSZ6</td> <td>LSZ5</td> <td>LSZ4</td> <td>LSZ3</td> <td>LSZ2</td> <td>LSZ1</td> <td>LSZ0</td>		1	1	0	0	0	1	0	0	LSZ7	LSZ6	LSZ5	LSZ4	LSZ3	LSZ2	LSZ1	LSZ0
(Box control U) 1 1 0 1 0 0 0 0 0 BXUU 0 BXUU 0 BXUU <		1	1	0	0	1	0	0	0	LSZ15	LSZ14	LSZ13	LSZ12	LSZ11	LSZ10	LSZ9	LSZ8
(Box control D) 1 1 0 1 0 1 0 0 BXDW BXW 0 BXDCT0 BXDC3 BXDC2 BXDC1 BXDC3 BXDC2 BXDC1 BXDC3 BXDC2 BXDC1 BXDC3 BXDC3 BXDC2 BXDC3 BXDC4 BXD1 BXD3 LBX3 <td></td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>BXUW</td> <td>BXLW</td> <td>0</td> <td>BXUCT0</td> <td>BXUC3</td> <td>BXUC2</td> <td>BXUC1</td> <td>BXUC0</td>		1	1	0	1	0	0	0	0	BXUW	BXLW	0	BXUCT0	BXUC3	BXUC2	BXUC1	BXUC0
(Box control: line setting U) 1 1 0 1 1 0 0 0 LBX7 LBX6 LBX5 LBX4 LBX3 LBX2 LBX1 LBX1 LBX3 LBX2 LBX1		1	1	0	1	0	1	0	0	BXDW	BXRW	0	BXDCT0	BXDC3	BXDC2	BXDC1	BXDC0
(Box control: line setting D) 1 1 0 1 1 1 0 0 LBX15 LBX14 LBX13 LBX12 LBX11 LBX10 LBX10 LBX14 LBX13 LBX12 LBX11 LBX11 LBX11 LBX14 LBX13 LBX12 LBX11 LBX14 LBX13 LBX12 LBX11 LBX10 LBX14 LBX14 LBX13 LBX12 LBX11 LBX11 LBX14 LBX13 LBX12 LBX11 LBX14 LBX13 LBX12 LBX11 LBX11 LBX14 LBX13 LBX12 LBX14 LBX13 LBX12 LBX14 LBX14 </td <td></td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>LBX7</td> <td>LBX6</td> <td>LBX5</td> <td>LBX4</td> <td>LBX3</td> <td>LBX2</td> <td>LBX1</td> <td>LBX0</td>		1	1	0	1	1	0	0	0	LBX7	LBX6	LBX5	LBX4	LBX3	LBX2	LBX1	LBX0
(Border control) 1 1 1 1 0 0 0 BLK1 BLK0 0 0 0 EGC1 EGC3 EGC2 EGC1 EGC3 EGC2 EGC1 EGC3		1	1	0	1	1	1	0	0	LBX15	LBX14	LBX13	LBX12	LBX11	LBX10	LBX9	LBX8
(Border control: line setting U) 1 1 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 0 0 1 1 1 1 1 0 0 1 1 1 1 0 1 0 0 0 1 1 1 1 1 0 1 0 0 0 0 0 1 1 1 1 1 0		1	1	1	0	0	0	BLK1	BLK0	0	0	0	EGCT0	EGC3	EGC2	EGC1	EGC0
(Border control: line setting D) 1 1 1 0 1 0 0 0 1 1 1 1 0 1 0 0 0 1 1 1 1 1 1 0 0 0 0 1 1 1 1 1 1 1 1 0		1	1	1	0	0	1	0	0	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
Color table 1 1 1 1 1 0 <th< td=""><td></td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>LFC15</td><td>LFC14</td><td>LFC13</td><td>LFC12</td><td>LFC11</td><td>LFC10</td><td>LFC9</td><td>LFC8</td></th<>		1	1	1	0	1	0	0	0	LFC15	LFC14	LFC13	LFC12	LFC11	LFC10	LFC9	LFC8
		1	1	1	1	0	0	0	0	0	0	0	CTN1	CTA3	CTA2	CTA1	CTA0
	Command71 (Data write) Color table	1	1	1	1	0	1	0	RMB(1) (2)	-	0 0	0 TG2	0 TG1	TCK TG0	TB2 TR2	TB1 TR1	TB0 TR0

Command 00 (Main screen write address set command)

• First byte

DA0 to 7	Pagiatar		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	0	Command 0 identification code	
5	—	0	Main screen write address setting	
4	—	0		
3	—	0	Sub-identification code: 0	
2	—	0		
1	V3	0		
	<msb></msb>	1		
0	V2	0		
0	٧Z	1		

DA0 to 7	Pagiator		Content	Notes
DAU IO 7	Register	State	Function	Notes
7	V1	0	Main screen memory line address	
	VI	1	(0 to E, hexadecimal)	
6	V0	0	QVGA mode: 13 lines	
0	<lsb></lsb>	1	WVGA mode: 15 lines	
5	H5	0		
5	<msb></msb>	1		
4	H4	0		
4		1		
3	H3	0	Main screen memory character position address	
3	пэ	1	(00 to 27, hexadecimal)	
2	H2	0	QVGA mode: 40 characters	
2	112	1	WVGA mode: 33 characters	
1	H1	0		
	111	1		
0	H0	0		
0	<lsb></lsb>	1		

Command 01 (Subscreen write address set command)

• First byte

DA0 to 7	Pagiatar		Content	Notes	
DAU 10 7	Register	State	Function	Notes	
7	—	1			
6	—	0	Command 0 identification code		
5	—	0	Subscreen memory write address setting		
4	—	0			
3	—	0	Sub-identification code: 1		
2	—	1			
1	_	0			
0	_	0			

DA0 to 7	Degister		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	0		
6	VO	0	Subscreen memory line address	
0	VU	1	(0 to 1, hexadecimal) 2 lines	
5	—	0		
4	—	0		
3	—	0		
2	—	0		
1	—	0		
0	HO	0	Subscreen memory character address	
	<lsb></lsb>	1	(0 to 1, hexadecimal) 2 characters	

Command 10 (Main screen display character data write setting command)

• First byte

DA0 to 7	Register				C	Content			Notes			
DAU 10 7	Register	State				Function			Notes			
7	—	1										
6	_	0	C	ommand 1	identificati	on code			When this command has been issued, the IC remains in display character data write mode until			
5	_	0	Di	splay char	acter data	write setting			the \overline{CS} pin is set high.			
4	_	1	1									
3	_	0	<u> </u>	.h. identifie	otion anda	0						
2	—	0		ub-identific	ation code	0						
4	RM2	0		RM2	RM1	M	ode]				
	RIVIZ	1	11	0	0	(1)(2)(3)(4)	End					
			-	0	1	(1)(2)(3)(4)	Continuous	1	Continuous write mode selection			
	DM4	0		1	0	(3)(4)	Continuous]				
0	RM1	1] [1 1 (2)(3)(4) Continuous								

• Second byte (1)

DA0 to 7	Degister		Content	Notes
DAU 10 7	0 to 7 Register	State	Function	Notes
7	—	0		
6	—	0		
5	at	0	Blinking off	Blinking specification
5	al	1	Blinking on	
4	BXS	0	Raised	
4	BAS	1	Recessed	Box specification: raised/recessed
3	BXL	0	None	Box specification: left side
3	BAL	1	Box displayed	box specification. Ien side
2	BXR	0	None	Box specification: right side
2	DAR	1	Box displayed	box specification. right side
4	BXU	0	None	
1	ВЛО	1	Box displayed	Box specification: upper
0	BXD	0	None	Pay aposition: lower
0	DVD	1	Box displayed	Box specification: lower

• Second byte (2)

DAG to 7	Desister		Content	Nister-
DA0 to 7	to 7 Register		Function	Notes
7	CB3	0		
	[MSB]	1		
6	CB2	0		
0	CB2	1	Character background color specification	Character background color specification When a character glyph is specified, 1 of 16 colors
5	CB1	0	0000 to 1111, or 0 to F (hexadecimal)	may be selected.
5	СВТ	1		
4	CB0	0		
4	[LSB]	1		
3	CC3	0		Character color specification When a character glyph is specified, 1 of 16 colors
3	[MSB]	1		
2	CC2	0		
2	002	1	Character color specification	
1	CC1	0	0000 to 1111, or 0 to F (hexadecimal)	may be selected.
I I		1		
0	CC0	0		
0	<lsb></lsb>	1		

• Second byte (3)

DA0 to 7	A0 to 7 Pogiator		Content	Notos
DAU 10 7	A0 to 7 Register	State	Function	Notes
7	_	0		
6	_	0		
5	CT0	0	Color table number 1	Color table selection
5	CIU	1	Color table number 2	
4	I/E	0	Internal ROM	ROM selection
4	1/ 12	1	External ROM	
3	M/G	0	Character	Character/graphic specification
3	W/G	1	Graphic	Character/graphic specification
2	C10	0		
2	[MSB]	1		
1	4 00	0		Character and appecification
	C9	1		Character code specification
0	C8	0		
0	6	1		

• Second byte (4)

DA0 to 7	Degister		Content	Notes
DAU 10 7	A0 to 7 Register	State	Function	Notes
7	C7	0		
	07	1		
6	C6	0		
0	0	1	Character code	
5	C5	0	Internal ROM: 512 characters 000 to 1FF (hexadecimal)	
5	0.5	1	0 to 511	
4	C4	0		
4	04	1	External ROM: 2048 characters 000 to 7FF (hexadecimal)	
3	63	0	0 to 2047	Character code specification
5	C3	1		
2	C2	0	 Transparent character specification I/E = 0 (Internal ROM) 	
2	02	1	M/G = 0 (Character)	
1	C1	0	Code = 1FF (hexadecimal)	
1		1		
0	C0	0		
0	[LSB]	1		

Command 11 (Subscreen display character data write setting command)

• First byte

	Pagiator		Content						Notes		
DA0 10 7	0A0 to 7 Register					Function			Notes		
7	—	1									
6	_	0	Command 1 identification code						When this command has been issued, the IC remains in display character data write mode until		
5	—	0	Di	splay char	acter data	write setting			the \overline{CS} pin is set high.		
4	—	1	1								
3	—	0	<u> </u>	.h. identifie	otion anda	4					
2	_	1		ub-identific	ation code	I					
4	RM2	0		RM2	RM1	N	lode]			
1	RIVIZ	1		0	0	[1][2][3][4]	End				
				0	1	[1][2][3][4]	Continuous	1	Continuous write mode selection		
0	RM1	RM1	5144	0		1	0	[3][4]	Continuous	1	
0			1		1	1	[2][3][4]	Continuous]		

• Second byte (1)

	DA0 to 7 Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	_	0		
6		0		
5		0		
4		0		
3		0		
2		0		
1		0		
0		0		

• Second byte (2)

DA0 to 7	Register		Content	Notes
DAU IO 7	Register	State	Function	Notes
7		0		
6		0		
5		0		
4		0		
3		0		
2		0		
1		0		
0		0		

• Second byte (3)

DAG to 7	DA0 to 7 Register		Content	Netza
DAU 10 7	A0 to 7 Register	State	Function	Notes
7	_	0		
6	_	0		
5	CT0	0	Color table number 1	Color table selection
5	CIU	1	Color table number 2	
4	I/E	0	Internal ROM	ROM selection
4	1/ 12	1	External ROM	
3	M/G	0	Only when transparent is selected	Graphic only
3	W/G	1	Graphic only	Graphic only
2	C10	0		
2	[MSB]	1		
1	4 00	0		Character and an activitien
	C9	1		Character code specification
0	C8	0		
0	0	1		

• Second byte (4)

DA0 to 7	Pagiatar		Content	Notes
DAU 10 7	A0 to 7 Register	State	Function	- Notes
7	C7	0		
1	07	1		
6	C6	0		
0	0	1	Character code	
5	C5	0	Internal ROM: 512 characters 000 to 1FF (hexadecimal) 0 to 511	
5	05	1		
4	C4	0		
4	04	1	External ROM: 2048 characters 000 to 7FF (hexadecimal) Character code specificat	Character code specification
3	C3	0	0 to 2047	
5	C3	1		
2	C2	0	 Transparent character specification I/E = 0 (Internal ROM) 	
2	2 02	1	M/G = 0 (Character)	
1	C1	0	Code = 1FF (hexadecimal)	
		1		
0	C0	0		
0	[LSB]	1		

Command 20 (System control setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	0	Command 2 identification code	
5		1	System control settings	
4		0		
3		0		
2		0	Sub-identification code 0	
1		0		
0		0		

DA0 to 7	Pagiator		Content	Notes
DAU IO 7	Register	State	Function	- INOLES
7	TSTMD2	0	Normal operation	Do not use test mode. This bit must always be set
	15TIVID2	1	Test mode 2	to 0.
6	TSTMD1	0	Normal operation	Do not use test mode. This bit must always be set
0	ISTIVIDT	1	Test mode 1	to 0.
5	Q/W2	0	Normal mode	Normal / Independent
5	Q/WZ	1	Independent mode Specified by COM24.	
4	Q/W1	0	QVGA mode D/A converter on, 40 characters × 13 lines	QVGA / WVGA
4	Q/W1	1	WVGA mode D/A converter off, 33 characters × 15 lines	_ QVGA7 WVGA
3	SYSRST	0		The registers are reset when the \overline{CS} pin is low.
3	515851	1	Reset all registers (All bits set to 0.)	The reset state is cleared when the CS pin goes high.
2	CTERS	0		Applications must provide a wait time of about 1ms.
2	CIERS	1	Erase the color table. (Sets all values to 00.)	Use DSPOFF to execute this operation.
		0		
1	1 SRMERS	1	Erase main RAM. (Sets all values to 00.) Wallpaper	 Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.
		0		
0	0 MRMERS	1	Erase sub-RAM. (Sets all values to 00.) Main screen	Applications must provide a wait time of about 1ms. Use DSPOFF to execute this operation.

Command 21 (Display control setting command)

• First byte

DA0 to 7	DA0 to 7 Bogistor		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	_	0	Command 2 identification code	
5	—	1	Display control	
4	—	0		
3	—	0		
2	_	0	Extended command 1 identification code	
1		0		
0		1		

• Second byte

DA0 to 7	Degister				Content	Notos
DAU 10 7	Register	State			Function	Notes
7	LCSOFF	0	Enables :	stopping	the LC oscillator	LC oscillator on/off control
	LCSOFF	1	Disables	stopping	the LC oscillator	Valid when the display is off.
6	BK1	0	BK1	BK0	Blinking period	
0	DKI	1	0	0	1/16	Blinking period
_		0	0	1	1/32	Specified for screen units.
5	BK0	1		0	1/64	
4	SBG1	0	Display a	fter the r	nain screen	Cuberreen display aposition
4	SEGI	1	Display b	efore the	e main screen	Subscreen display specification
3	SBG0	0	Iterated d	lisplay (v	vallpaper)	Subarran diaplay apolitication
3	3660	1	Horizonta	al 2-chara	acter x vertical 2-ch	splay (sprite) Subscreen display specification
2	DSPBG	0	Display o	ff		Screen background color
2	DSFBG	1	Display o	n		Scieen background color
1	DSPGS	0	Display o	ff		Subscroon (wallpaper)
	Dorgo	1	Display o	n		Subscreen (wallpaper)
0	DSPGM	0	Display o	ff		Main screen
0	DSPGIN	1	Display o	n		

Command 22 (I/O polarity control setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	_	1		
6	_	0	Command 2 identification code	
5	—	1	I/O polarity control 1	
4	—	0		
3	—	0		
2	_	0	Extended command 2 identification code	
1		1		
0		0		

• Second byte

DA0 to 7	Degister		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	BLD1	0	BLD1 BLD0 BLY output delay	
'	DEDT	1	$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	BLK output delay setting
		0	1 0 +2	In dot clock units
6	BLD0	1	1 1 +3	
5	BLOP	0	BLK output: positive polarity	BLK output polarity selection
5	BLOF	1	BLK output: negative polarity	BER output polarity selection
4	BLO1	0	BLO1 BLO0 BLK output	
4	BLUT	1	0 0 Text + character background + wallpaper + screen background	BLK output control
_	DI OO	0	0 1 Text + character background + wallpaper 1 0 Text + character background	
3	BLO0	1	1 1 Text	
2	СКР	0	Clock input: positive polarity	
2	CKF	1	Clock input: negative polarity	Clock input polarity selection
1	VIP	0	VSYNC input: negative polarity	VSYNC input polarity selection
	VIF	1	VSYNC input: positive polarity	
0	HIP	0	HSYNC input: negative polarity	HSYNC input polarity selection
	THE	1	HSYNC input: positive polarity	

Command 23 (Screen background color setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	DA0 to 7 Register		Function	
7	_	1		
6		0	Command 2 identification code	
5	_	1	Screen background color	
4	_	0		
3	_	0		
2	_	0	Extended command 3 identification code	
1		1		
0		1		

• Second byte

DA0 to 7	Pagiatar		Content	Notes
DAU IO 7	Register	State	Function	Notes
7	_	0		
6	_	0		
5	BGCT1	0	T1 T0 Color table setting 0 0 Color table No. 2	Screen background color
4	BGCT0	0	0 1 Invalid setting 1 X Color table No. 1	Color table setting
3	BGC3	0		
3	BGC3	1		
2	BGC2	0		
2	BGC2	1	Screen background color 0000 to 1111	Screen background color
1	BGC1 0		0 to F (hexadecimal)	Selects 1 of 16 values.
	BGCI	1		
0	PCC0	0		
0	0 BGC0			

Command 24 (I/O polarity control setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	DA0 to 7 Register		Function	Notes
7	—	1		
6	—	0	Command 2 identification code	
5	—	1	I/O polarity control 2	
4	—	0		
3	—	0		
2	_	1	Extended command 4 identification code	
1		0		
0		0		

• Second byte

DA0 to 7	Degister		Content	Notes
DAU 10 7	Register	State	Function	Noles
7	DSPMD1	0	MD1 MD0 Main screen display area 0 0 40 characters × 13 lines	Main screen display area selection Only valid in independent mode. COM20 to COM2
6	DSPMD0	0	0 1 33 characters × 15 lines 1 0 40 characters × 16 lines	*: In WVGA mode: fixed 33-character × 15-line display
5	D/ASEL	0	On Off	D/A converter used/unused selection Only valid in independent mode. COM20 to COM2
4	VBLKON	0	Disabled	VBLK input selection
3	HBLKON	0	Enabled Disabled	- HBLK input selection
3	HELKON	1	Enabled	
2	СКОР	0	Clock output positive polarity	
2	2 CROP		Clock output negative polarity	Clock output polarity selection
1	VBP	0	VBLK input negative polarity	VBLK input polarity selection
1	VDF	1	VBLK input positive polarity	VBLK Input polarity selection
0	HBP	0	HBLK input negative polarity	HBLK input polarity selection
0	TIBE	1	HBLK input positive polarity	

Command 25 (Output control 3 setting command)

• First byte

DA0 to 7	Pagiator		Content	Notes
DAU 10 7	DA0 to 7 Register		Function	Notes
7	—	1		
6	_	0	Command 2 identification code	
5	—	1	Output control	
4	—	0		
3	—	0		
2	_	1	Extended command 5 identification code	
1		0		
0		1		

• Second byte

DA0 to 7	Register		Content					Notes						
DAUIO7	Register	State	State Function						Notes					
-	051101	0	Normal ope	eration										
7	CEHSL	1	CE pin hele	d fixed at th	ne high leve	el			CE pin					
		0	Normal mo	de										
6	TOKSL	1	Transmissi The color s in the trans	specified at		in coloi	r table No. 1 is disp	blayed	Transmissive mode specification					
5	VIPSL	0	Falling edge detection											
5	VIPSL	1	Rising edge detection						Selects the detection polarity for the VSYNC signal.					
	OTMDO	0	Output off state (always low)						CLKOUT pin (pin 18)					
4	OTMD2	1	Normal out	put					Output control					
	OTUDA	0	OTMD2	OTMD1	OTMD0		Output	1						
3	OTMD1	1		0		Norm		1						
		0	0	0	1	RGB	No. 1	1	A0 to 17 output selection					
2		OTMD0						0	1	0	RGB	-		
_	••••••	1	0	1	1	High-i	mpedance state]						
		0					-							
1	QRM1	1	QRM1	QRM0	ROM sel		-							
			0	0	RON RON		4		ROM selection when character output is specified					
		0		0	RON		{		in QVGA mode					
0	QRM0	1	1	1	RON	-]							

*: This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

• When RGB No. 1 or RGB No. 2 is selected:

The A17 to 9 output is set to the RD2 to BD0 three-value output. (Supported by connecting external resistors.)

* It will not be possible to use external ROM in this case. (Only internal ROM can be used.)

No. 1: RGB = 000 = Black only. Here the output will go to the high-impedance state giving the middle level due to the external resistor. For areas other than the display area, the output will be at the low level.

No. 2: When any individual color is zero, the output will go to the high-impedance state giving the middle level due to the external resistor. For areas other than the display area, the output will be at the low level.

Command 30 (Main screen: vertical display start position setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	Register	State	Function	Notes
7	_	1		
6		0	Command 3 identification code	
5	_	1	Main screen: vertical display start position setting	
4	_	1		
3	_	0		
2	_	0	Extended command 0 identification code	
1	_	0		
0	_	0		

DA0 to 7	Pagiatar			Content	Notes
DAU IO 7	Register	State		Function	Notes
7	VPM7	0			
1	(MSB)	1	The ver	tical display start position, VSM, is given by:	
6	VPM6	0	VSM	$= 1H \times (\sum_{n=1}^{7} 2^{n} V P M n)$	
0	VEINO	1		n=0	
5	VPM5	0		HSYNC	Main screen
5	VT 1015	1			The vertical display start position is specified by the
4	VPM4	0			8 bits VPM7 to 0.
7	V1 IVI-	1		VSM	The weight of the LSB is 1H in QVGA mode, and
3	VPM3	0	VSYNC		the weight of the LSB is 2H in WVGA mode
0	VI MO	1	\S/	HSM Main scroon display graa	-
2	VPM2	0		HSM Main screen display area	This setting applies in screen units.
2	VI IVIZ	1			
1	VPM1	0			
	VI IVII	1			
0	VPM0	0			
5	(LSB)	1			

Command 31 (Main screen: horizontal display start position setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	0	Command 3 identification code	
5	—	1	Main screen: horizontal display start position setting	
4	—	1		
3	—	0		
2	—	0	Extended command 1 identification code	
1	—	1		
0	HPM8	0		
0	(MSB)	1		

• Second byte

DA0 to 7	Pagiator		Content	Notes	
DAU IO 7	Register	State	Function	notes	
7	HPM7	0			
1		1			
6	HPM6	0	The horizontal display start position, HSM, is given by:		
0		1			
5	HPM5	0	$HSM = 1Tc \times (\sum_{n=0}^{2} HPMn) + \alpha$	Main screen	
Ŭ		1	α = 57 Tc		
4	HPM4	0		The horizontal display start position is specified by the 9 bits HPM8:0.	
		1	Tc: The input clock frequency in operating mode.	The weight of the LSB is 1TC in QVGA mode, and	
3	HPM3	0		the weight of the LSB is 2TC in WVGA mode	
		1		Ŭ	
2	HPM2	0	Setting disable range	This setting applies in screen units.	
_		1	QVGA : 00 to 07 HEX		
1	HPM1	0	WVGA : 00 to 07 HEX		
		1			
0	HPM0	0			
	(LSB)	1			

Command 32 (Subscreen: vertical display start position setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	DA0 to 7 Register		Function	Notes
7	—	1		
6	—	0	Command 3 identification code	
5	—	1	Subscreen: vertical display start position setting	
4	—	1		
3	—	0		
2	—	1	Extended command 2 identification code	
1	_	0		
0	_	0		

DA0 to 7	Register				Co	ntent	Notes	
DAU 10 7	Register	State				Function	Notes	
7	VPS7	0						
'	(MSB)	1	The ve	rtical dis	play start	position, VSS, is given by:		
6	VPS6	0		– 1H v (∑2 ⁷ VP	Sn)		
0	VF 30	1			n=0			
5	VPS5	0				HSYNC		Subscreen (wallpaper)
Ŭ	11.00	1		. –		Home		The vertical display start position is specified by the
4	VPS4	0		<u> </u>		1		8 bits VPS7 to 0.
		1				VSS		The weight of the LSB is 1H in QVGA mode, and
3	VPS3	0	VSYNC			¥		the weight of the LSB is 2H in WVGA mode
		1	N		HSS	• Outra and a disal automatic		
2	VPS2	0	-		1100	Subscreen display area		This setting applies in screen units.
		1						
1	VPS1	0						
		1						
0	VPS0	0						
Ŭ	(LSB)	1						

Command 33 (Subscreen: horizontal display start position setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	0	Command 3 identification code	
5	—	1	Subscreen: horizontal display start position setting	
4	—	1		
3	—	0		
2	—	1	Extended command 3 identification code	
1		1		
0	HPS8	0		
0	0 (MSB)	1		

• Second byte

DA0 to 7	Pagiator		Content	Notes
DAUIO7	Register	State	Function	Notes
7	HPS7	0		
'	111 07	1		
6	HPS6	0	The horizontal display start position, HSS, is given by:	
0	11 00	1	8 (No. 17 (No. 1170))	
5	HPS5	0	$HSS = 1Tc \times (\sum_{n=0}^{\infty} 2^{n}HPSn) + \alpha$ $\alpha = 14 Tc$	Subscreen (wallpaper)
4	HPS4	0		The horizontal display start position is specified by the 9 bits HPS8 to 0.
-	111 04	1	Tc: The input clock frequency in operating mode.	The weight of the LSB is 1TC in QVGA mode, and
3	HPS3	0		the weight of the LSB is 2TC in WVGA mode
Ŭ		1		
2	HPS2	0		This setting applies in screen units.
_		1	Setting disable range	0.11
1	HPS1	0	QVGA : 00 to 2F HEX	
		1	WVGA : 00 to 17 HEX	
0	HPS0	0		
	(LSB)	1		

Command 34 (Screen background color: vertical display start position setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	A0 to 7 Register		Function	Notes
7	—	1		
6	—	0	Command 3 identification code	
5	—	1	Screen background color: vertical display start position setting	
4	—	1		
3	—	1		
2	—	0	Extended command 4 identification code	
1	_	0		
0	_	0		

DA0 to 7	Register				Co	ntent	Notes	
DAU IU 7	Register	State				Function	NOLES	
7	VPG7	0						
'	(MSB)	1	The ve	rtical dis	splay start	position, VSG, is given by:		
6	VPG6	0	Vec	- 1U V	(∑2°VP	2 n)		
0	VPG6	1	030		(<u>2</u> 2 VF) n=0	511)		
5	VPG5	0					Screen background color	
5	VFG5	1		HSYNC				
4	VPG4	0]					The vertical display start position is specified by the 8 bits VPG7 to 0.
4	VF 64	1				VSG		The weight of the LSB is 1H in QVGA mode, and
3	VPG3	0	VSYNC			¥		the weight of the LSB is 2H in WVGA mode
		1	<pre>S</pre>		← → →	Screen background		
2	VPG2	0			1100	color display area		This setting applies in screen units.
2	11 02	1						
1	VPG1	0						
I	vrGi	1						
0	VPG0	0						
0	(LSB)	1						

Command 35 (Screen background color: horizontal display start position setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	0	Command 3 identification code	
5	—	1	Screen background color: horizontal display start position setting	
4	—	1		
3	—	1		
2	—	0	Extended command 5 identification code	
1		1		
0	HPS8	0		
0 (MSB)		1		

• Second byte

DA0 to 7	Pagiator		Content	Notes	
DAUIO7	Register	State	Function	Notes	
7	HPG7	0			
	TIF G7	1			
6	HPG6	0	The horizontal display start position, HSG, is given by:		
0	TIF G0	1	8		
5	HPG5	0	$HSG = 1Tc \times (\sum_{n=0}^{\infty} 2^n H P G n)$		
5	TIF 05	1	Tc: The input clock frequency in operating mode.	Screen background color	
4	HPG4	0		The horizontal display start position is specified by	
-	111 04	1		the 9 bits HPG8 to 0.	
3	HPG3	0		The weight of the LSB is 1TC in QVGA mode, and	
5	TIF 05	1		the weight of the LSB is 2TC in WVGA mode	
2	HPG2	0		This setting applies in screen units.	
2	111 02	1			
1	HPG1	0			
	11 01	1			
0	HPG0	0			
	(LSB)	1			

Command 40 (Character size control setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7			Function	Notes
7	—	1		
6	—	1	Command 4 identification code	
5	—	0	Display character data write settings	
4	—	0		
3	—	0	Extended command 0 identification code	
2	—	0		
1		0		
0		0		

• Second byte

DA0 to 7	Pagiator		Content		Notes		
DAU 10 7	Register	State	State Function				Notes
7	_	0					
6	_	0					
5	_	0					
4	_	0					
3	SZV1	0	SZV1	SZV0	Character size		
-		1	0	0	1×		Specifies the character size in the vertical direction.
		0	0	1	2×		This setting applies in line units.
2	SZV0		1	0	3×		
		1	1	1	4×		
		0	0714	07110	Oh ann at an air a		
1	SZH1	1	SZH1 0	SZH0 0	Character size 1×		Specifies the character size in the horizontal
		0	0	1	2×		direction.
		0	1	0	3×		This setting applies in line units.
0	SZH0	1	1	1	4×		

Command 41 (Character size line U control setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7			Function	Notes
7	_	1		
6	—	1	Command 4 identification code	
5	—	0	Character size line U control	
4	—	0		
3	—	0	Extended command 1 identification code	
2	—	1		
1	_	0		
0	_	0		

DA0 to 7	Degister	Content		Notes	
DA0 to 7 Register		State Function		notes	
7	LSZ7	0	Do not set for line 8.		
1	L3Z1	1	Set for line 8.		
6	LSZ6	0	Do not set for line 7.		
0	L320	1	Set for line 7.		
5	LSZ5	0	Do not set for line 6.		
5	L325	1	Set for line 6.		
4	4 LSZ4	0	Do not set for line 5.	Character size line setting control Upper lines	
4	L324	1	Set for line 5.		
3	LSZ3	0	Do not set for line 4.		
3	L323	1	Set for line 4.		
2	LSZ2	0	Do not set for line 3.		
2	LOZZ	1 Set for line 3.		_	
1	LSZ1	0	Do not set for line 2.		
I	LOZI	1	Set for line 2.		
0	LSZ0	0	Do not set for line 1.		
U	L320	1	Set for line 1.		

Command 42 (Character size line D control setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	DA0 to 7 Register		Function	Notes
7	_	1		
6	—	1	Command 4 identification code	
5	—	0	Character size line D control	
4	—	0		
3	—	1	Extended command 2 identification code	
2	—	0		
1	_	0		
0	_	0		

DA0 to 7	Decister	Content		Notes
DA0 to 7 Register		State Function		INDIES
7	LSZ15	0	Do not set for line 16.	
<i>'</i>	1 15215	1	Set for line 16.	
6	LSZ14	0	Do not set for line 15.	
0	L3Z14	1	Set for line 15.	
5	LSZ13	0	Do not set for line 14.	
5	L3213	1	Set for line 14.	
4	4 LSZ12	0	Do not set for line 13.	
4	LOZIZ	1	Set for line 13.	Character size line setting control
3	LSZ11	0	Do not set for line 12.	Lower lines
3	LOZII	1	Set for line 12.	
2	LSZ10	0	Do not set for line 11.	
2	L3210	1 Set for line 11.		
1	LSZ9	0	Do not set for line 10.	
I	L329	1	Set for line 10.	
0	LSZ8	0	Do not set for line 9.	
0	L320	1	Set for line 9.	

Command 50 (Box control: U setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	1	Command 5 identification code	
5	—	0	Box control U settings	
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	—	0		
0	_	0		

• Second byte

	DA0 to 7 Register		Content	Notes	
DAUIO7			Function		
7	BXUW	0	Box display: upper side is 1 dot.	Box display: upper side	
	BAUW	1	Box display: upper side is 2 dots.	Dot width. This setting applies in line units.	
6	BXLW	0	Box display: left side is 1 dot.	Box display: left side	
0	BALVV	1	Box display: left side is 2 dots.	Dot width. This setting applies in line units.	
5		0			
4	4 BXUCT0	0	Color table No. 1	Box display: upper side Color table specification	
4	BAUCTU	1	Color table No. 2	This setting applies in line units.	
3	BXUC3	0			
3	BAUC3	1			
2	BXUC2	0			
2	BAUCZ	1	Box display: upper side color specification 0000 to 1111	Box display: upper side	
1	BXUC1	0	0 to F (hexadecimal)	Color specification This setting applies in line units.	
	BAUCT	1			
0	BXUC0	0			
	BAUCU	1			

Command 51 (Box control: D setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7			Function	Notes
7	—	1		
6	—	1	Command 5 identification code	
5	—	0	Box control D settings	
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	1		
1	_	0		
0	—	0		

• Second byte

DAO to 7	DA0 to 7 Register		Content	Notes	
DAU IO 7			Function		
7	BXDW	0	Box display: lower side is 1 dot.	Box display: lower side	
	BADW	1	Box display: lower side is 2 dots.	Dot width. This setting applies in line units.	
6	BXRW	0	Box display: right side is 1 dot.	Box display: right side	
0	DARW	1	Box display: right side is 2 dots.	Dot width. This setting applies in line units.	
5	_	0			
4	4 BXDCT0	0	Color table No. 1	Box display: lower side Color table specification	
4	BADCIU	1	Color table No. 2	This setting applies in line units.	
3	BXDC3	0			
3	BADC3	1			
2	BXDC2	0	7		
2	BADC2	1	Box display: lower side color specification 0000 to 1111	Box display: lower side	
1	BXDC1	0	0 to F (hexadecimal)	Color specification This setting applies in line units.	
	DADCI	1			
0	BXDC0	0			
0	BADCO	1			

Command 52 (Box control: U line setting command)

• First byte

DA0 to 7	DA0 to 7 Register		Content	Notes
DAU 10 7			Function	Notes
7	—	1		
6	—	1	Command 5 identification code	
5	—	0	Box control U line setting	
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	—	0		
0	—	0		

DA0 to 7	Degister	Content		Notes	
DAU 10 7	DA0 to 7 Register		Function	noies	
7	LBX7	0	Do not set for line 8.		
'	LBAT	1	Set for line 8.		
6	LBX6	0	Do not set for line 7.		
0	LBA0	1	Set for line 7.		
5	LBX5	0	Do not set for line 6.		
5	LBAS	1	Set for line 6.		
4	4 LBX4	0	Do not set for line 5.	Box control line setting control Upper lines	
4	LDA4	1	Set for line 5.		
3	LBX3	0	Do not set for line 4.		
5	LBAS	1	Set for line 4.		
2	LBX2	0	Do not set for line 3.		
2	LDAZ	1	Set for line 3.		
1	LBX1	0	Do not set for line 2.		
I	LDAT	1	Set for line 2.]	
0	LBX0	0	Do not set for line 1.		
0	LDAU	1	Set for line 1.		

Command 53 (Box control: D line control setting command)

• First byte

DA0 to 7 Register			Content	Notes
DAU 10 7	Register	State	Function	Notes
7	—	1		
6	—	1	Command 4 identification code	
5	—	0	Box control D line setting	
4	—	0		
3	—	1	Extended command 3 identification code	
2	—	1		
1	_	0		
0	_	0		

DA0 to 7	Degister		Content	Notes
DA0 to 7 Register		State Function		- Notes
7	LBX15	0	Do not set for line 16.	
1	/ LBX15	1	Set for line 16.	
6	LBX14	0	Do not set for line 15.	
0	LDA14	1	Set for line 15.	
5		0	Do not set for line 14.	
5	LBX13	1	Set for line 14.	
4	4 LBX12	0	Do not set for line 13.	Box control line setting control Lower lines
4	LBATZ	1	Set for line 13.	
3	LBX11	0	Do not set for line 12.	
3	LBATT	1	Set for line 12.	
2	LBX10	0	Do not set for line 11.	
2	LBATO	1	Set for line 11.	-
1	LBX9	0	Do not set for line 10.	
1	LDVA	1	Set for line 10.	
0	LBX8	0	Do not set for line 9.	
0	LDAO	1	Set for line 9.	

Command 60 (Border control setting command)

• First byte

DA0 to 7	Register				Content		Notes	
DAU 10 7	Register	State			Function		Notes	
7	—	1						
6	_	1	Command	6 identifica	ation code			
5	—	1	Border con	trol setting				
4	—	0	1					
3	—	0	Extended) identification code			
2	—	0		ommanu (deminication code			
1	DL K4	0	BLK1	BLK0	Border mode specification			
	BLK1	DLKI	1	0	0	Normal display		Border mode specification
		0	0	1	Border		This setting applies in line units.	
0	BLK0	0	1	0	Shadow 1 (lower side)		The setting applies in the units.	
		1	1	1	Shadow 2 (lower and right sides)			

• Second byte

DA0 to 7	Register	Content		Natao
		State	Function	Notes
7	—	0		
6	—	0		
5	_	0		
4	EGCT0	0	Color table No. 1	Border display Color table specification This setting applies in line units.
		1	Color table No. 2	
3	EGC3	0	Border display: color specification 0000 to 1111 0 to F (hexadecimal)	Border display color specification This setting applies in line units.
		1		
2	EGC2	0		
		1		
1	EGC1	0		
		1		
0	EGC0	0		
		1		
Command 61 (Border control U line setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU 10 7		State	Function	Notes
7	—	1		
6	—	1	Command 6 identification code	
5	—	1	Border control U line setting	
4	—	0		
3	—	0	Extended command 1 identification code	
2	—	1		
1	_	0		
0	—	0		

• Second byte

DA0 to 7	Register		Content	Notes
		State	Function	Notes
7	LFC7	0	Do not set for line 8.	
1	LFC/	1	Set for line 8.	
6	LFC6	0	Do not set for line 7.	
0	LFC0	1	Set for line 7.	
5	LFC5	0	Do not set for line 6.	
5		1	Set for line 6.	
4	LFC4	0	Do not set for line 5.	
4	LFC4	1	Set for line 5.	Border control line settings control
3	LFC3	0	Do not set for line 4.	Upper lines
3	LFC3	1	Set for line 4.	
2	LFC2 -	0	Do not set for line 3.	
2		1	Set for line 3.	
1	LFC1	0	Do not set for line 2.	
1	60	1	Set for line 2.	
0	LFC0	0	Do not set for line 1.	
U		1	Set for line 1.	

Command 62 (Border control D line setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU 10 7		State	Function	Notes
7	—	1		
6	—	1	Command 6 identification code	
5	—	1	Border control D line setting	
4	—	0		
3	—	1	Extended command 2 identification code	
2	—	0		
1	—	0		
0	—	0		

• Second byte

DA0 to 7	Register		Content	Notes
		State	Function	Notes
7	LFC15	0	Do not set for line 16.	
<i>'</i>	LFC15	1	Set for line 16.	
6	LFC14	0	Do not set for line 15.	
0	LFC14	1	Set for line 15.	
5	LFC13	0	Do not set for line 14.	
5	LFC13	1	Set for line 14.	
4	LFC12	0	Do not set for line 13.	
4	LFG12	1	Set for line 13.	Border control line settings control
3	LFC11	0	Do not set for line 12.	Lower lines
5	LICH	1	Set for line 12.	
2	LFC10	0	Do not set for line 11.	
2	LFC10	1	Set for line 11.	
1	LFC9 -	0	Do not set for line 10.	
I	LI C9	1	Set for line 10.	
0	LFC8	0	Do not set for line 9.	
0		1	Set for line 9.	

Command 70 (Color table write address setting command)

• First byte

DA0 to 7	Register		Content	Notes
DAU 10 7		State	Function	Notes
7	_	1		
6	—	1	Command 7 identification code	
5	—	1	Color table write address setting	
4	—	1		
3	—	0	Sub-identifier code 0	
2	—	0		
1	_	0		
0	_	0		

• Second byte

DA0 to 7	Register		Content	Notes
DAU IO 7		State	Function	
7	—			
6	—			
5	—			
4	CTN1	0	Color table No. 1 selected	Color table selection
4	CINI	1	Color table No. 2 selected	No. 1 or No. 2
3	CTA3	0		
3	<msb></msb>	1		
2	CTA2	0		
2	CTAZ	1	Color table address 0 to 15	Addresses of the color tables
1	CTA1	0	0 to F (hexadecimal) 16 values	
I		1		
0	CTA0 <lsb></lsb>	0		
0		1		

Command 71 (Color table data write setting command)

• First byte

DA0 to 7	Register	Content		Notes	
DAU 10 7		State	Function	Notes	
7	—	1			
6	—	1	Command 7 identification code	When this command has been issued, the IC remains in display character data write mode until the \overline{CS} pin is set high.	
5	—	1	Display character data write setting		
4	_	1			
3	_	0	Sub-identifier code 1		
2	—	1			
1	—	0			
0	RM3	0	RM3 Mode 0 [1][2] End 1 [1][2] Continuous	Continuous write mode selection	

• Second byte (1)

DA0 to 7	Register		Content	Notes
DAU 10 7		State	Function	Notes
7	—	0		
6	—	0		
5	—	0		
4	—	0		
3	ТОК	0	Color	
3		1	Transparent (BLK output: low)	
2	TB2	0	Color table	
2	I DZ	1		
1	TB1	0		Color table setting B
	IBI	1	000 to 111	
0	TB0		0 to 7 (hexadecimal)	
0	IBU	1		

• Second byte (2)

DA0 to 7	Register	Pogiator		Content	Notes
DAU 10 7		State	Function	Notes	
7	_	0			
6	_	0			
5	TG2	0			
э	TG2	1	Color table		
4	TG1	0	G output	Color table setting G	
4	IGI	1	000 to 111	Color table setting G	
3	TG0	0	0 to 7 (hexadecimal)		
3	160	1			
2	TR2	0			
2	TRZ	1	Color table		
1	TR1	0	Routput	Color table setting R	
	IK1	1	000 to 111		
0	TR0	0	0 to 7 (hexadecimal)		
0		1			

*: This register is set to the all bits zero state when the IC is reset by the $\overline{\text{RST}}$ pin.

When transparent is selected, the BLK output is set to the low level. (Transparent state) The RGB outputs are values from the color table.

The transparent specification is best for color table 1, address 0000.

Since the data is set to all zeros by a RAM clear operation,

the RGB output will be 000 (black) and the BLK output will be 1.

Transparent is specified by setting the TOK bit to 1. (The BLK output will go to the low level.)

Display Structure

The display screen consists of a 40-character \times 15-line grid.

QVGA mode (12×18 dot characters)

40-character \times 13-line QVGA panel (480 \times 234)

WVGA mode (12×16 dot characters)

33-character \times 15-line WVGA panel (800 \times 480)

Up to a maximum of 600 characters can be displayed.

If the character size is increased, the number of characters that can be displayed will decrease to be fewer than 600 characters.

Display memory is addressed by specifying a line address (0 to 14 (decimal) and a character position address (0 to 39 (decimal)).



Display Structure (Display memory address)

Sample Application Circuits

• QVGA mode (analog output)



• WVGA mode (digital output)



Operational Description

Command transfer method

Overview

- Commands are transferred in 8-bit units, LSB first. Always send a first byte and a second byte (16 bits).
- Command 10 (Main RAM write)
 - Command 11 (Wallpaper write)
 - Command 71 (Color table write)

When these commands specify continuous mode (RM2, 1 RM3), the IC is locked in continuous write mode. (Continuous write mode is cleared by setting the CS $\overline{\text{pin}}$ high.)

Writing Data to VRAM

- Write start address specification
 - Use command 00 to set the write start address.
 - V3:0: Vertical direction, H5:0: Horizontal direction
- Data write

Continuous write mode differs depending on the write mode specification. (RM1, RM2)

- 1 Normal (RM2 = 0, RM1 = 0: initial state) *Continuous mode not used* -- COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 command wait state --
- 2 Write continuous (RM2 = 0, RM1 = 1): Mode 2 COM10-1 ↓10-2-1 10-2-2 10-2-3 10-2-4 ¬
- 3 Write continuous (RM2 = 1, RM1 = 0): Mode 3 COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 ▲10-2-3 10-2-4 ¬
- 4 Write continuous (RM2 = 1, RM1 = 1): Mode 4 COM10-1 10-2-1 10-2-2 10-2-3 10-2-4 ▲10-2-2 10-2-3 10-2-4 ¬
- *: In modes 2, 3, and 4, the IC remains locked in continuous write mode until the $\overline{\text{CS}}$ pin is set high.

• The write address is automatically incremented.

• The write address is retained unless the IC is reset or a new write address is issued.

Color Table write

• Write start address specification

Use command 70 to set the color table write start address.

CTN1: Color table specification (No.1, No.2), CTA3 to 0: Address specification



• Data write

Continuous write mode differs depending on the write mode specification. (RM3)

- Normal (RM3 = 0: initial state) *Continuous mode not used*
 COM71-1 71-2-1 71-2-2 command wait state ---
- 2 Write continuous (RM3 = 1) mode COM71-1 ▲ 71-2-1 71-2-2 ¬

*: In mode 2, the IC remains locked in continuous write mode until the $\overline{\text{CS}}$ pin is set high.

- The write address is automatically incremented.
- The write address is retained unless the IC is reset or a new write address is issued.

Display format

Color Specification Related Items

- When a character is specified
 - Specify color with the character color (character area) and character background color (outside the character area) Character color: One of 16 colors

Character background color: One of 16 colors

Color tables: Table No. 1 or No. 2 specified by CT1 to CT0. (COM1-2-3: VRAM)

 \rightarrow One of 32 types



• When a graphic is specified

Specify color is in dot units $(12 \times 18 \text{ or } 12 \times 16)$

One of 16 colors (FROM)

Color tables: Table No. 1 or No. 2 specified by CT1 to CT0. (COM1-2-3: VRAM)

 \rightarrow One of 32 types



Display Control Related Items

- Blinking: In character units
 - Normal at1 = 0 (COM1-2-1: VRAM)



Blinking at1 = 1Display alternates between normal and transparent with the blinking period. (COM21-2: BK1, 0)

• Border display: Only valid for font specified characters

Border color: One of 16 colors (COM60-2 EGC3 to 0) Color table specification (COM60-2 EGCT0)

 \rightarrow One of 32 types

Border mode control (COM60-1 BLK1, 0)





Shadow 2: lower + right



• Character size: Specified in line units

The character size is specified as 1x to 4x independently for the vertical and horizontal directions. (COM40-2)

Box Display (raised/recessed)



- Raised/recessed specification: In character units (COM10-2-1 BXS)
- Left side displayed/undisplayed specification: in character units (COM10-2-1 BXL)
- Right side displayed/undisplayed specification: in character units (COM10-2-1 BXR)
- Upper side displayed/undisplayed specification: in character units (COM10-2-1 BXU)
- Lower side displayed/undisplayed specification: in character units (COM10-2-1 BXD)
- Color specification: In line units

COM50 (Upper side) COM51 (Lower side) BXUC3:0: One of 16 colors BXDC3:0: One of 16 colors

Color table specification

BXUCT0

- BXDCT0
- ' One of 32 types

Dot width specification: 1 or 2 dots

Each of left, right, upper, and lower can be specified independently. (BXLW BXRW BXUW BXDW)

LC74735YW

Screen Structure

Screen ba	ackground color	
	Wallpaper display screen	
	Main screen	
	QVGA mode (12 × 18 dot characters) 40-character × 13-line QVGA panel WVGA mode (12 × 16 dot characters) 33-character × 15-line WVGA panel	

- For each screen: Display on/off (transparent) can be specified independently.
- For each screen: The display start position can be specified independently. The wallpaper display screen and the main screen require xxxx clocks before the horizontal start position is reached.

Display Format

• QVGA



• WVGA



ROM structure

Internal ROM (512 characters)

• Character font

QVGA: 12×18 -dot structure

WVGA: 24×32 -dot structure, i.e. 12×16 times 4

• Graphics

CQVGA: 12×18 -dot structure

WVGA: 12×16 -dot structure, i.e. displayed magnified $2 \times$ in both the horizontal and vertical directions.

Note that the contents of ROM differ for QVGA and WVGA. (That is, different ROMs for QVGA and WVGA must be created.)

External ROM (2048 characters)

• Conditions

Use a 16-bit 4M ROM with an access time less than 3 times the dot clock period Example: DCLK = 50 MHz = 20 ns period \times 3 = under 60 ns DCLK = 10 MHz = 100 ns period \times 3 = under 300 ns

• ROM map



A17 to A7 (10 bits) = 2048 characters = character codes

• Display appearance

QVGA: 1 character = 12×18 dots Character font: [1] Graphics: [1] + [2] + [3] + [4] WVGA: 1 character = 12×16 dots Character font: [1] [2] [3] [4]

Graphics: ([1] + [2] + [3] + [4]) displayed magnified $2 \times$ in both the horizontal and vertical directions.



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