

## ZL70571/72/73/74/88 Medical Surge Protection Device (Data Sheet)

### **Features**

- Extremely Fast Turn-On
- Very Small Size and Very Low Leakage
- 5, 6 and 7 Terminals Available
- Standard Delivery Form: Solder Bumped Die
- Variant for Wire Bonding: ZL70588
- Facilitates Compliance with EN-45502 and EN-50061
- Superior Quality
  - QA Procedures Based on MIL-PRF-38535
  - Traceability for Every Chip to Lot and Wafer Number
  - 100% Burn-In Capability
  - <u>L</u>ot <u>A</u>cceptance <u>T</u>esting (LAT) Included

### **Applications**

- Pacemakers and Neurostimulators
- Medical Devices with Electronics Requiring Protection
   against a High Voltage Surge

### **Ordering Information**

ZL70571UDJ	Bumped Die, Waffle Tray
ZL70571UDJ	Bumped Die, Waffle Tray

- ZL70572UDJ Bumped Die, Waffle Tray
- ZL70573UDJ Bumped Die, Waffle Tray
- ZL70574UDJ Bumped Die, Waffle Tray
- ZL70588UBJ Wirebondable Die, Waffle Tray

0°C to +55°C.



Figure 1 • ZL70573 Block Diagram









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# 1 – Description

The ZL70571/72/73/74/88 is a family of transient surge suppressing devices designed specifically for implanted medical devices. The device terminals exhibit extremely low leakage during normal voltages and can therefore be connected in parallel with the pins of the device they protect. When the voltage rises to dangerous level it then rapidly turns on and limits the voltage by shunting the current through its thyristors. This makes the ZL70571/72/73/74/88 family an effective means of compliance with international regulations EN-45502, "Active Implantable" and EN-50061, "Safety of Implantable Cardiac Pacemakers".



# 2 – Applications

The EN-45502 standard states that all active medical devices implanted in a human torso should not be permanently affected by an external defibrillation of the patient. Compliance is confirmed if the implanted device continues to meet device specification after being subjected to a sequence of 140-volt pulses, in series with a 300-ohm resistor between each conductive part of the device, including the device case (see EN-45502 for details). The ZL70571/72/73/74/88 family meets this test and is an effective means of complying with the EN-45502 standard. Without surge protection, the electronics, in almost all cases would be destroyed. The same compliance tests are also described in EN-50061.

In the application example shown in Figure 2-1, each of the dual chamber pacemaker's terminals, and the case, are connected to a terminal on the protection device. If a defibrillation pulse causes the ventricular tip to begin to go positive, relative to the case, the ZL70571 thyristor structure rapidly becomes active and forms a low impedance path between T2 and T3 to absorb the current and limit the voltage. This provides an effective means of protecting the pacemaker chip. The voltages and currents the implanted device is subjected to in an actual defibrillation can be higher than described in EN-45502/EN-50061 and has been taken into account in the design of the ZL70571/72/73/74/88 family.



#### Figure 2-1 • Pacemaker Application Example

Terminals placed most remotely to others must get special attention since they effectively form a large pick-up coil and could therefore be exposed to a large amount of current. When implanted, the pacemaker case is placed beneath the collarbone and all other terminals are placed together inside the heart. For this reason, the largest current will pass through the surge protection terminal connected to the case of the pacemaker. For ZL70571/72, it is recommended that the case be connected to T3 of the protection device; this terminal is designed to withstand the largest amount of current. If the ZL70573/74/88 device is used in a 5 terminal application, we recommend that 2/3/3 pins of the protection device are connected to the implantable device terminal with the largest current flow (typically the terminal for the device case).



Pin #	In/Output	Name	Description
1	I	T1	Transient Surge Protection Terminal 1
2	I	T2	Transient Surge Protection Terminal 2
3	I	Т3	Transient Surge Protection Terminal 3
4	I	T4	Transient Surge Protection Terminal 4
5	I	Т5	Transient Surge Protection Terminal 5
6	I	Т6	Transient Surge Protection Terminal 6
7	I	T7	Transient Surge Protection Terminal 7 (ZL70574 and ZL70588 only)

Table 2-1 • Pin Description Table — ZL70573, ZL70574, and ZL70588

<u>ZL70573</u>











Figure 2-2 • ZL70573 and ZL70574 Bumped Chip Appearance and ZL70588 Bond Pad Placement



Pin #	In/Output	Name	Description
1	I	T1	Transient Surge Protection Terminal 1
2	I	T2	Transient Surge Protection Terminal 2
3	I/O	SUB1	Transient Surge Protection Substrate Connection 1
4	I	Т3	Transient Surge Protection Terminal 3 Doubled Area
5	I/O	SUB2	Transient Surge Protection Substrate Connection 2
6	I	T4	Transient Surge Protection Terminal 4
7	I	T5	Transient Surge Protection Terminal 5

*Table 2-2* • Pin Description Table — ZL70571 and ZL70572

#### ZL70571 and ZL70572



Figure 2-3 • ZL70270, ZL70571 and ZL70572 Bumped Chip Appearance



## **3 – Functional Description**

### ZL70573

The ZL70573 is a six-branch device. The suppression is achieved by a self-triggering thyristor-diode device in parallel with a diode between each branch-input and a common node which is also the substrate of the device. The six branches of the device are reached through terminals T1, T2, T3, T4, T5, and T6. The electrical characteristic observed between any two of the terminals (T1, T2, T3, T4, T5, and T6) very much resembles that of a DIAC (see Figure 4-2 on page 4-4).

When a transient current is forced between two branch-input terminals, the positive terminal will be clamped to the common node by the thyristor-diode of one branch and the negative terminal of the forward voltage diode of other branch. Due to the low on-state voltage of the thyristor that voltage will stay at a safe value during the transient.

ZL70573 has a very high dV/dt immunity, > 2,300 V/µs.

### ZL70574 and ZL70588

The ZL70574 and ZL70588 are seven-branch devices with exactly the same electrical characteristics as ZL70573.

### ZL70571 and ZL70572

The ZL70571 and ZL70572 are five-branch transient surge suppressing devices with the same functionality as ZL70573. The only functional difference is that the substrate of the device is accessible through the two terminals SUB1 and SUB2.

ZL70571 and ZL70572 have both an excellent peak voltage handling in the turn-on, they are on in < 150 ns. Because of that, the peak voltage is reduced to a minimum in the overshot. As a drawback of this characteristic, dV/dt is guaranteed to be better than > 100 V/µs.



## 4 – Electrical Data

	Parameter	Sym.	Min.	Max.	Units	Test Conditions
1	Storage temperature range	Τ <sub>S</sub>	-40	125	°C	
2	Maximum junction temperature	Τj		125	°C	
3	Maximum surge current	ITSM		8	A	Test according to Figure 4-1 on page 4-3. tp for flip mounted chips with underfill: 10 ms. tp die wire bonded die: 1 ms.
4	Continuous power dissipation	Pmax		300	mW	t > 1 s

#### Table 4-1 • Absolute Maximum Ratings\*

\* Exceeding these values may cause permanent damage. Functional operations under these conditions is not implemented.

#### Table 4-2 • Recommended Operating Conditions

	Parameter	Sym.	Min.	Typ. <sup>1</sup>	Max.	Units	Test Conditions
5	Operating temperature range	T <sub>OP</sub>	0	37	55	°C	

Note:

1. Typical figures are at 37°C and are for design only.

#### Table 4-3 • DC Electrical Characteristics @ +37°C

	Parameter	Sym.	Min.	Тур.	Max.	Units	Test Conditions
6	Forward breakdown voltage	Iz = 10 μA					
	ZL70573/74/88	Vfz	9.0	10.1	11.0	V	
	ZL70571	Vfz	9.0	9.5	12.2	V	
	ZL70572	Vfz	17.0	18.0	19.5	V	
7	Forward breakdown voltage	, Zener die	ode, term	iinal to su	bstrate		Iz = 10 μA
	ZL70571	Vfz	8.5	9.2	11.5	V	
	ZL70572	Vfz	16.5	17.7	19.0	V	
8	Breakover voltage, terminal	to termina	1				Figure 4-2 on page 4-4
	ZL70573/74/88	Vbo	9.0	11.2	12.0	V	
	ZL70571	Vbo	9.0	10.5	12.2	V	
	ZL70572	Vbo	17.0	18.7	19.5	V	
9	Breakover voltage, terminal	to substra	te				Figure 4-2 on page 4-4
	ZL70571	Vbo	8.5	9.8	11.5	V	
	ZL70572	Vbo	16.5	18.4	19.0	V	
10	Forward diode voltage drop	, substrate	to termi	nal			Measured at 2 A
	ZL70571/72	Vfwd			2	V	



	Parameter	Sym.	Min.	Тур.	Max.	Units	Test Conditions
11	Breakover current	1					Figure 4-2 on page 4-4
	ZL70573/74/88	lbo		15	200	mA	
	ZL70571/72	lbo		15	40	mA	
12	Holding current	lh	1			mA	Figure 4-2 on page 4-4
13	On-state voltage terminal to terminal	Von		2.2	3.0	V	Measured with a 300 µs pulse, IT = 1 A
14	On-state voltage terminal to substrate, ZL70571/72	Von		1.0	3.0	V	Measured with a 300 $\mu$ s pulse, IT = 1 A
15	On-state dynamic resistanc	e					Measured with a 300 µs pulse,
	ZL70571/73/74/88	Ron		0.4	1	Ω	dIT = 1–2 A
	ZL70572	Ron		0.3	1	Ω	-
16	Off-state current, terminal to						
	ZL70573/74/88	ld		10	100	nA	Measured at 8.0 V
	ZL70571	ld		10	150	nA	Measured at +8.5 V
	ZL70572	ld		10	150	nA	Measured at +16.5 V
17	Off-state current terminal to						
	ZL70571	ld		10	150	nA	Measured at +8.0 V
	ZL70572	ld		10	150	nA	Measured at +16.0 V
18	After surge pulse	Δld			20	nA	Force 3 current surge pulses, with max 10 s between each (I = 3 A, t = 2 ms), between the terminal under test and the res of inputs (they should be tied together). If there are substrate connections, these should be le floating.
19	Parasitic capacitance		·	-	·		
	ZL70573/74/88	Ср			50	pF	
20	Parasitic capacitance	•	•		•		
	ZL70571/72	Ср			200	pF	

#### Table 4-3 • DC Electrical Characteristics @ +37°C (continued)



	Parameter	Sym	Min	Тур	Max	Units	Test Conditions	
21	Turn-on delay						Defined according to Figure 4-3 on	
	ZL70573/74/88	tond		500	13000	ns	page 4-4. A 200-mA pulse is generated using the shortest possible delay. The time is measured from Vbo – 2 V until the voltage has decreased to 3.5 V.	
	ZL70571	tond		140	4000	ns		
	ZL70572	tond			6000	ns		
22	Maximum voltage during surge						Measured at peak and defined	
	ZL7073/74/88	Vpeak		13	15	V	according to Figure 4-5 on page 4-5.	
	ZL70571	Vpeak		11.5	13	V		
	ZL70572	Vpeak			21.5	V		
23	Immunity to dV/dt t	riggering	Defined according to Figure 4-4 on page 4-4.					
	ZL70073/74/88	dV/dt	1000	> 2300		V/µs	Measured at 8.0 V	
	ZL70571	dV/dt	100	160		V/µs	Measured at 9 V terminal to terminal and at 8.5 V terminal to substrate	
	ZL70572	dV/dt	100			V/µs	Measured at 17 V terminal to terminal and at 16.5 V terminal to substrate	

Table 4-4 • AC Electrical Characteristics @ +37°C



Figure 4-1 • 10 ms Surge Current Waveform







Figure 4-4 • dV/dt Immunity Test Pulse



**dV/dt** variable, adjusted to determine the maximum slew rate for which a device does not trigger.

t



Figure 4-5 • Peak Voltage during Surge Definition



## **5 – Quality Assurance Procedures**

Microsemi's QA procedures are based on MIL-PRF-38535. Microsemi maintains traceability records for every chip to the wafer lot and wafer level. Each wafer lot is subjected to a Lot Acceptance Test (LAT). The devices are assembled to a ceramic test substrate and subjected a 168-hour burn-in test at +125°C, or equivalent. Wafer lots acceptance requires all LAT devices must pass the pre- and post-burn-in electrical tests. A certification of compliance (C of C) is included with each shipment.

Additional details/information are available upon request from Microsemi.



## 6 – Additional Information

### **Evaluation Boards**

For bench evaluation purposes, Microsemi offers the surge protection devices mounted on ceramic substrate. Each surge protection device terminal and substrate terminal (if present) is accessible by two through hole solder pins attached to either side of the test substrate. Ordering information is listed in Table 6-1 below. Evaluation boards are for testing and evaluation purposes only and are not for use in implanted devices.

Surge Protection Device Part Number	Evaluation Board Part Number	Evaluation Board Description
ZL70571UDJ	ZLE70571MAD	Eval Board, Surge Protection, ZL70571
ZL70572UDJ	ZLE70572MAD	Eval Board, Surge Protection, ZL70572
ZL70573UDJ	ZLE70573MAD	Eval Board, Surge Protection, ZL70573
ZL70574UDJ	ZLE70574MAD	Eval Board, Surge Protection, ZL70574
ZL70588UBJ	ZLE70588MAD	Eval Board, Surge Protection, ZL70588

Table 6-1 • Evaluation Board, Cross-Reference

## **Flip Chip Processing Recommendations**

The surge protection devices described in this document (with the exception of ZL70588) are designed for flip chip assembly. The face or active surface of the chip is covered with small tin/lead solder bumps designed to connect to solder pads on the surface of a circuit board via reflow soldering. For best results, an underfill should be added to fill in the gap between the die and circuit board pad pattern for these devices. However, there are two approaches to consider when designing the circuit board pad pattern. One method is too layout a pattern of individual pads matched to each solder bump. A second method is to design a pattern of rectangular pads large enough to connect all of the pads for a single terminal. No matter the method used, all of the solder bumps associated with an individual terminal must be connected together via the circuit board (refer to Figure 2-2 on page 2-2 and Figure 2-3 on page 2-3). Likewise, in the case of ZL70571/72, all of the SUB1 and SUB2 solder bumps must also be connected together (refer to Figure 2-3). If unfamiliar with flip chip processing, Microsemi recommends that the customer seek advice from a consultant or subcontractor familiar with the process.



## 7 – Mechanical Data

### Mechanical Data — ZL70573



Figure 7-1 • Die Size and Bump Placement of ZL70573

## Mechanical Data — ZL70574



Figure 7-2 • Die Size and Bump Placement of ZL70574

## Mechanical Data — ZL70571 and ZL70572



Figure 7-3 • Die Size and Bump Placement of ZL70571 and ZL70572

## Mechanical Data — Solder Bumps ZL70571/72/73/74





## Mechanical Data — ZL70588



Figure 7-5 • Size and Bond Pad Placement of ZL70588



## 8 – Datasheet Information

## **List of Changes**

The following table lists critical changes that were made in the ZL70571/72/73/74/88 Medical Surge Protection Device (Data Sheet) (107092) after September 2008.

Revision	Changes	Page		
Revision 14 (August 2013)	Figure 7-3 was updated to add additional details.	7-3		
Revision 13 (April 2013)	Assigned test number 18 to After Surge Pulse, as the number had been inadvertently omitted and the tests out of order. Subsequent lines (i.e., test numbers) were renumbered appropriately.			
	In Table 4-4, replaced the text in the Test Condition column for line 20, Turn-on delay, to clarify the test method.	4-3		
	Replaced Figure 4-3 with a new drawing. Added a new Figure 4-5 (comprising a portion of the previous Figure 4-3). Changed figure cross-references in Table 4-4 for lines 22 and 23 to reflect the changes to the figures.	4-3, 4-4, 4-5		
Revision 12 (April 2012)	Name change from Zarlink to Microsemi. Included changing document format and chapter structure. Spelling and grammar were also corrected throughout the document.	All		
	Updated bullets for "Applications".	I		
Revision 11 (December 2010)	Complete revamp due to transfer from MHS to Dalsa. There will be no changes electrically.	-		
	Corrected dimensions and tolerances in Figure 7-1.	7-1		
	Corrected dimensions and tolerances in Figure 7-5.	7-4		

## **Datasheet Categories**

### Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

#### **Product Brief**

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

#### Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label will only be used when the data has not been fully characterized.

#### Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Production

This version contains information that is considered to be final.

## Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in an advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi CMPG Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the CMPG Products Group's products is available from Microsemi upon request. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.



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