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FAN7392

High-Current, High- and Low-Side, Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- 3A/3A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- 3.3V Logic Compatible
- Separate Logic Supply (V_{DD}) Range from 3.3V to 20V
- Under-Voltage Lockout for V_{CC} and V_{BS}
- Cycle-by-Cycle Edge-Triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs In-phase with Input Signals
- Available in 14-DIP and 16-SOP (Wide) Packages

Applications

- High-Speed Power MOSFET and IGBT Gate Driver
- Server Power Supply
- Uninterrupted Power Supply (UPS)
- Telecom System Power Supply
- Distributed Power Supply
- Motor Drive Inverter

Description

The FAN7392 is a monolithic high- and low-side gate drive IC, that can drive high-speed MOSFETs and IGBTs that operate up to +600V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction. Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to $V_S = -9.8V$ (typical) for $V_{BS} = 15V$. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The UVLO circuit prevents malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. The high-current and low-output voltage drop feature makes this device suitable for half- and full-bridge inverters, like switching-mode power supply and high-power DC-DC converter applications.

14-PDIP



16-SOP



Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN7392N	-40°C to +125°C	14-PDIP	Tube
FAN7392M		16-SOP	Tube
FAN7392MX			Tape and Reel

Typical Application Diagrams

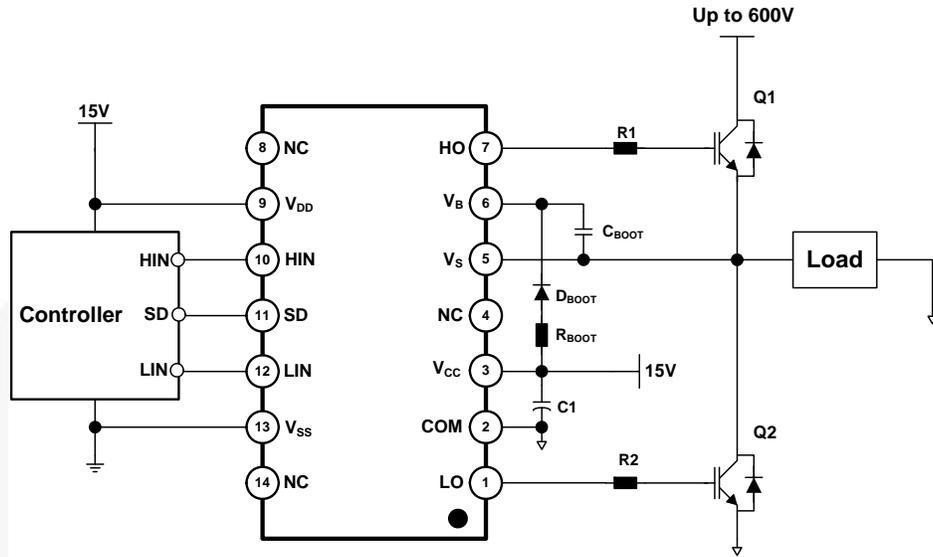


Figure 1. Typical Application Circuit (Referenced 14-DIP)

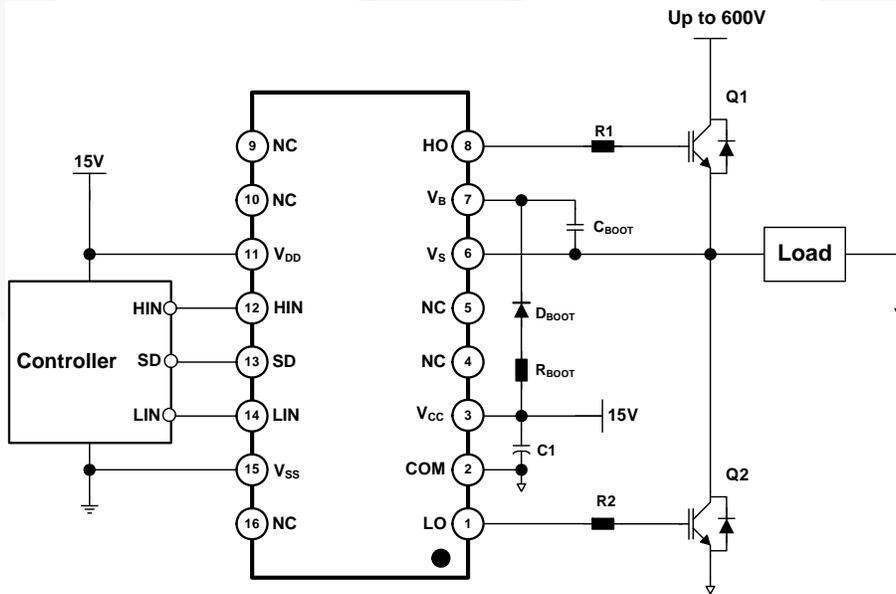


Figure 2. Typical Application Circuit (Referenced 16-SOP)

Pin Configuration

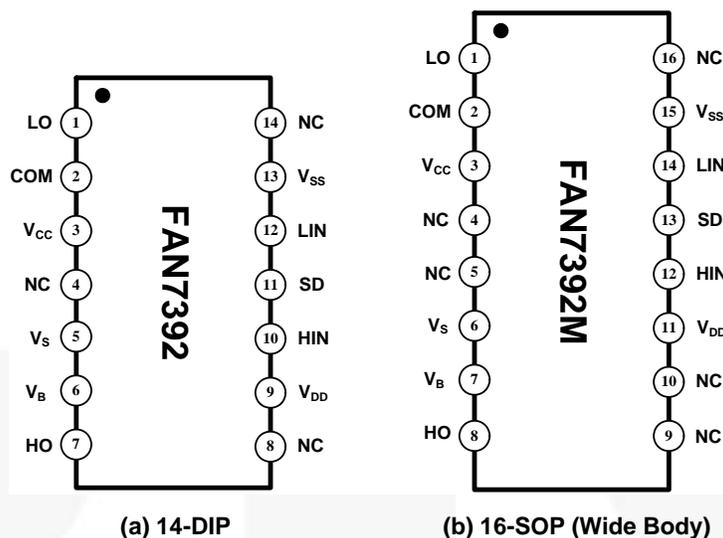


Figure 5. Pin Configurations (Top View)

Pin Definitions

14-Pin	16-Pin	Name	Description
1	1	LO	Low-Side Driver Output
2	2	COM	Low-Side Return
3	3	V _{CC}	Low-Side Supply Voltage
5	6	V _S	High-Voltage Floating Supply Return
6	7	V _B	High-Side Floating Supply
7	8	HO	High-Side Driver Output
9	11	V _{DD}	Logic Supply Voltage
10	12	HIN	Logic Input for High-Side Gate Driver Output
11	13	SD	Logic Input for Shutdown Function
12	14	LIN	Logic Input for Low-Side Gate Driver Output
13	15	V _{SS}	Logic Ground
4,8,14	4, 5, 9, 10, 16	NC	No Connect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	-0.3	625.0	V
V_S	High-Side Floating Offset Voltage	$V_B-25.0$	$V_B+0.3$	V
V_{HO}	High-Side Floating Output Voltage	$V_S-0.3$	$V_B+0.3$	V
V_{CC}	Low-Side Supply Voltage	-0.3	25.0	V
V_{LO}	Low-Side Floating Output Voltage	-0.3	$V_{CC}+0.3$	V
V_{DD}	Logic Supply Voltage	-0.3	$V_{SS}+25.0$	V
V_{SS}	Logic Supply Offset Voltage	$V_{CC}-25.0$	$V_{CC}+0.3$	V
V_{IN}	Logic Input Voltage (HIN, LIN and SD)	$V_{SS}-0.3$	$V_{DD}+0.3$	V
dV_S/dt	Allowable Offset Voltage Slew Rate		± 50	V/ns
P_D	Power Dissipation ^(1, 2, 3)	14-PDIP	1.6	W
		16-SOP	1.3	
θ_{JA}	Thermal Resistance	14-PDIP	75	$^{\circ}\text{C/W}$
		16-SOP	95	
T_J	Maximum Junction Temperature		+150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-55	+150	$^{\circ}\text{C}$

Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
 JESD51-2: Integral circuits thermal test method environmental conditions, natural convection; and
 JESD51-3: Low effective thermal conductivity test board for leaded surface-mount packages.
- Do not exceed power dissipation (P_D) under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_B	High-Side Floating Supply Voltage	V_S+10	V_S+20	V
V_S	High-Side Floating Supply Offset Voltage	$6-V_{CC}$	600	V
V_{HO}	High-Side Output Voltage	V_S	V_B	V
V_{CC}	Low-Side Supply Voltage	10	20	V
V_{LO}	Low-Side Output Voltage	0	V_{CC}	V
V_{DD}	Logic Supply Voltage	$V_{SS}+3$	$V_{SS}+20$	V
V_{SS}	Logic Supply Offset Voltage	-5	5	V
V_{IN}	Logic Input Voltage	V_{SS}	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	$^{\circ}\text{C}$

Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS}, V_{DD})=15.0V$, $V_{SS}=COM=0V$ and $T_A=25^\circ C$, unless otherwise specified. The V_{IH} , V_{IL} , and I_{IN} parameters are referenced to V_{SS} and are applicable to the respective input leads: HIN, LIN, and SD. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective output leads: HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
Low-Side Power Supply Section						
I_{QCC}	Quiescent V_{CC} Supply Current	$V_{IN}=0V$ or V_{DD}		40	80	μA
I_{QDD}	Quiescent V_{DD} Supply Current	$V_{IN}=0V$ or V_{DD}			10	μA
I_{PCC}	Operating V_{CC} Supply Current	$f_{IN}=20kHz$, rms, $V_{IN}=15V_{PP}$		430		μA
I_{PDD}	Operating V_{DD} Supply Current	$f_{IN}=20kHz$, rms, $V_{IN}=15V_{PP}$		300		μA
I_{SD}	Shutdown Supply Current	$S_D=V_{DD}$		120		μA
V_{CCUV+}	V_{CC} Supply Under-Voltage Positive-Going Threshold Voltage	$V_{IN}=0V$, $V_{CC}=\text{Sweep}$	7.7	8.8	9.9	V
V_{CCUV-}	V_{CC} Supply Under-Voltage Negative-Going Threshold Voltage	$V_{IN}=0V$, $V_{CC}=\text{Sweep}$	7.3	8.4	9.5	V
V_{CCUVH}	V_{CC} Supply Under-Voltage Lockout Hysteresis Voltage	$V_{IN}=0V$, $V_{CC}=\text{Sweep}$		0.4		V
Bootstrapped Supply Section						
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{IN}=0V$ or V_{DD}		60	130	μA
I_{PBS}	Operating V_{BS} Supply Current	$f_{IN}=20kHz$, rms value		500		μA
V_{BSUV+}	V_{BS} Supply Under-Voltage Positive-Going Threshold Voltage	$V_{IN}=0V$, $V_{BS}=\text{Sweep}$	7.7	8.8	9.9	V
V_{BSUV-}	V_{BS} Supply Under-Voltage Negative-Going Threshold Voltage	$V_{IN}=0V$, $V_{BS}=\text{Sweep}$	7.3	8.4	9.5	V
V_{BSUVH}	V_{BS} Supply Under-Voltage Lockout Hysteresis Voltage	$V_{IN}=0V$, $V_{BS}=\text{Sweep}$		0.4		V
I_{LK}	Offset Supply Leakage Current	$V_B=V_S=600V$			50	μA
Input Logic Section (HIN, LIN, and SD)						
V_{IH}	Logic "1" Input Threshold Voltage	$V_{DD}=3V$	2.4			V
		$V_{DD}=15V$	9.5			V
V_{IL}	Logic "0" Input Threshold Voltage	$V_{DD}=3V$			0.8	V
		$V_{DD}=15V$			4.5	V
I_{IN+}	Logic Input High Bias Current	$V_{IN}=V_{DD}$		20	40	μA
I_{IN-}	Logic Input Low Bias Current	$V_{IN}=0V$			3	μA
R_{IN}	Logic Input Pull-Down Resistance		375	750		$K\Omega$
Gate Driver Output Section						
V_{OH}	High-Level Output Voltage ($V_{BIAS} - V_O$)	No Load ($I_O=0A$)			1.5	V
V_{OL}	Low-Level Output Voltage	No Load ($I_O=0A$)			200	mV
I_{O+}	Output High, Short-Circuit Pulsed Current ⁽⁴⁾	$V_O=0V$, $PW \leq 10\mu s$	2.5	3.0		A
I_{O-}	Output Low, Short-Circuit Pulsed Current ⁽⁴⁾	$V_O=15V$, $PW \leq 10\mu s$	2.5	3.0		A
V_{SS}/COM	$V_{SS}-COM/COM-V_{SS}$ Voltage Endurability		-5.0		5.0	V
$-V_S$	Allowable Negative V_S Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V

Dynamic Electrical Characteristics

$V_{BIAS}(V_{CC}, V_{BS}, V_{DD})=15.0V$, $V_{SS}=COM=0V$, $C_{LOAD}=1000pF$, $T_A=25^{\circ}C$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-On Propagation Delay Time	$V_S=0V$		130	180	ns
t_{off}	Turn-Off Propagation Delay Time	$V_S=0V$		150	200	ns
t_{sd}	Shutdown propagation Delay Time ⁽⁴⁾			130	180	ns
t_r	Turn-On Rise Time			25	50	ns
t_f	Turn-Off Fall Time			20	45	ns
MT	Delay Matching, HO & LO Turn-On/Off				35	ns

Note:

4. These parameters guaranteed by design.

Typical Characteristics

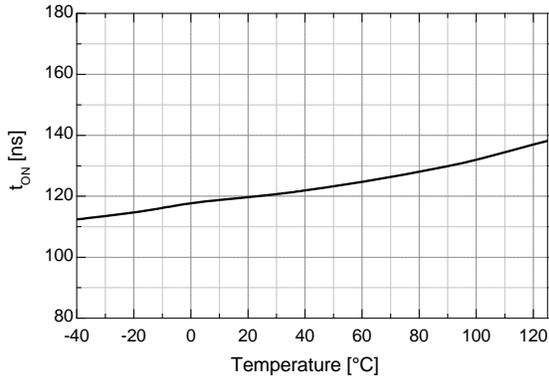


Figure 6. Turn-On Propagation Delay vs. Temperature

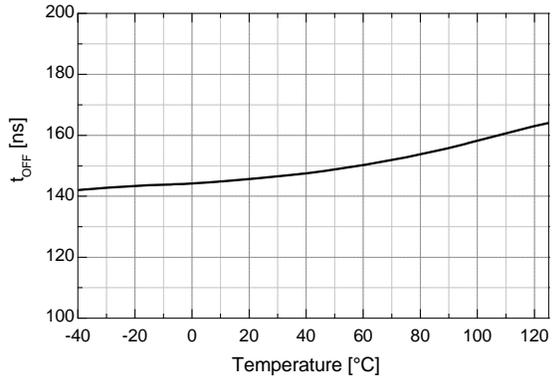


Figure 7. Turn-Off Propagation Delay vs. Temperature

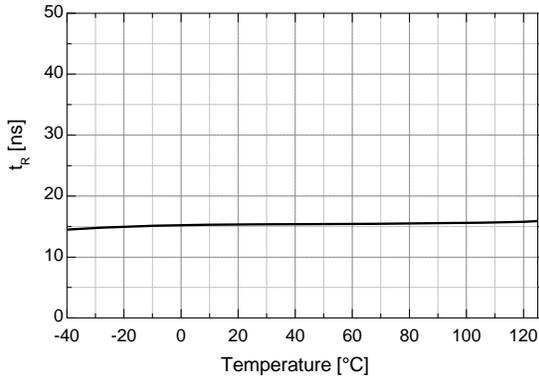


Figure 8. Turn-On Rise Time vs. Temperature

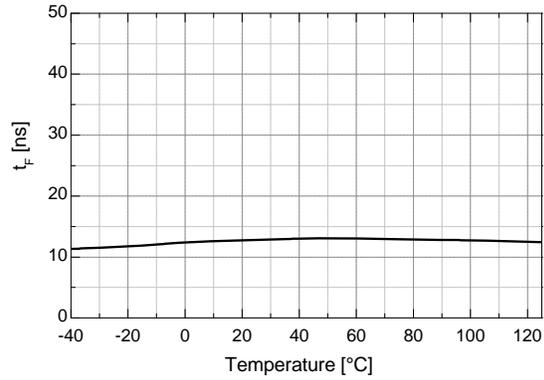


Figure 9. Turn-Off Fall Time vs. Temperature

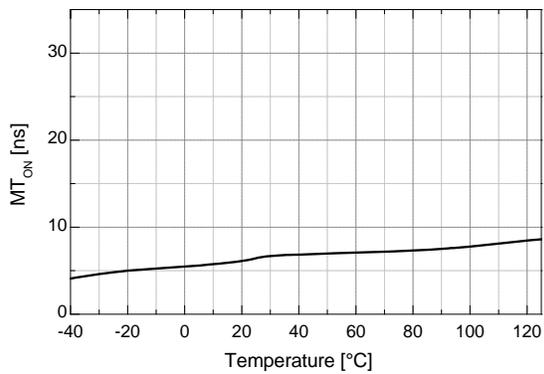


Figure 10. Turn-On Delay Matching vs. Temperature

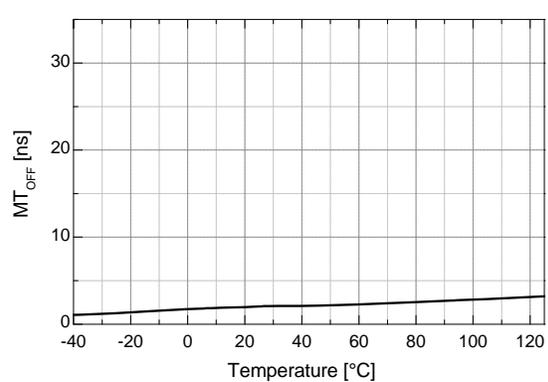


Figure 11. Turn-Off Delay Matching vs. Temperature

Typical Characteristics (Continued)

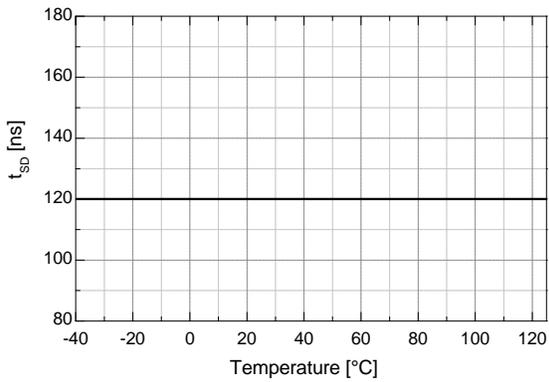


Figure 12. Shutdown Propagation Delay vs. Temperature

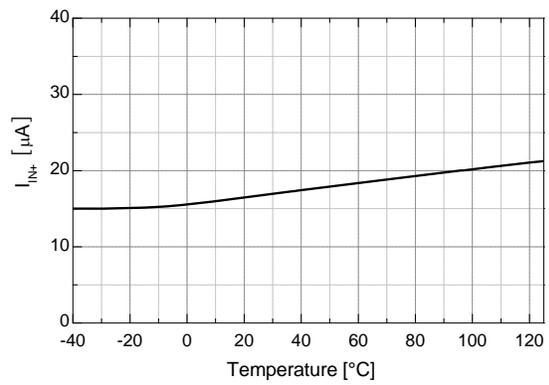


Figure 13. Logic Input High Bias Current vs. Temperature

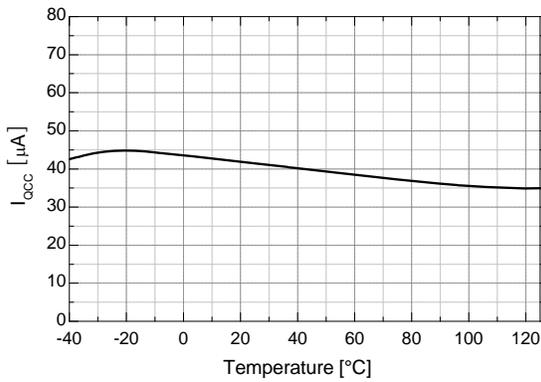


Figure 14. Quiescent V_{CC} Supply Current vs. Temperature

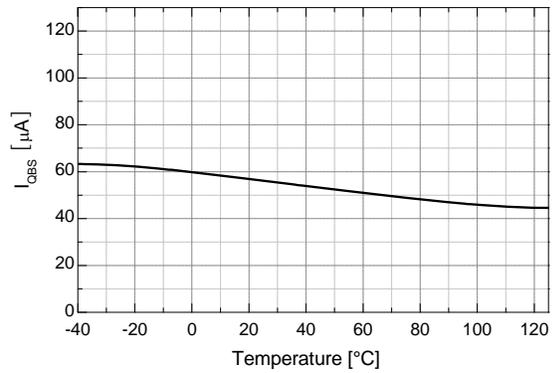


Figure 15. Quiescent V_{BS} Supply Current vs. Temperature

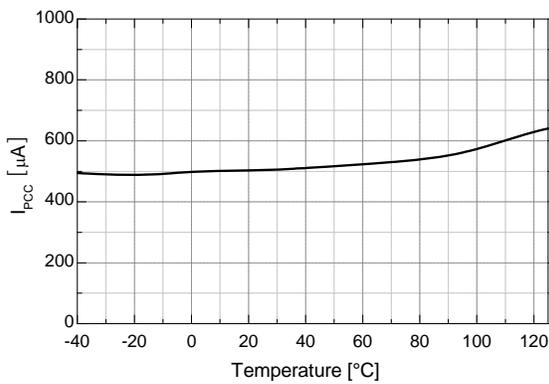


Figure 16. Operating V_{CC} Supply Current vs. Temperature

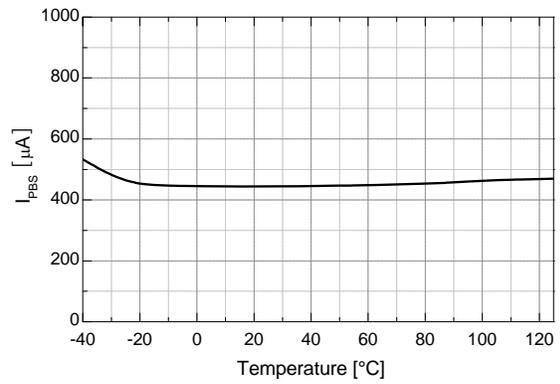


Figure 17. Operating V_{BS} Supply Current vs. Temperature

Typical Characteristics (Continued)

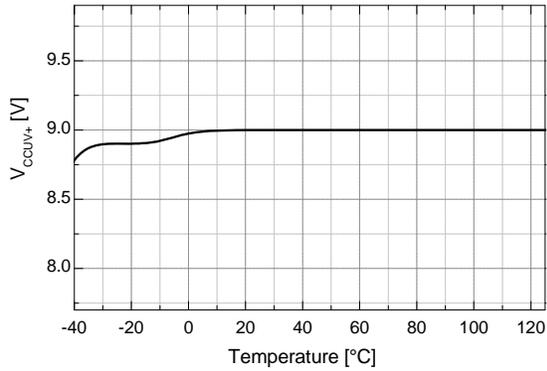


Figure 18. V_{CC} UVLO+ vs. Temperature

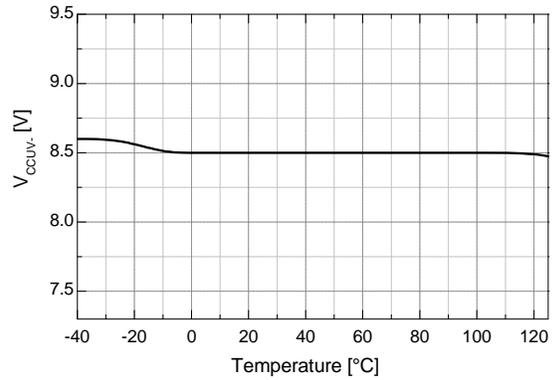


Figure 19. V_{CC} UVLO- vs. Temperature

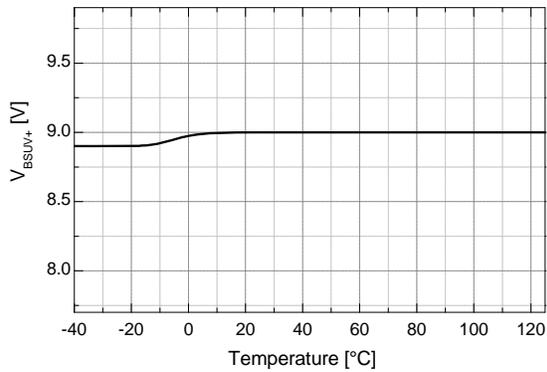


Figure 20. V_{BS} UVLO+ vs. Temperature

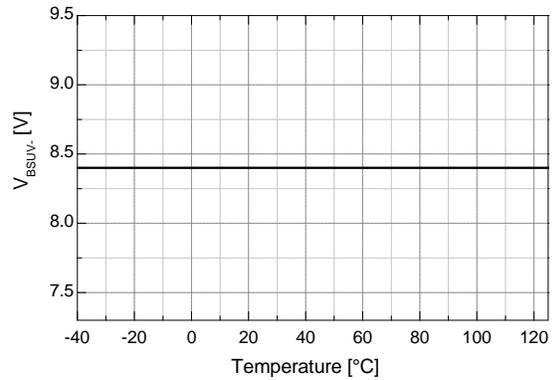


Figure 21. V_{BS} UVLO- vs. Temperature

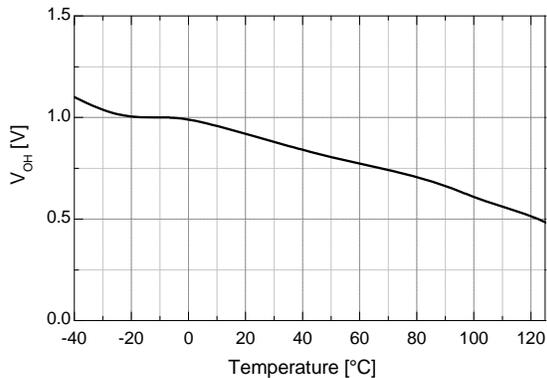


Figure 22. High-Level Output Voltage vs. Temperature

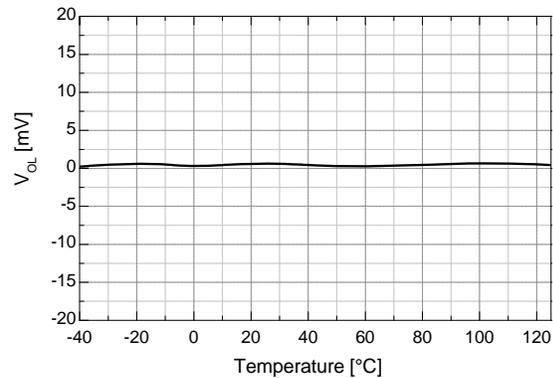


Figure 23. Low-Level Output Voltage vs. Temperature

Typical Characteristics (Continued)

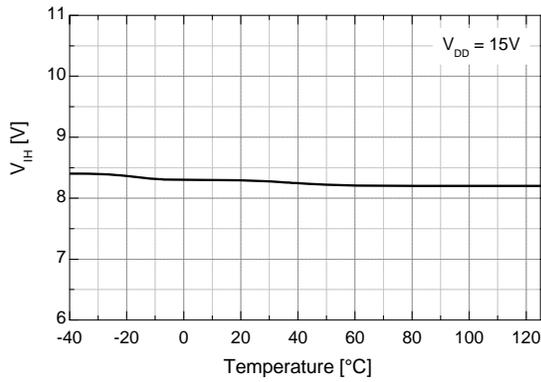


Figure 24. Logic High Input Voltage vs. Temperature

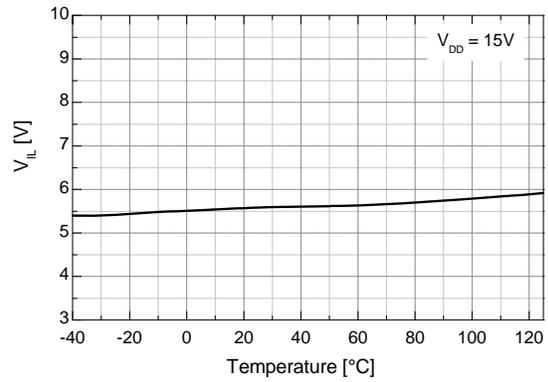


Figure 25. Logic Low Input Voltage vs. Temperature

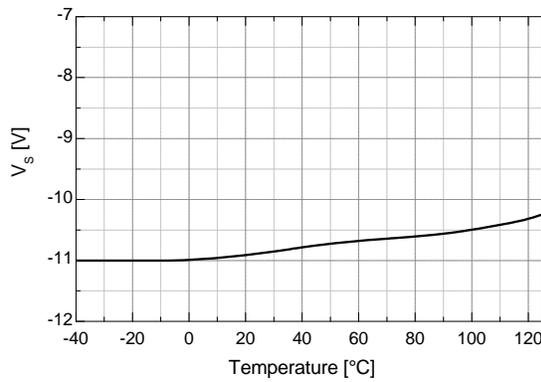


Figure 26. Allowable Negative V_S Voltage vs. Temperature

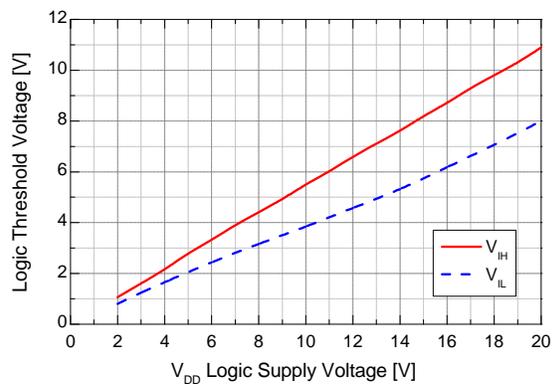


Figure 27. Input Logic (HIN & LIN) Threshold Voltage vs. V_{DD} Supply Voltage

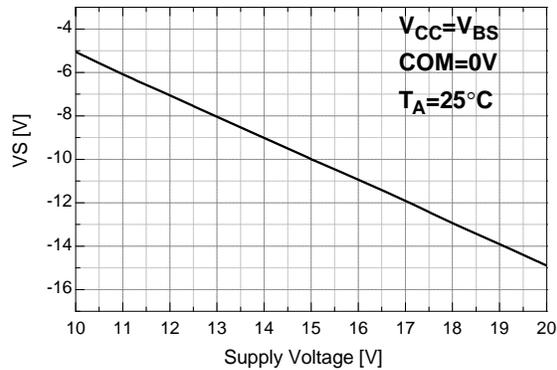


Figure 28. Allowable Negative V_S Voltage for HIN Signal Propagation to High Side vs. Supply Voltage

Switching Time Definitions

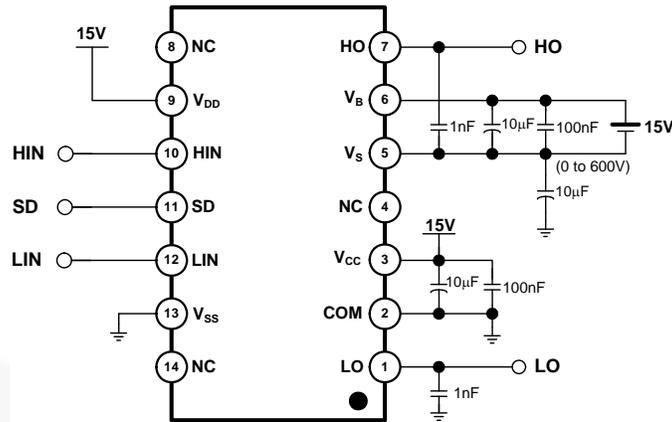


Figure 29. Switching Time Test Circuit (Referenced 14-DIP)

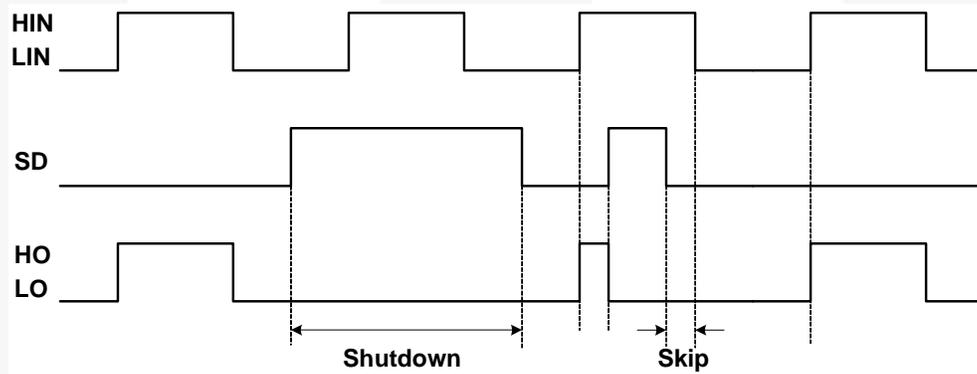


Figure 30. Input/Output Timing Diagram

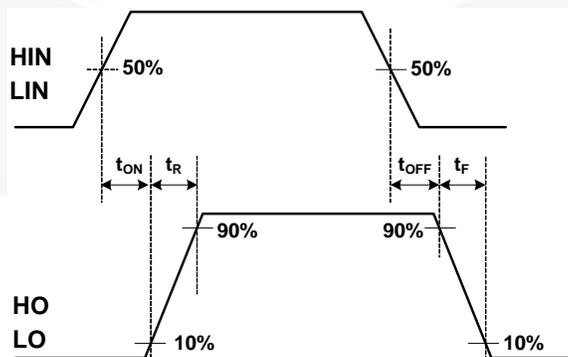


Figure 31. Switching Time Waveform Definitions

Switching Time Definitions (Continued)

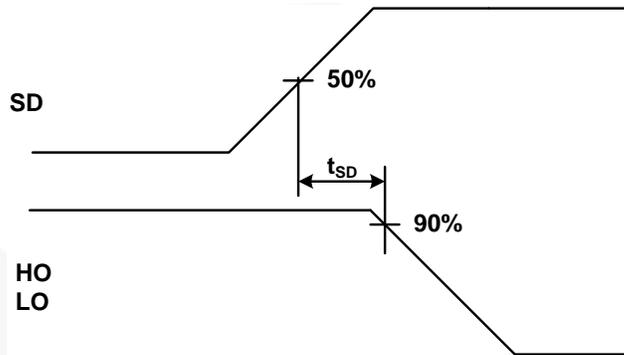


Figure 32. Shutdown Waveform Definition

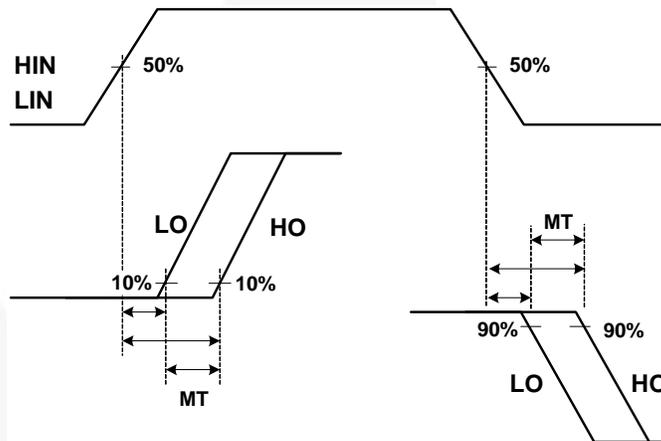


Figure 33. Delay Matching Waveform Definitions

Application Information

Negative V_S Transient

The bootstrap circuit has the advantage of being simple and low cost, but has some limitations. The biggest difficulty with this circuit is the negative voltage present at the emitter of the high-side switching device when high-side switch is turned-off in half-bridge application.

If the high-side switch, Q1, turns-off while the load current is flowing to an inductive load, a current commutation occurs from high-side switch, Q1, to the diode, D2, in parallel with the low-side switch of the same inverter leg. Then the negative voltage present at the emitter of the high-side switching device, just before the freewheeling diode, D2, starts clamping, causes load current to suddenly flow to the low-side freewheeling diode, D2, as shown in Figure 34.

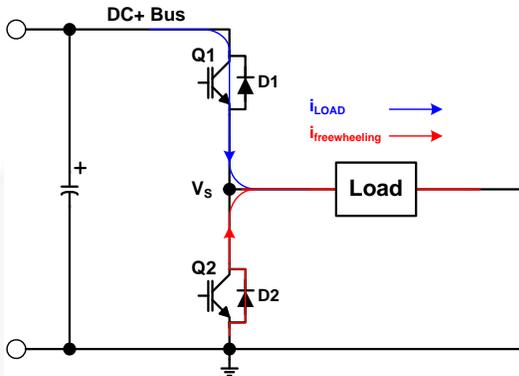


Figure 34. Half-Bridge Application Circuits

This negative voltage can be trouble for the gate driver's output stage, there is the possibility to develop an over-voltage condition of the bootstrap capacitor, input signal missing and latch-up problems because it directly affects the source V_S pin of the gate driver, as shown in Figure 35. This undershoot voltage is called "negative V_S transient".

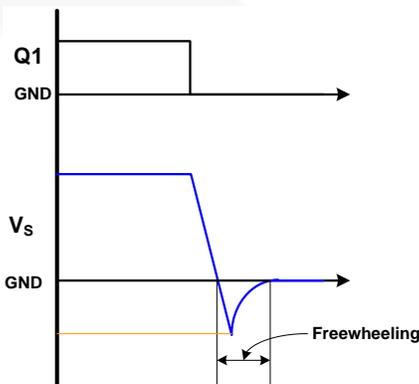


Figure 35. V_S Waveforms During Q1 Turn-Off

Figure 36 and Figure 37 show the commutation of the load current between high-side switch, Q1, and low-side freewheeling diode, D3, in same inverter leg. The parasitic inductances in the inverter circuit from the die wire bonding to the PCB tracks are jumped together in L_C and L_E for each IGBT. When the high-side switch, Q1, and low-side switch, Q4, are turned on, the V_{S1} node is below DC+ voltage by the voltage drops associated with the power switch and the parasitic inductances of the circuit due to load current is flows from Q1 and Q4, as shown in Figure 36. When the high-side switch, Q1, is turned off and Q4, remained turned on, the load current to flows the low-side freewheeling diode, D3, due to the inductive load connected to V_{S1} as shown in Figure 37. The current flows from ground (which is connected to the COM pin of the gate driver) to the load and the negative voltage present at the emitter of the high-side switching device.

In this case, the COM pin of the gate driver is at a higher potential than the V_S pin due to the voltage drops associated with freewheeling diode, D3, and parasitic elements, L_{C3} and L_{E3} .

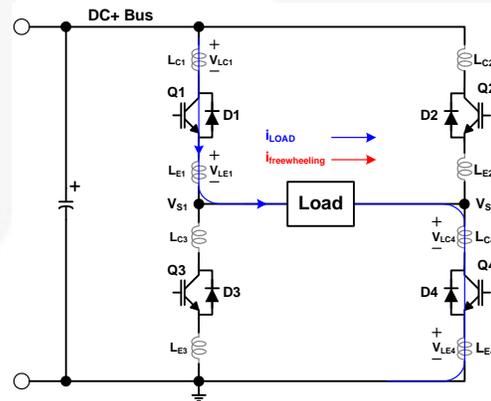


Figure 36. Q1 and Q4 Turn-On

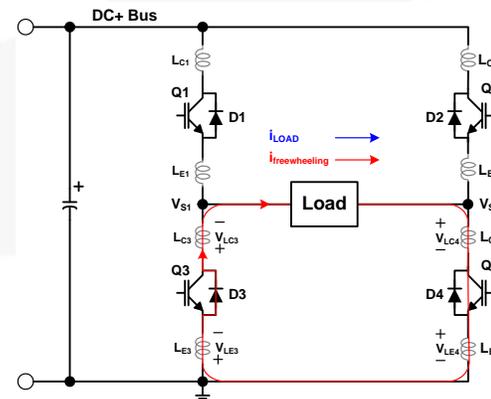


Figure 37. Q1 Turn-Off and D3 Conducting

The FAN7392 has a negative V_S transient performance curve, as shown in Figure 38.

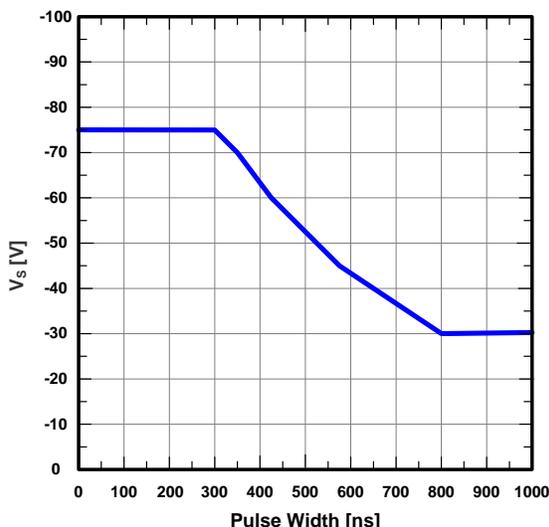


Figure 38. Negative V_S Transient Characteristic

Even though the FAN7392 has been shown able to handle these negative V_S transient conditions, it is strongly recommended that the circuit designer limit the negative V_S transient as much as possible by careful PCB layout to minimize the value of parasitic elements and component use. The amplitude of negative V_S voltage is proportional to the parasitic inductances and the turn-off speed, di/dt , of the switching device.

General Guidelines

Printed Circuit Board Layout

The layout recommended for minimized parasitic elements is as follows:

- Direct tracks between switches with no loops or deviation.
- Avoid interconnect links. These can add significant inductance.
- Reduce the effect of lead-inductance by lowering package height above the PCB.
- Consider co-locating both power switches to reduce track length.
- To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.
- To reduce the EM coupling and improve the power switch turn-on/off performance, the gate drive loops must be reduced as much as possible.

Placement of Components

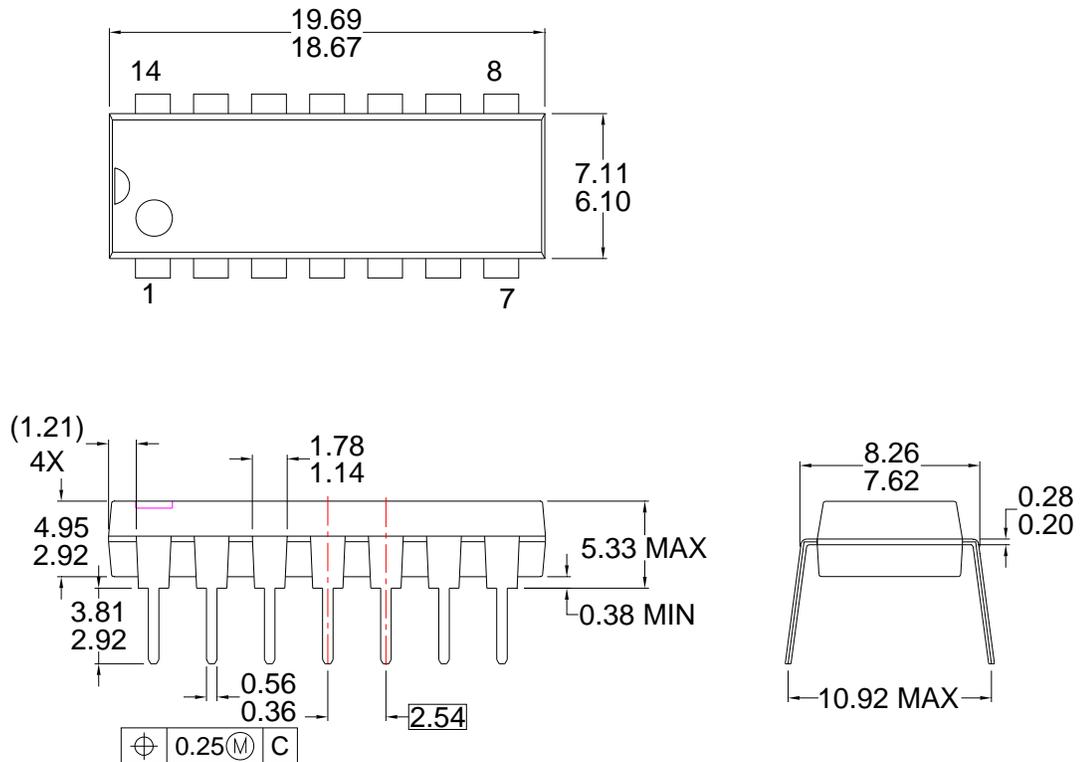
The recommended placement and selection of component as follows:

- Place a bypass capacitor between the V_{DD} and V_{SS} pins. A ceramic $1\mu\text{F}$ capacitor is suitable for most applications. This component should be placed as close as possible to the pins to reduce parasitic elements.
- The bypass capacitor from V_{CC} to COM supports both the low-side driver and bootstrap capacitor recharge. A value at least ten times higher than the bootstrap capacitor is recommended.
- The bootstrap resistor, R_{BOOT} , must be considered in sizing the bootstrap resistance and the current developed during initial bootstrap charge. If the resistor is needed in series with the bootstrap diode, verify that V_B does not fall below COM (ground). Recommended use is typically $5 \sim 10\Omega$ that increase the V_{BS} time constant. If the voltage drop of bootstrap resistor and diode is too high or the circuit topology does not allow a sufficient charging time, a fast recovery or ultra-fast recovery diode can be used.
- The bootstrap capacitor, C_{BOOT} , uses a low-ESR capacitor, such as ceramic capacitor.

It is strongly recommended that the placement of components is as follows:

- Place components tied to the floating voltage pins (V_B and V_S) near the respective high-voltage portions of the device and the FAN7392. NC (not connected) pins in this package maximize the distance between the high-voltage and low-voltage pins (see Figure 5).
- Place and route for bypass capacitors and gate resistors as close as possible to gate drive IC.
- Locate the bootstrap diode, D_{BOOT} , as close as possible to bootstrap capacitor, C_{BOOT} .
- The bootstrap diode must use a lower forward voltage drop and minimal switching time as soon as possible for fast recovery or ultra-fast diode.

Physical Dimensions



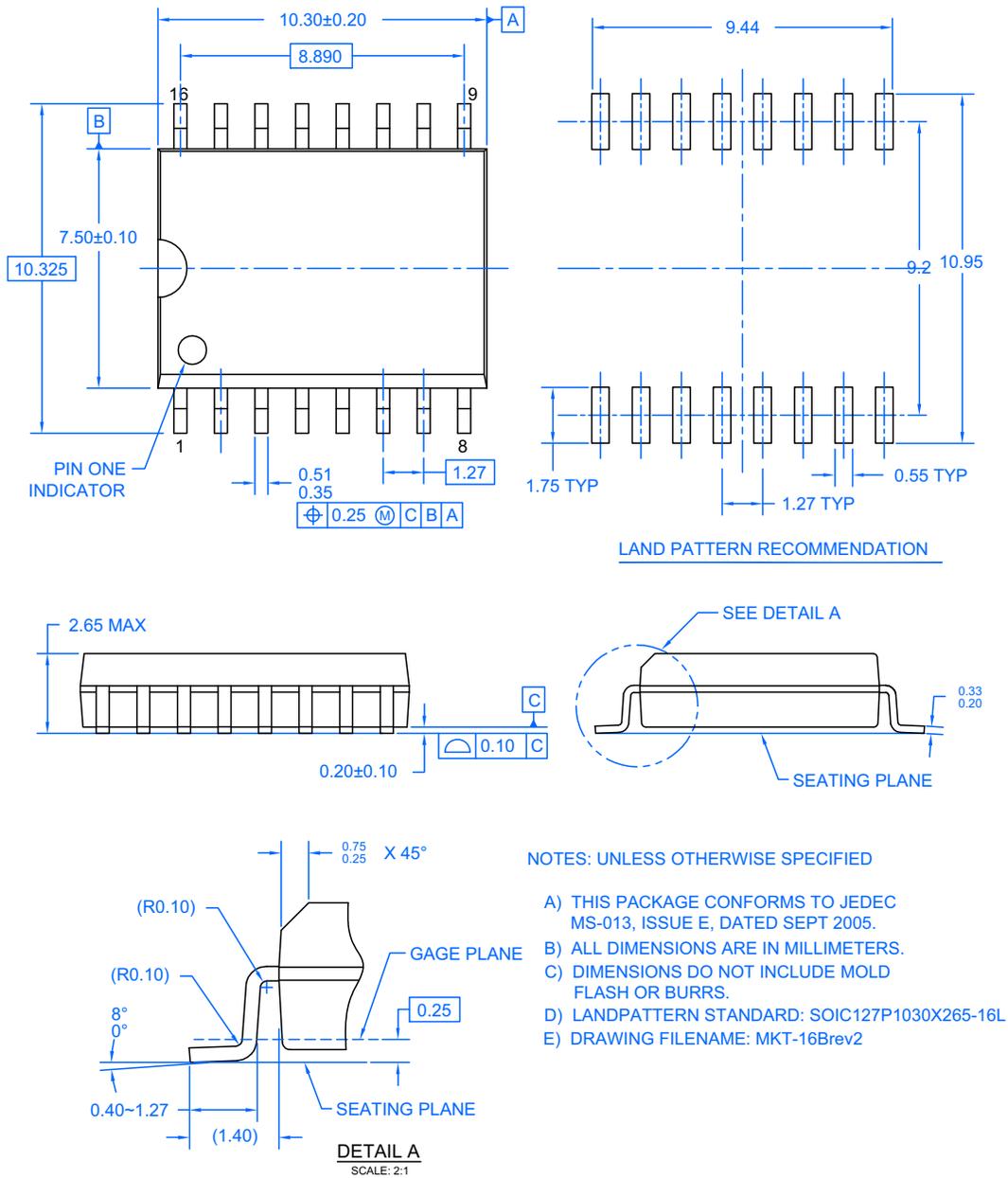
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Figure 39. 14-Lead Dual In-Line Package (DIP)

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Physical Dimensions (Continued)



M16BREV2

Figure 40. 16-Lead Small Outline Package (SOP)

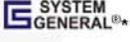
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