Document Number: MMRF1316N
Rev. 0, 7/2014

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This high ruggedness device is designed for use in high VSWR military, aerospace and defense, radar and radio communications applications. It is an unmatched input and output design allowing wide frequency range utilization, between 1.8 and 600 MHz.

Typical Performance: V_{DD} = 50 Vdc

Frequency (MHz)	Signal Type	P_{out} (W)	G_{ps} (dB)	η_D (%)
87.5-108 (1,3)	CW	361	23.8	80.1
230 (2)	CW	300	25.0	70.0
230 (2)	Pulse (100 μsec, 20% Duty Cycle)	300 Peak	27.0	71.0

Load Mismatch/Ruggedness

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage	Result
98 (1)	CW	> 65:1 at all Phase Angles	3 (3 dB Overdrive)	50	No Device Degradation
230 (2)	Pulse (100 μsec, 20% Duty Cycle)		1.16 Peak (3 dB Overdrive)		

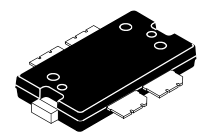
1. Measured in 87.5–108 MHz broadband reference circuit.
2. Measured in 230 MHz narrowband test circuit.
3. The values shown are the minimum measured performance numbers across the indicated frequency range.

Features

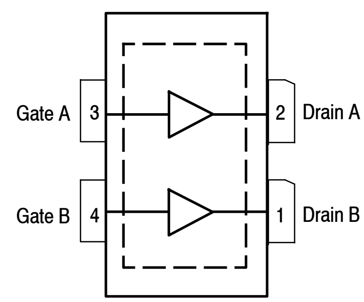
- Wide Operating Frequency Range
- Extreme Ruggedness
- Unmatched Input and Output Allowing Wide Frequency Range Utilization
- Integrated Stability Enhancements
- Low Thermal Resistance
- Integrated ESD Protection Circuitry
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel.

MMRF1316NR1

1.8–600 MHz, 300 W CW, 50 V
WIDEBAND
RF POWER LDMOS TRANSISTOR



TO-270WB-4
PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +133	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	909 4.55	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case CW: Case Temperature 81°C, 305 W CW, 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, 230 MHz	$R_{\theta JC}$	0.22	°C/W
Thermal Impedance, Junction to Case Pulse: Case Temperature 59°C, 300 W Peak, 100 μsec Pulse Width, 20% Duty Cycle, 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, 230 MHz	$Z_{\theta JC}$	0.034	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2, passes 2500 V
Machine Model (per EIA/JESD22-A115)	A, passes 150 V
Charge Device Model (per JESD22-C101)	IV, passes 2000 V

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
Drain-Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 50 mA)	$V_{(BR)DSS}$	133	140	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 960 μAdc)	$V_{GS(th)}$	1.8	2.3	2.8	Vdc
Gate Quiescent Voltage (V_{DD} = 50 Vdc, I_D = 100 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.2	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.26	—	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Each side of device measured separately.

(continued)

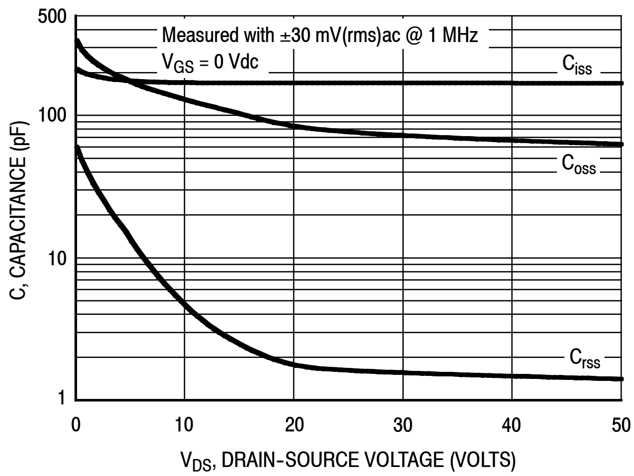
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.4	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	63	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	168	—	pF
Functional Tests (2) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, P_{out} = 300 W Peak (60 W Avg.), f = 230 MHz, 100 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	26.0	27.0	28.5	dB
Drain Efficiency	η_D	69.0	71.0	—	%
Input Return Loss	IRL	—	–20	–9	dB

Table 6. Load Mismatch/Ruggedness (In Freescale Test Fixture, 50 ohm system) $I_{DQ(A+B)}$ = 100 mA

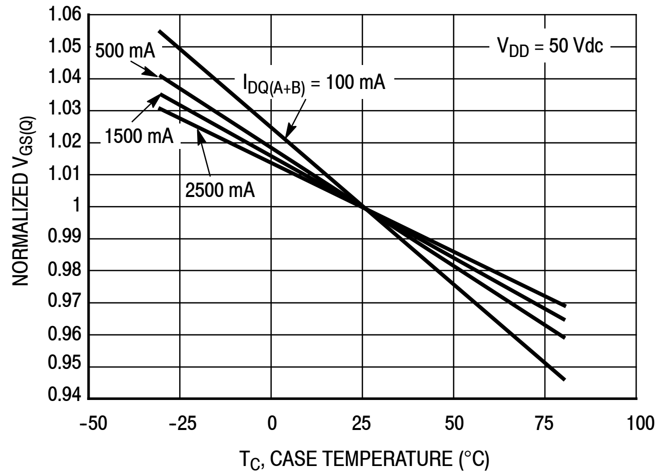
Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
230	Pulse (100 μsec, 20% Duty Cycle)	> 65:1 at all Phase Angles	1.16 Peak (3 dB Overdrive)	50	No Device Degradation

1. Each side of device measured separately.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.



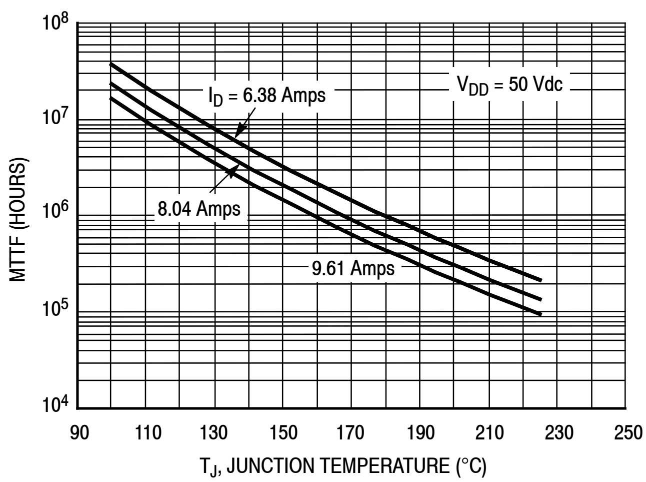
Note: Each side of device measured separately.

Figure 2. Capacitance versus Drain-Source Voltage



I_{DQ} (mA)	Slope (mV/°C)
100	–2.651
500	–2.158
1500	–1.977
2500	–1.787

Figure 3. Normalized V_{GS} versus Quiescent Current and Case Temperature



Note: MTTF value represents the total cumulative operating time under indicated test conditions.

MTTF calculator available at http:/www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 4. MTTF versus Junction Temperature - CW

230 MHz NARROWBAND PRODUCTION TEST FIXTURE

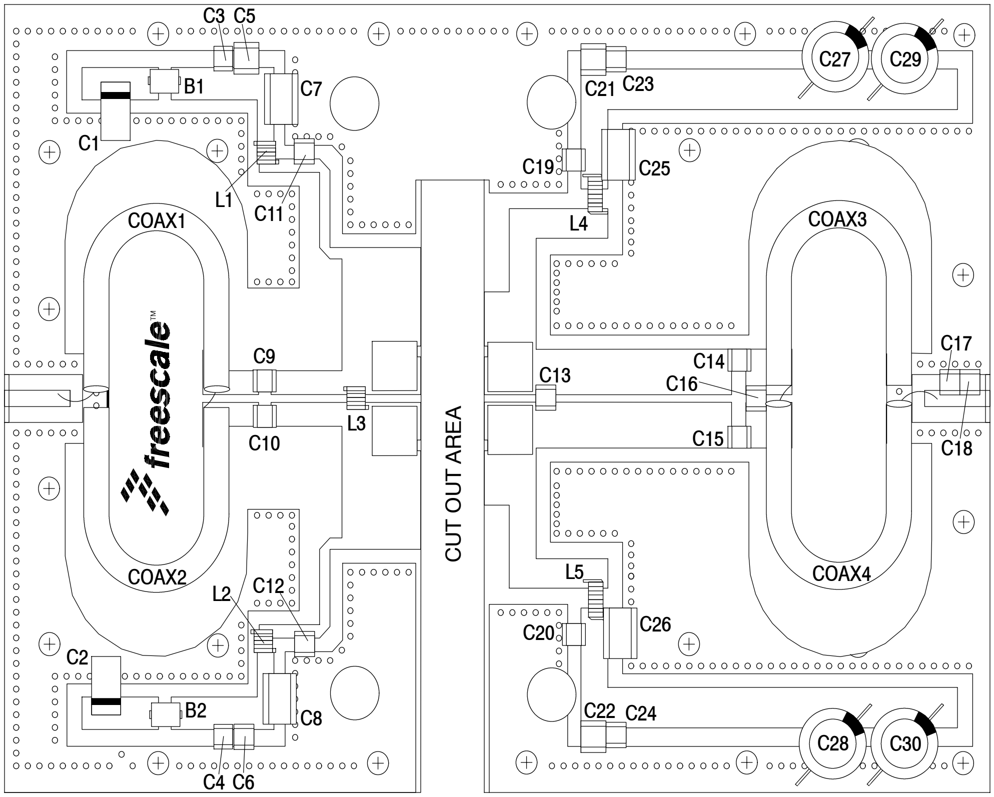


Figure 5. MMRF1316NR1 Narrowband Test Circuit Component Layout — 230 MHz

Table 7. MMRF1316NR1 Narrowband Test Circuit Component Designations and Values — 230 MHz

Part	Description	Part Number	Manufacturer
B1, B2	Small Ferrite Beads, Surface Mount	2743019447	Fair-Rite
C1, C2	22 μF, 35 V Tantulum Capacitors	T491X226K035AT	Kemet
C3, C4	0.1 μF Chip Capacitors	CDR33BX104AKWS	AVX
C5, C6	220 nF Chip Capacitors	C1812C224K5RACTU	Kemet
C7, C8	2.2 μF Chip Capacitors	C1825C225J5RACTU	Kemet
C9, C10, C11, C12	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C13	75 pF Chip Capacitor	ATC100B750JT500XT	ATC
C14, C15	680 pF Chip Capacitors	ATC100B681JT200XT	ATC
C16	82 pF Chip Capacitor	ATC100B820JT500XT	ATC
C17	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C18	11 pF Chip Capacitor	ATC100B110JT500XT	ATC
C19, C20	240 pF Chip Capacitors	ATC100B241JT200XT	ATC
C21, C22	0.10 μF Chip Capacitors	C1812F104K1RACTU	Kemet
C23, C24	0.1 μF Chip Capacitors	CDR33BX104AKWS	AVX
C25, C26	2.2 μF Chip Capacitors	2225X7R225KJT3AB	ATC
C27, C28, C29, C30	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
Coax1, 2, 3, 4	25 Ω Semi Rigid Coax, 2.4″	UT-141C-25	Micro-Coax
L1, L2	12 nH Inductors, 3 Turns	GA3094-ALC	Coilcraft
L3	22 nH Inductor	1812SMS-22NJLC	Coilcraft
L4, L5	17.5 nH Inductors, 4 Turns	GA3095-ALC	Coilcraft
PCB	Arlon AD255A 0.030″, ε_r = 2.55	D49840	MTL

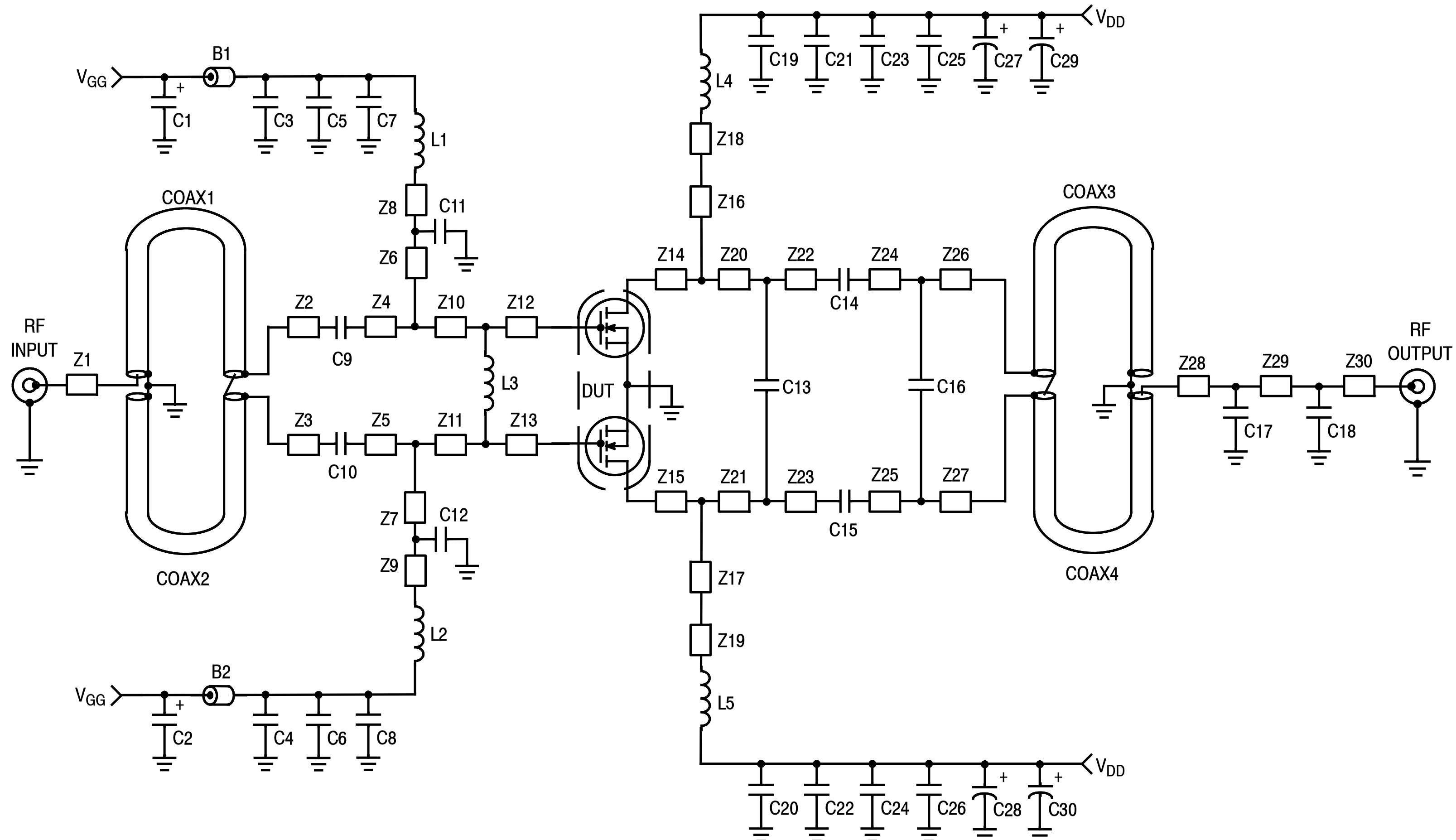


Figure 6. MMRF1316NR1 Narrowband Test Circuit Schematic — 230 MHz

Table 8. MMRF1316NR1 Narrowband Test Circuit Microstrips — 230 MHz

Microstrip	Description	Microstrip	Description	Microstrip	Description
Z1	0.366″ × 0.082″ Microstrip	Z12, Z13	0.361″ × 0.746″ Microstrip	Z24, Z25	0.057″ × 0.230″ Microstrip
Z2, Z3	0.169″ × 0.120″ Microstrip	Z14, Z15	0.289″ × 0.522″ Microstrip	Z26, Z27	0.199″ × 0.230″ Microstrip
Z4, Z5	0.432″ × 0.120″ Microstrip	Z16, Z17	0.347″ × 0.150″ Microstrip	Z28	0.155″ × 0.082″ Microstrip
Z6*, Z7*	0.655″ × 0.058″ Microstrip	Z18, Z19	0.329″ × 0.150″ Microstrip	Z29	0.110″ × 0.082″ Microstrip
Z8, Z9	0.252″ × 0.068″ Microstrip	Z20, Z21	0.060″ × 0.230″ Microstrip	Z30	0.100″ × 0.082″ Microstrip
Z10, Z11	0.078″ × 0.746″ Microstrip	Z22, Z23	1.040″ × 0.230″ Microstrip		

* Line length include microstrip bends

TYPICAL CHARACTERISTICS — 230 MHz

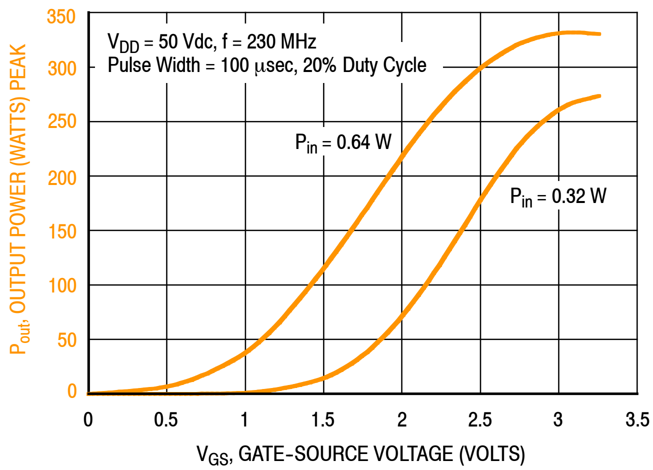
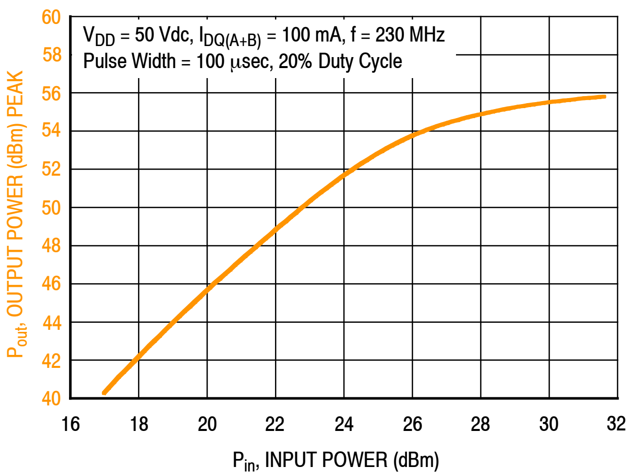


Figure 7. Output Power versus Gate-Source Voltage at a Constant Input Power



f (MHz)	P1dB (W)	P3dB (W)
230	313	370

Figure 8. Output Power versus Input Power

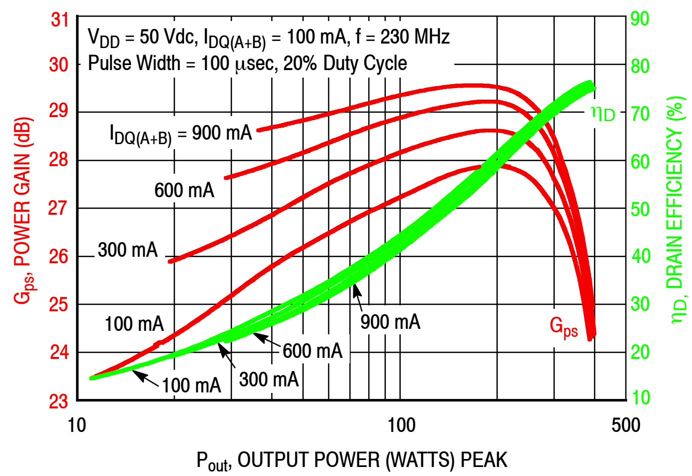


Figure 9. Power Gain and Drain Efficiency versus Output Power and Quiescent Current

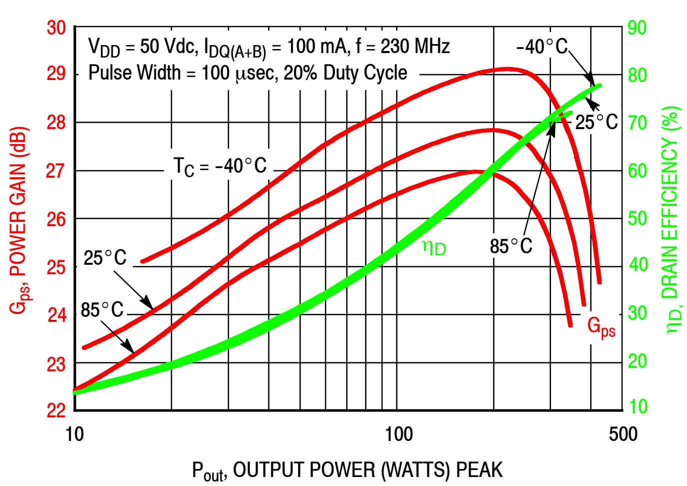


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

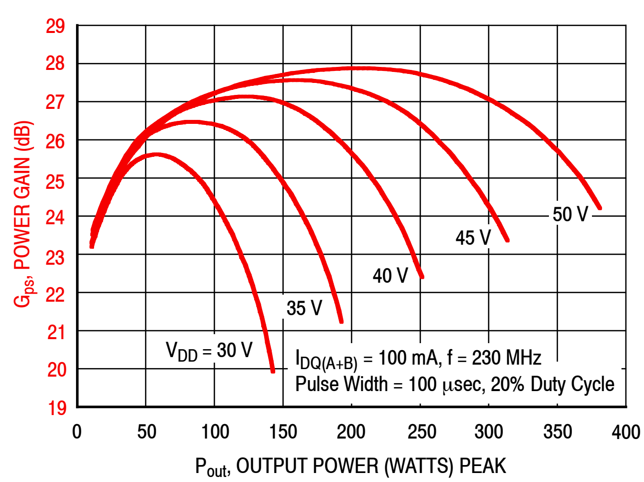


Figure 11. Power Gain versus Output Power and Drain-Source Voltage

V_{DD} = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, P_{out} = 300 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
230	1.50 – j10.70	8.30 + j6.90

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

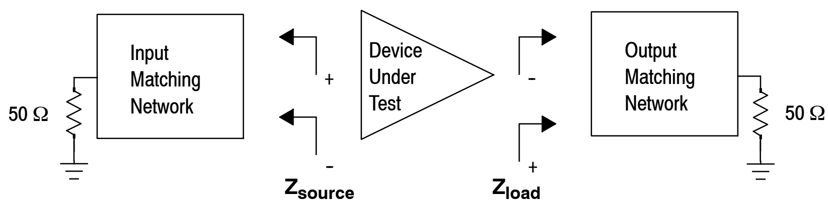


Figure 12. Narrowband Series Equivalent Source and Load Impedance — 230 MHz

87.5–108 MHz BROADBAND REFERENCE CIRCUIT

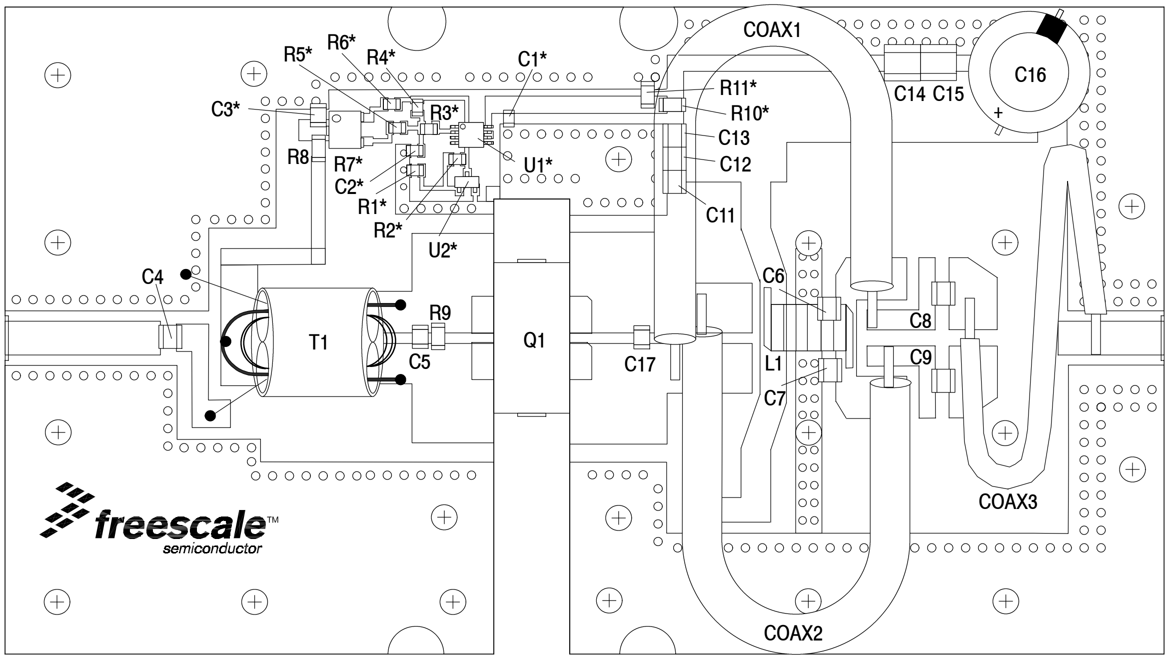
Table 9. 87.5–108 MHz Broadband Performance (In Freescale Reference Circuit, 50 ohm system)
V_{DD} = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, P_{in} = 1.5 W, CW

Frequency (MHz)	G_{ps} (dB)	η_D (%)	P_{out} (W)
87.5	24.4	80.1	415
98	24.3	81.8	404
108	23.8	80.5	361

Table 10. Load Mismatch/Ruggedness (In Freescale Reference Circuit, 50 ohm system) $I_{DQ(A+B)}$ = 100 mA

Frequency (MHz)	Signal Type	VSWR	P_{in} (W)	Test Voltage, V_{DD}	Result
98	CW	> 65:1 at all Phase Angles	3 (3 dB Overdrive)	50	No Device Degradation

87.5–108 MHz BROADBAND REFERENCE CIRCUIT



Note: Component number C10 is not used.

*Bias Regulator and Temperature Compensation. Refer to AN1643, *RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1643.

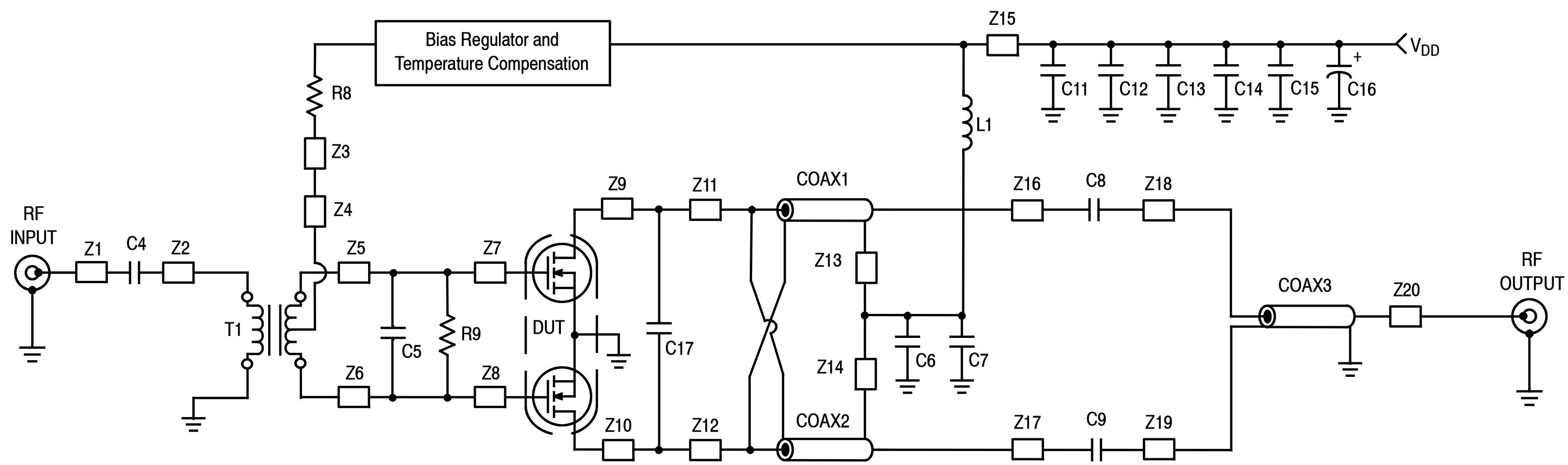
Figure 13. MMRF1316NR1 Broadband Reference Circuit Component Layout — 87.5–108 MHz

87.5–108 MHz BROADBAND REFERENCE CIRCUIT

Table 11. MMRF1316NR1 Broadband Reference Circuit Component Designations and Values — 87.5–108 MHz

Part	Description	Part Number	Manufacturer
C1, C2	1 μF Chip Capacitors	GRM31CR72A105KA01L	Murata
C3	10 nF Chip Capacitor	ATC200B103KT50XT	ATC
C4	150 pF Chip Capacitor	ATC100B151JT300XT	ATC
C5	20 pF Chip Capacitor	ATC100B200JT500XT	ATC
C6, C8, C9	1000 pF Chip Capacitors	ATC200B102KT50XT	ATC
C7	560 pF Chip Capacitor	ATC100B561KT50XT	ATC
C11	10 nF Chip Capacitor	GCJ216R72A103KA01D	Murata
C12	47 nF Chip Capacitor	GCJ21BR72A473KA01L	Murata
C13	470 nF Chip Capacitor	GRM31MR72A474KA01L	Murata
C14, C15	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C16	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26	Multicomp
C17	20 pF Chip Capacitor	ATC100B200JT500XT	ATC
Coax1, 2	35 Ω Flex Cable, 4.72″	HSF-141	Hongsen Cable
Coax3	50 Ω Flex Cable, 6.3″	SM141	Huber Suhner
L1	5 Turns, #16 AWG ID = 0.315″/8 mm Inductor, Hand Wound	Copper Wire	
Q1	RF Power LDMOS Transistor	MMRF1316NR1	Freescale
R1	2.2 kΩ, 1/8 W Chip Resistor	CRCW08052K20FKEA	Vishay
R2	390 Ω, 1/8 W Chip Resistor	CRCW0805390RFKEA	Vishay
R3	10 Ω, 1/8 W Chip Resistor	CRCW080510R0FKEA	Vishay
R4	1.0 kΩ, 1/8 W Chip Resistor	CRCW08051K00FKEA	Vishay
R5	2.7 kΩ, 1/8 W Chip Resistor	CRCW08052K70FKEA	Vishay
R6	200 Ω, 1/8 W Chip Resistor	CRCW0805200RFKEA	Vishay
R7	5.0 kΩ Multi-turn Cermet Trimmer Potentiometer	3224W-1-502E	Bourns
R8	10 Ω, 1/4 W Chip Resistor	CRCW120610R0FKEA	Vishay
R9	240 Ω, 1/4 W Chip Resistor	CRCW1206240RFKEA	Vishay
R10	4.7 kΩ, 1/2 W Chip Resistor	CRCW12104K70FKEA	Vishay
R11	5.1 kΩ, 1/2 W Chip Resistor	CRCW12105K10FKEA	Vishay
T1	61 Material Binocular Core Ferrite (9:1) with 24 AWG 1 Turn Primary, 24 AWG 3 Turns Secondary, Hand Wound	2861000202	Fair-Rite
U1	Voltage Regulator 5 V, Micro8	LP2951ACDMR2G	ON Semiconductor
U2	NPN Bipolar Transistor	BC847ALT1G	ON Semiconductor
PCB	Rogers RO4350B, 0.030″, ε_r = 3.66	D59349	MTL

Note: Component number C10 is not used.



Note: Component number C10 is not used.

Figure 14. MMRF1316NR1 Broadband Reference Circuit Schematic — 87.5–108 MHz

Table 12. MMRF1316NR1 Broadband Reference Circuit Microstrips — 87.5–108 MHz

Microstrip	Description	Microstrip	Description
Z1	0.430″ × 0.150″ Microstrip	Z11, Z12	0.400″ × 0.240″ Microstrip
Z2*	0.320″ × 0.080″ Microstrip	Z13, Z14	0.170″ × 0.210″ Microstrip
Z3*	0.680″ × 0.080″ Microstrip	Z15	0.680″ × 0.140″ Microstrip
Z4	0.310″ × 0.170″ Microstrip	Z16*, Z17*	0.200″ × 0.100″ Microstrip
Z5, Z6	0.195″ × 0.240″ Microstrip	Z18, Z19	0.230″ × 0.300″ Microstrip
Z7, Z8	0.380″ × 0.630″ Microstrip	Z20	0.190″ × 0.170″ Microstrip
Z9, Z10	0.380″ × 0.630″ Microstrip		

* Line length includes microstrip bends

TYPICAL CHARACTERISTICS — 87.5–108 MHz BROADBAND REFERENCE CIRCUIT

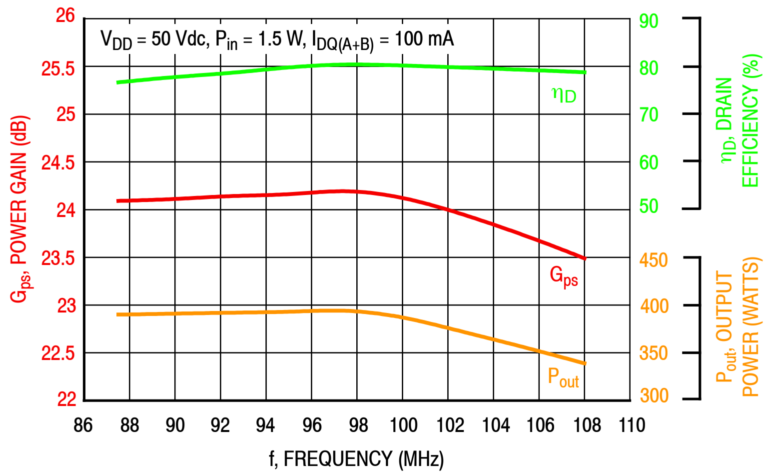


Figure 15. Power Gain, Drain Efficiency and CW Output Power versus Frequency at a Constant Input Power

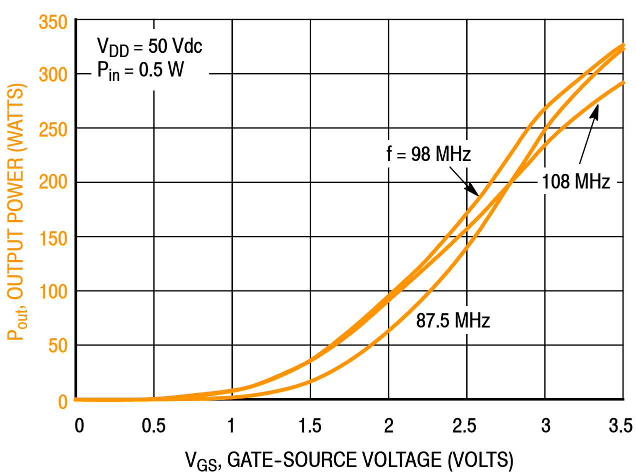


Figure 16. CW Output Power versus Gate-Source Voltage at a Constant Input Power

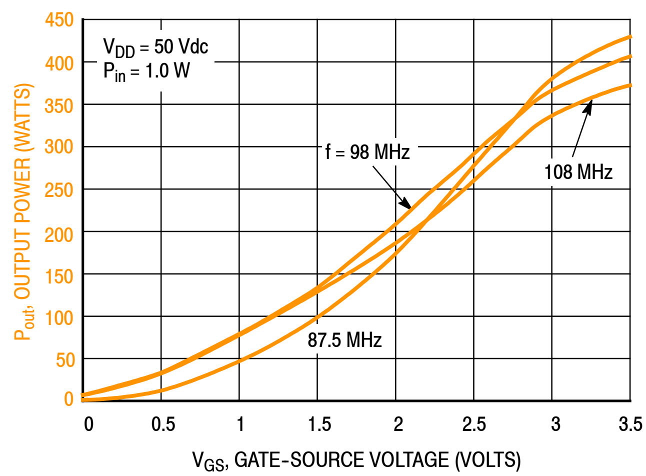
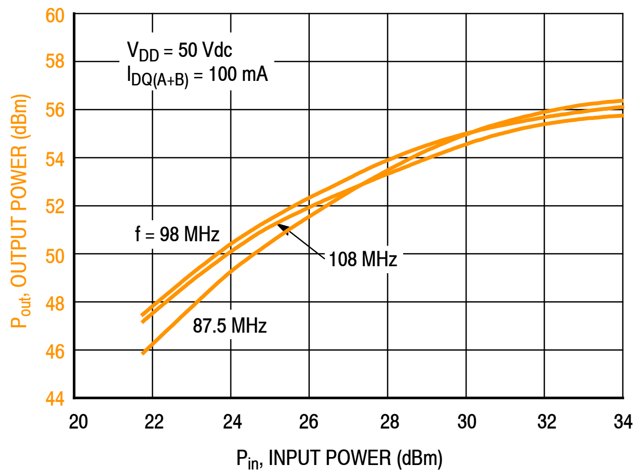


Figure 17. CW Output Power versus Gate-Source Voltage at a Constant Input Power



f (MHz)	P1dB (W)	P3dB (W)
87.5	346	429
98	293	379
108	240	355

Figure 18. CW Output Power versus Input Power

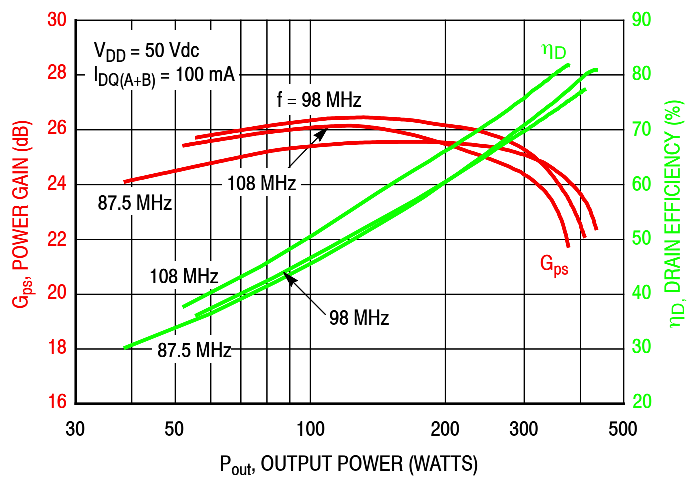
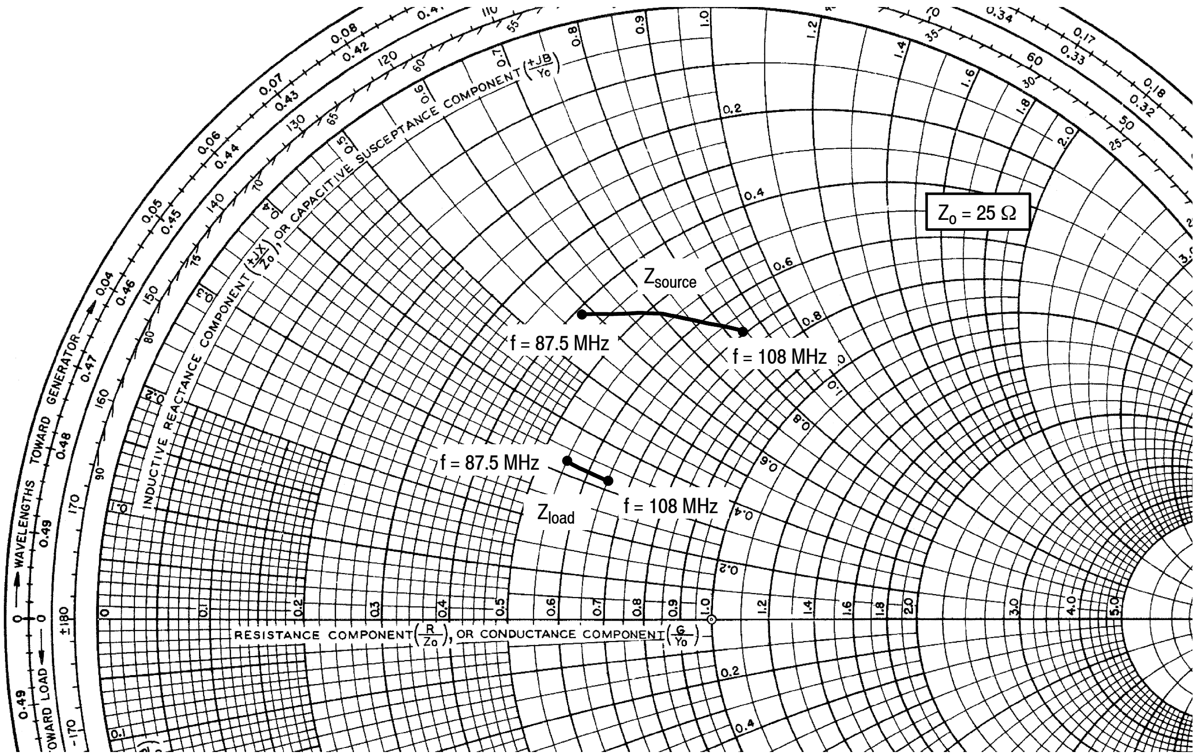


Figure 19. Power Gain and Drain Efficiency versus CW Output Power

87.5–108 MHz BROADBAND REFERENCE CIRCUIT



V_{DD} = 50 Vdc, $I_{DQ(A+B)}$ = 100 mA, P_{out} = 300 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
87.5	10.3 + j14.4	13.7 + j8.15
92	11.5 + j15.8	14.2 + j8.09
96	12.6 + j17.0	14.7 + j8.04
100	13.9 + j18.2	15.2 + j7.99
104	15.5 + j19.6	15.7 + j7.94
108	17.2 + j20.9	16.2 + j7.89

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

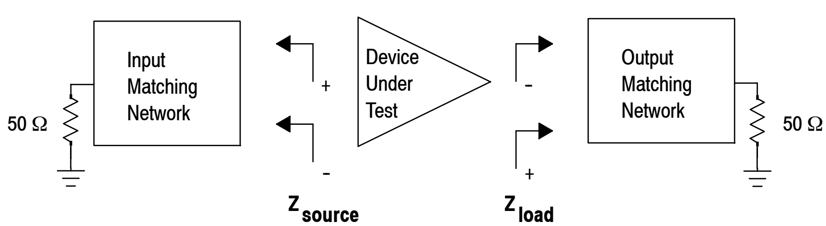
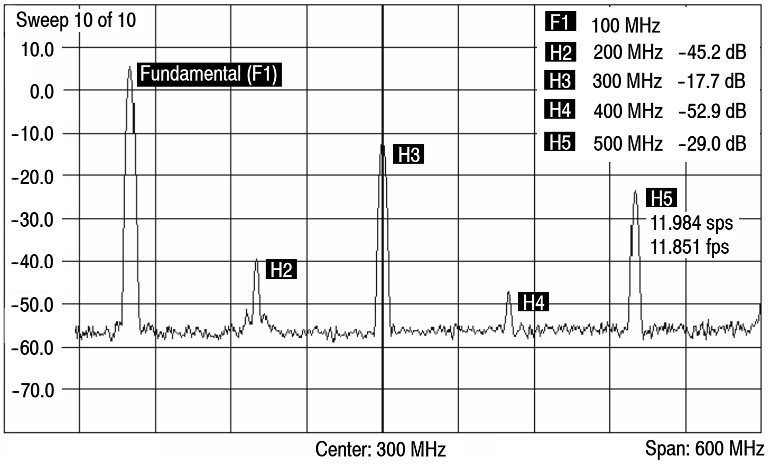


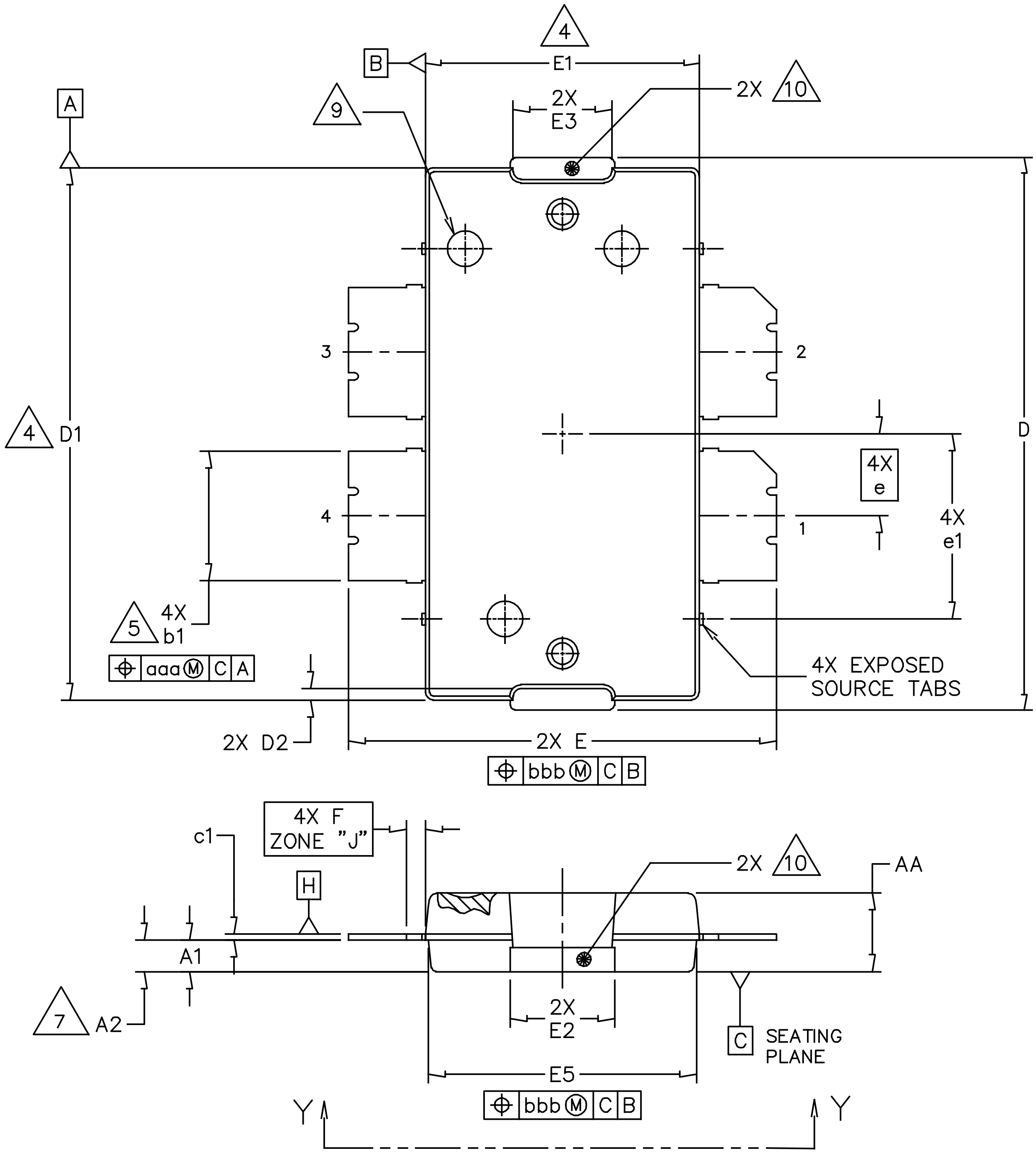
Figure 20. Broadband Series Equivalent Source and Load Impedance — 87.5–108 MHz



H2 (200 MHz)	H3 (300 MHz)	H4 (400 MHz)	H5 (500 MHz)
–45.2 dB	–17.7 dB	–52.9 dB	–29.0 dB

Figure 21. 100 MHz Harmonics @ 300 W CW

PACKAGE DIMENSIONS



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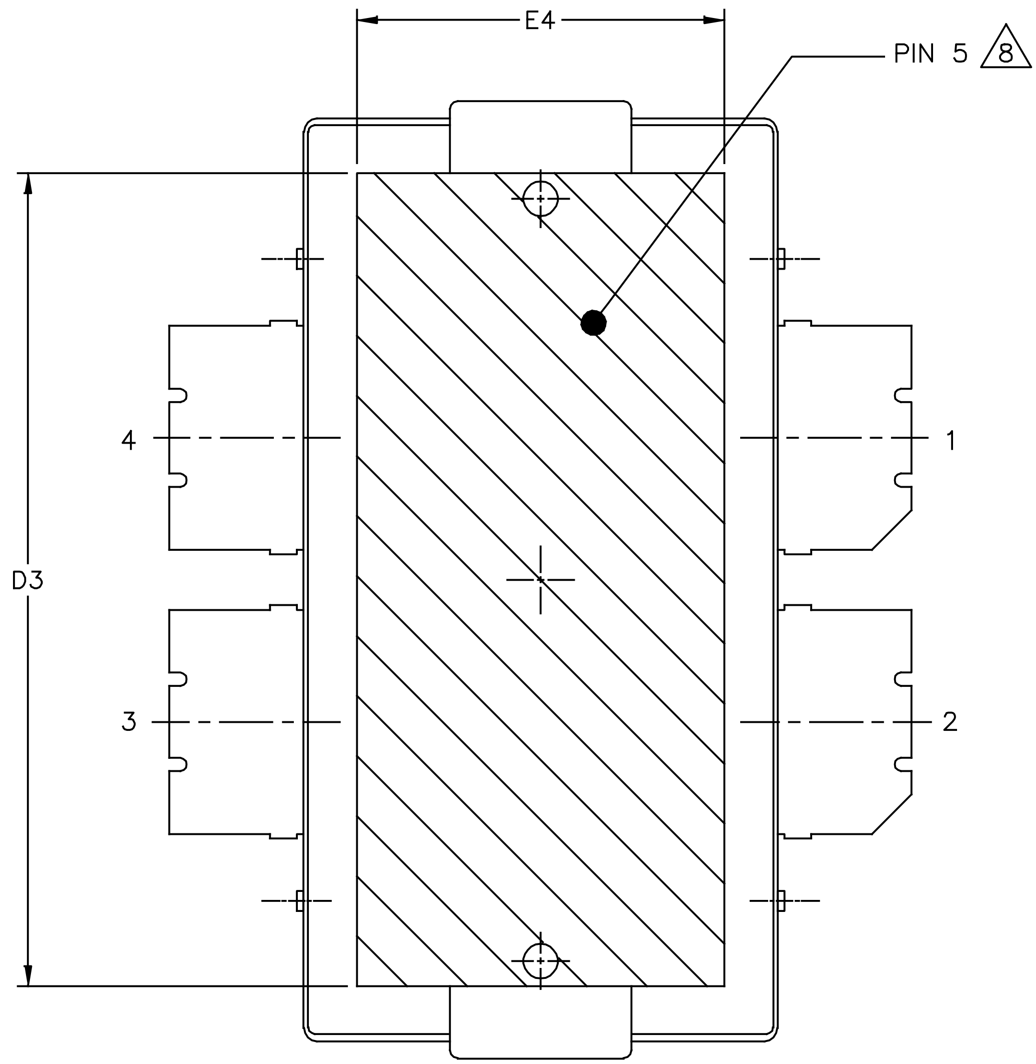

VIEW Y–Y

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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15MM) PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13MM) TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. DIMENSIONS D3 AND D4 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.011	.019	0.28	0.48	aaa	.004		0.10	
D3	.600	---	15.24	---	bbb	.008		0.20	
E	.551	.559	14.00	14.20					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1643: RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2014	• Initial Release of Data Sheet

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