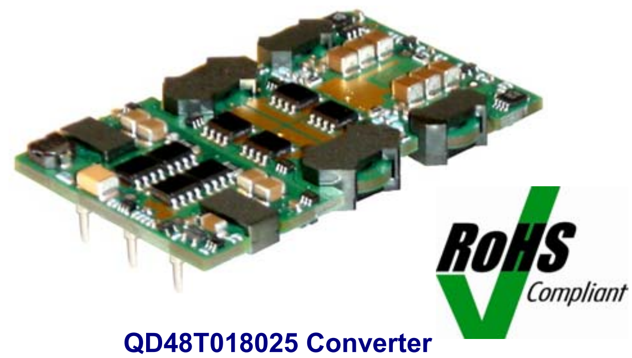
The **QD48T018025** dual output through-hole mounted DC-DC converter offers unprecedented performance in a quarter brick package by providing two independently regulated high current outputs. This is accomplished by the use of patent pending circuit and packaging techniques to achieve ultra-high efficiency, excellent thermal performance and a very low body profile.

In telecommunications applications the **QD48** converters provide up to 15 A per channel simultaneously – 30 A total – with thermal performance far exceeding existing dual quarter bricks and comparable to dual half-bricks. Low body profile and the preclusion of heat sinks minimize airflow shadowing, thus enhancing cooling for downstream devices. The use of 100% surface-mount technologies for assembly, coupled with Power-One's advanced electric and thermal circuitry and packaging, results in a product with extremely high quality and reliability.



QD48T018025 Converter

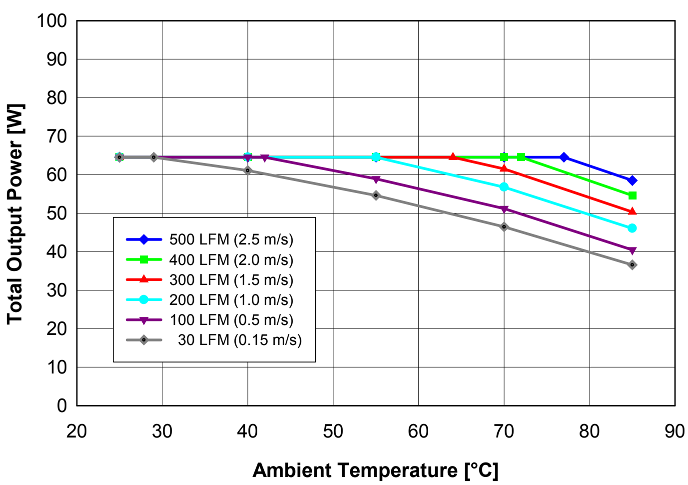


Fig. 1: Available output power vs. ambient air temperature and airflow rates for QD48T018025 converter with D height pins mounted vertically with air flowing from pin 3 to pin 1, MOSFET temperature ≤ 120°C, Vin = 48 V and balanced load on both outputs (Iout1 = Iout2).

Applications

- Telecommunications
- Datacommunications
- Wireless
- Servers

Features

- RoHS lead-free solder and lead-solder-exempted products are available
- Delivers up to 15 A simultaneously on 1.8 VDC and 2.5 VDC outputs
- Can replace two single output quarter-bricks
- Minimal cross-channel interference
- High efficiency: 86% @ 2x15 A, 87% @ 2x7.5 A
- Starts-up into pre-biased output
- No minimum load required
- No heat sink required
- Low profile: 0.28" [7.2 mm]
- Low weight: 1 oz [28 g] typical
- Industry-standard footprint: 1.45" x 2.30"
- Industry-standard pinout
- Meets Basic Insulation Requirements of EN60950
- Withstands 100 V input transient for 100 ms
- On-board LC input filter
- Fixed-frequency operation
- Fully protected
- Output voltage trim range: ±10% for both outputs
- Trim resistor via industry-standard equations
- High reliability: MTBF 2.6 million hours, calculated per Telcordia TR-332, Method I Case 1
- Positive or negative logic ON/OFF option
- UL 60950 recognized in U.S. & Canada, and DEMKO certified per IEC/EN 60950 (pending)
- Meets conducted emissions requirements of FCC Class B and EN55022 Class B with external filter
- All materials meet UL94, V-0 flammability rating

Electrical Specifications

Conditions: T_A=25ºC, Airflow=300 LFM (1.5 m/s), Vin=48 Vdc, unless otherwise specified.

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS						
Input Voltage		Continuous	0		80	Vdc
Operating Ambient Temperature			-40		85	°C
Storage Temperature			-55		125	°C
INPUT CHARACTERISTICS						
Operating Input Voltage Range			36	48	75	Vdc
Input Under Voltage Lockout		Non-latching				
Turn-on Threshold			33	34	35	Vdc
Turn-off Threshold			31	32	33	Vdc
Input Voltage Transient		100 ms			100	V
OUTPUT CHARACTERISTICS						
External Load Capacitance:	1.8 V	Plus full load (resistive)			10,000	µF
	2.5 V	Plus full load (resistive)			10,000	µF
Output Current Range:	1.8 V	At nominal output voltage 1.8 V	0		15	Adc
	2.5 V	At nominal output voltage 2.5 V	0		15	Adc
Current Limit Inception:	1.8 V	Non-latching	16.5	18	19.5	Adc
	2.5 V	Non-latching	16.5	18	19.5	Adc
Peak Short-Circuit Current:	1.8 V	Non-latching. Short = 10 mΩ.		20	30	A
	2.5 V	Non-latching. Short = 10 mΩ.		20	30	A
RMS Short-Circuit Current:	1.8 V	Non-latching			4	Arms
	2.5 V	Non-latching			4	Arms
ISOLATION CHARACTERISTICS						
I/O Isolation			2000			Vdc
Isolation Capacitance				1.3		nF
Isolation Resistance			10			MΩ
FEATURE CHARACTERISTICS						
Switching Frequency				415		kHz
Output Voltage Trim Range[1]	1.8 V	See section: Output Voltage Adjust/TRIM	-10		+10	%
	2.5 V	Simultaneous with 1.8 V output	-10		+10	%
Output Over-Voltage Protection	1.8 V	Non-latching	2.10	2.25	2.34	V
	2.5 V	Non-latching	2.90	3.125	3.25	V
Over-Temperature Shutdown (PCB)		Non-latching		125		°C
Auto-Restart Period		Applies to all protection features		100		ms
Turn-On Time	2.5 V	1.8 V tracks 2.5 V		3		ms
ON/OFF Control (Positive Logic)						
Converter Off			-20		0.8	Vdc
Converter On			2.4		20	Vdc
ON/OFF Control (Negative Logic)						
Converter Off			2.4		20	Vdc
Converter On			-20		0.8	Vdc

Additional Notes:

1. Vout1 and Vout2 can be simultaneously increased or decreased up to 10% via the Trim function. When trimming up, in order not to exceed the converter's maximum allowable output power capability equal to the product of the nominal output voltage and the allowable output current for the given conditions, the designer must, if necessary, decrease the maximum current (originally obtained from the derating curves) by the same percentage to ensure the converter's actual output power remains at or below the maximum allowable output power.

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Electrical Specifications (continued)

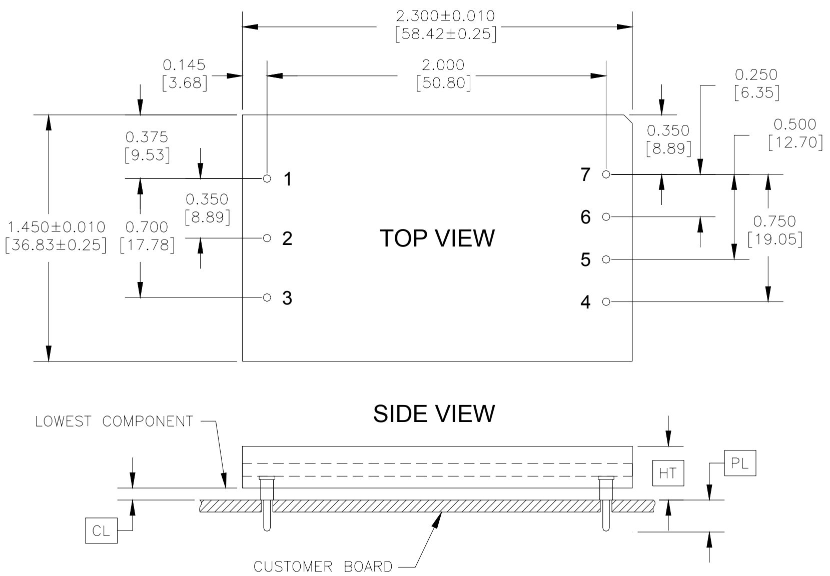
Conditions: T_A=25ºC, Airflow=300 LFM (1.5 m/s), Vin=48 Vdc, unless otherwise specified.

PARAMETER		NOTES	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Maximum Input Current		1.8 Vdc @ 15 Adc, 2.5 Vdc @ 15 Adc, Vin = 36 V			2.1	Adc
Input Stand-by Current		Vin = 48 V, converter disabled		3		mAdc
Input No Load Current (0 load on both outputs)		Vin = 48 V, converter enabled		48		mAdc
Input Reflected-Ripple Current		See Figure 33 - 25MHz bandwidth		6		mA_{PK-PK}
Input Voltage Ripple Rejection		120Hz		TBD		dB
OUTPUT CHARACTERISTICS						
Output Voltage Set Point[2] (no load)	1.8 V	-40ºC to 85ºC	1.787	1.805	1.823	Vdc
	2.5 V	-40ºC to 85ºC	2.480	2.505	2.530	Vdc
Output Regulation: Over Line	1.8 V			±2		mV
	2.5 V			±2		mV
Over Load[3]	1.8 V			-10		mV
	2.5 V			-10		mV
Cross Regulation[4]	1.8 V	For Iout2 (2.5 V) change from 0 to 15 A		-5		mV
	2.5 V	For Iout1 (1.8 V) change from 0 to 15 A		-5		mV
Output Voltage Range	1.8 V	Over line, load and cross regulation	1.764		1.836	Vdc
	2.5 V	Over line, load and cross regulation	2.450		2.550	Vdc
Output Ripple and Noise - 25MHz BW	1.8 V	Full load + 1 µF ceramic		25	40	mV_{PK-PK}
	2.5 V	Full load + 1 µF ceramic		30	50	mV_{PK-PK}
DYNAMIC RESPONSE						
Load Change: 50% to 75% to 50%		ΔIout = 25% of IoutMax				
di/dt = 0.1 A/µS	1.8 V	Co = 10 µF tant. + 1 µF ceramic (Fig.20)		75		mV
	2.5 V	Co = 10 µF tant. + 1 µF ceramic (Fig.21)		60		mV
Setting Time to 1%	1.8 V			100		µs
	2.5 V			100		µs
di/dt = 5 A/µS	1.8 V	Co = 300 µF tant. + 1 µF ceramic (Fig.22)		100		mV
	2.5 V	Co = 300 µF tant. + 1 µF ceramic (Fig.23)		100		mV
Setting Time to 1%	1.8 V			60		µs
	2.5 V			60		µs
EFFICIENCY						
1.8 V 100% Load, 2.5 V 100% Load				86		%
1.8 V 50% Load, 2.5 V 50% Load				87		%

Additional Notes:

2. No load set point is 5 mV higher than the nominal voltage, to partially compensate voltage drop on the output pins.
3. Load regulation is affected with resistance of the output pins (approximately 0.3 mΩ) since there is no remote sense.
4. Cross regulation is affected with resistance of the RETURN pin (approximately 0.3 mΩ) since there is no remote sense.

Physical Information



Pin Connections	
Pin #	**Function**
1	Vin (+)
2	ON/OFF
3	Vin (-)
4	Vout1 (+)
5	RTN [Vout1(-) and Vout2(-)]
6	TRIM
7	Vout2 (+)

- All dimensions are in inches [mm]
- All pins are Ø 0.040" [1.02] with Ø 0.078" [1.98] shoulder
- Pin Material: Brass
- Pin Finish: Tin/Lead over Nickel
- Converter Weight: 1 oz [28 g] typical

Height Option	HT (Maximum Height)	CL (Minimum Clearance)
	+0.000 [+0.00] -0.038 [- 0.97]	+0.016 [+0.41] -0.000 [- 0.00]
A	0.303 [7.69]	0.030 [0.77]
B	0.336 [8.53]	0.063 [1.60]
C	0.500 [12.70]	0.227 [5.77]
D	0.400 [10.16]	0.127 [3.23]

Pin Option	PL Pin Length
	±0.005 [±0.13]
A	0.188 [4.77]
B	0.145 [3.68]
C	0.110 [2.79]

Converter Part Numbering Scheme

Product Series	Input Voltage	Mounting Scheme	Output Voltage 1 ($V_{OUT}1$)	Output Voltage 2 ($V_{OUT}2$)		ON/OFF Logic	Maximum Height [HT]	Pin Length [PL]	Special Features
QD	**48**	**T**	**018**	**025**	**-**	**N**	**B**	**A**	**0**
Dual Quarter-Brick Format	36-75 V	Through-hole	018 ⇒ 1.8 V Note: Always specify $V_{OUT}2$ as the higher of the two output voltages.	025 ⇒ 2.5 V		N ⇒ Negative P ⇒ Positive	A ⇒ 0.303" B ⇒ 0.336" C ⇒ 0.500" D ⇒ 0.400"	A ⇒ 0.188" B ⇒ 0.145" C ⇒ 0.110"	0 ⇒ STD

The example above describes P/N QD48T018025-NBA0: 36-75 V input, dual output, through-hole mounting, 1.8 V and 2.5 V outputs @ 15 A each, negative ON/OFF logic, a maximum height of 0.336", and a through the board pin length of 0.188". Please consult factory regarding availability of a specific version.

RoHS Ordering Information:

- No RoHS suffix character is required for lead-solder-exemption compliance.
- For RoHS compliance to all six substances, add the letter "G" as the last letter of the part number.

Operation

Input and Output Impedance

These power converters have been designed to be stable with no external capacitors when used in low inductance input and output circuits.

However, in many applications, the inductance associated with the distribution from the power source to the input of the converter can affect the stability of the converter. The addition of a 33 µF electrolytic capacitor with an ESR < 1 Ω across the input helps ensure stability of the converter. In many applications, the user has to use decoupling capacitance at the load. The converter will exhibit stable operation with external load capacitance up to 10,000 µF on both outputs.

ON/OFF (Pin 2)

The ON/OFF pin is used to turn the power converter on or off remotely via a system signal. There are two remote control options available, positive logic and negative logic and both are referenced to Vin(-). Typical connections are shown in Fig. 2.

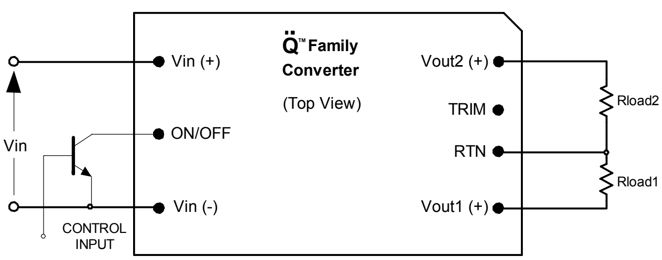


Fig. 2: Circuit configuration for ON/OFF function.

The positive logic version turns on when the ON/OFF pin is at logic high and turns off when at logic low. The converter is on when the ON/OFF pin is left open.

The negative logic version turns on when the pin is at logic low and turns off when the pin is at logic high. The ON/OFF pin can be hard wired directly to Vin(-) to enable automatic power up of the converter without the need of an external control signal.

ON/OFF pin is internally pulled-up to 5 V through a resistor. A mechanical switch, open collector transistor, or FET can be used to drive the input of the ON/OFF pin. The device must be capable of sinking up to 0.2 mA at a low level voltage of ≤ 0.8 V. An external voltage source of ±20 V max. may be connected directly to the ON/OFF input, in which case it should be capable of sourcing or sinking up to 1 mA depending on the signal polarity. See the Start-up Information section for system timing waveforms associated with use of the ON/OFF pin.

Output Voltage Adjust /TRIM (Pin 6)

The converter's output voltages can be adjusted simultaneously up 10% or down 10% relative to the rated output voltages by the addition of an externally connected resistor.

The TRIM pin should be left open if trimming is not being used. To minimize noise pickup, a 0.1 µF capacitor is connected internally between the TRIM and RETURN pins.

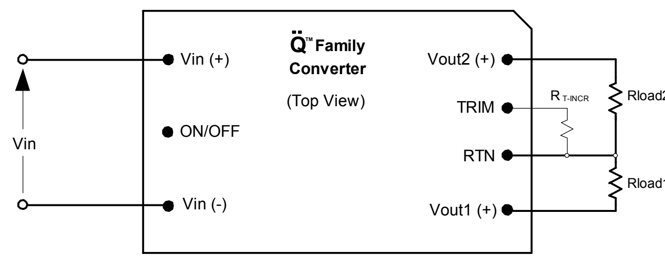


Fig. 3: Configuration for increasing output voltage.

To increase the output voltage (refer to Fig. 3), a trim resistor, $R_{T\text{-}INCR}$, should be connected between the TRIM (Pin 6) and RETURN (Pin 5), with a value from the table below.

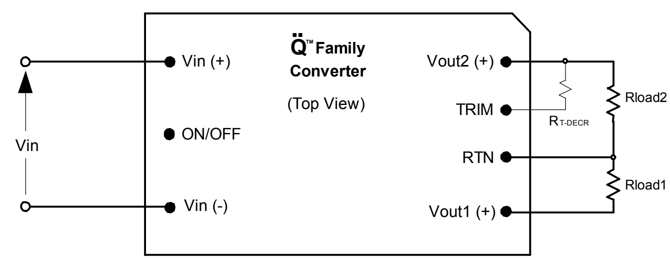


Fig. 4: Configuration for decreasing output voltage.

To decrease the output voltage, a trim resistor $R_{T\text{-}DECR}$, (Fig. 4) should be connected between the TRIM (Pin 6) and Vout2(+) pin (Pin 7), with a value from the table below, where:

Δ = percentage of increase or decrease Vout(NOM).

Note 1: Both outputs are trimmed up or down simultaneously.

Trim Resistor (Vout Increase)	
Δ [%]	R_{T-INCR} [kΩ]
1	46.4
2	20.5
3	12.1
4	8.06
5	5.23
6	3.57
7	2.21
8	1.30
9	0.604
10	0

Trim Resistor (Vout Decrease)	
Δ [%]	R_{T-DECR} [kΩ]
-1	57.6
-2	25.5
-3	14.0
-4	8.87
-5	5.90
-6	3.83
-7	2.32
-8	1.30
-9	0.432
-10	0

Note 2: The above trim resistor values match those typically used in industry-standard dual quarter bricks.

Protection Features

Input Undervoltage Lockout

Input undervoltage lockout is standard with this converter. The converter will shut down when the input voltage drops below a pre-determined voltage.

The input voltage must be at least 35 V for the converter to turn on. Once the converter has been turned on, it will shut off when the input voltage drops below 31 V. This feature is beneficial in preventing deep discharging of batteries used in telecom applications.

Output Overcurrent Protection (OCP)

The converter is protected against over-current or short circuit conditions on both outputs. Upon sensing an over-current condition, the converter will switch to constant current operation and thereby begin to reduce output voltages. If, due to current limit, the output voltage Vout2 (2.5 V) drops below Vout1 - 0.6 V converter will shutdown. If, due to current limit, the output voltage Vout1 (1.8 V) drops below 60% of its nominal value (1.1 V) the converter will shut down (Figs. 26 and 27). Thus, current limit on one output does not affect regulation on the other output.

Once the converter has shut down, it will attempt to restart nominally every 100 ms with a typical 2% duty cycle (Figs. 28 and 29). The attempted restart will continue indefinitely until the overload or short circuit conditions are removed or the output voltage rises above under-voltage threshold.

Output Overvoltage Protection (OVP)

The converter will shut down if the output voltage across either Vout1(+) (Pin 4) or Vout2(+) (Pin 7) and RETURN (Pin 5) exceeds the threshold of the OVP circuitry. The OVP protection is separate for Vout1 and Vout2 with their own reference independent of the output voltage regulation loops. Once the converter has shut down, it will attempt to restart every 100 ms until the OVP condition is removed.

Overtemperature Protection (OTP)

The converter will shut down under an overtemperature condition to protect itself from overheating caused by operation outside the thermal derating curves, or operation in abnormal conditions such as system fan failure. After the converter has cooled to a safe operating temperature, it will automatically restart.

Safety Requirements

The converters meet North American and International safety regulatory requirements per UL60950 and EN60950. Basic Insulation is provided between input and output.

To comply with safety agencies requirements, an input line fuse must be used external to the converter. A 4-A fuse is recommended for use with this product.

Electromagnetic Compatibility (EMC)

EMC requirements must be met at the end-product system level, as no specific standards dedicated to EMC characteristics of board mounted component dc-dc converters exist. However, Power-One tests its converters to several system level standards, primary of which is the more stringent EN55022, *Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement.*

With the addition of a simple external filter (see application notes), all versions of the QD48T converters pass the requirements of Class B conducted emissions per EN55022 and FCC, and meet at a minimum, Class A radiated emissions per EN 55022 and Class B per FCC Title 47CFR, Part 15-J. Please contact Power-One Applications Engineering for details of this testing.

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Characterization

General Information

The converter has been characterized for many operational aspects, to include thermal derating (maximum load current as a function of ambient temperature and airflow) for vertical and horizontal mounting, efficiency, start-up and shutdown parameters, output ripple and noise, transient response to load step-change, overload and short circuit.

The following pages contain specific plots or waveforms associated with the converter. Additional comments for specific data are provided below.

Test Conditions

All data presented were taken with the converter soldered to a test board, specifically a 0.060" thick printed wiring board (PWB) with four layers. The top and bottom layers were not metalized. The two inner layers, comprising two-ounce copper, were used to provide traces for connectivity to the converter.

The lack of metalization on the outer layers as well as the limited thermal connection ensured that heat transfer from the converter to the PWB was minimized. This provides a worst-case but consistent scenario for thermal derating purposes.

All measurements requiring airflow were made in Power-One's vertical and horizontal wind tunnel facilities using infrared (IR) thermography and thermocouples for thermometry.

Ensuring that the components on the converter do not exceed their ratings is important to maintaining high reliability. If one anticipates operating the converter at or close to the maximum loads specified in the derating curves, it is prudent to check actual operating temperatures in the application. Thermographic imaging is preferable; if this capability is not available, then thermocouples may be used. Power-One recommends the use of AWG #40 gauge thermocouples to ensure measurement accuracy. Careful routing of the thermocouple leads will further minimize measurement error. Refer to Figure 34 for optimum measuring thermocouple location.

Thermal Derating

Available output power and load current vs. ambient temperature and airflow rates are given in Figs. 8-11. Ambient temperature was varied between 25°C and 85°C, with airflow rates from 30 to 500 LFM (0.15 to 2.5 m/s), and vertical and horizontal converter mounting.

For each set of conditions, the maximum load current was defined as the lowest of:

(i) The output current at which either any FET junction temperature did not exceed a maximum specified temperature (120°C) as indicated by the thermographic image, or

(ii) The nominal rating of the converter (15 A on either output)

During normal operation, derating curves with maximum FET temperature less than or equal to 120°C should not be exceeded. Temperature on the PCB at the thermocouple location shown in Fig. 34 should not exceed 118°C in order to operate inside the derating curves.

Efficiency

Efficiency vs. load current plots are shown in Figs. 12-17 for ambient temperature of 25ºC, airflow rate of 300 LFM (1.5 m/s), both vertical and horizontal orientations, and input voltages of 36 V, 48 V and 72 V, for different combinations of the loads on outputs Vout1 and Vout2.

Start-up

Output voltage waveforms during the turn-on transient using the ON/OFF pin, are shown without and with full rated load currents (resistive load) in Figs. 18 and 19, respectively.

Ripple and Noise

Figure 30 shows the output voltage ripple waveform, measured at full rated load current on both outputs with a 1 μF ceramic capacitor across both outputs. Note that all output voltage waveforms are measured across a 1 μF ceramic capacitor.

The input reflected ripple current waveforms are obtained using the test setup shown in Fig. 31. The corresponding waveforms are shown in Figs. 32 and 33.

Start-up Information (using negative ON/OFF)

Scenario #1: Initial Start-up From Bulk Supply
ON/OFF function enabled, converter started via application of V_{IN}. See Figure 5.

Time	Comments
t_0	ON/OFF pin is ON; system front end power is toggled on, V_{IN} to converter begins to rise.
t_1	V_{IN} crosses Under-Voltage Lockout protection circuit threshold; converter enabled.
t_2	Converter begins to respond to turn-on command (converter turn-on delay).
t_3	Output voltage $V_{OUT}1$ reaches 100% of nominal value.
t_4	Output voltage $V_{OUT}2$ reaches 100% of nominal value.

For this example, the total converter start-up time (t_4- t_1) is typically 3 ms.

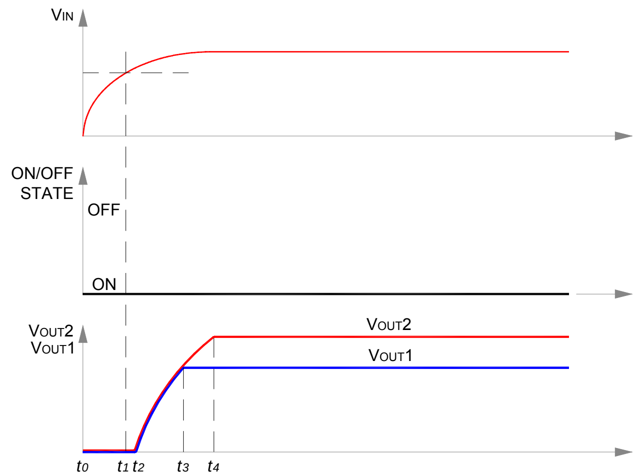

Fig. 5: Start-up scenario #1.

Scenario #2: Initial Start-up Using ON/OFF Pin
With V_{IN} previously powered, converter started via ON/OFF pin. See Figure 6.

Time	Comments
t_0	V_{INPUT} at nominal value.
t_1	Arbitrary time when ON/OFF pin is enabled (converter enabled).
t_2	End of converter turn-on delay.
t_3	Output voltage $V_{OUT}1$ reaches 100% of nominal value.
t_4	Output voltage $V_{OUT}2$ reaches 100% of nominal value.

For this example, the total converter start-up time (t_4 - t_1) is typically 3 ms.

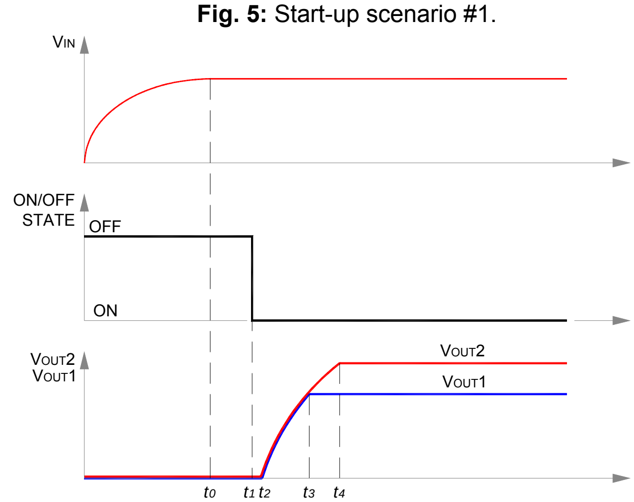

Fig. 6: Start-up scenario #2.

Scenario #3: Turn-off and Restart Using ON/OFF Pin
With V_{IN} previously powered, converter is disabled and then enabled via ON/OFF pin. See Figure 7.

Time	Comments
t_0	V_{IN} and V_{OUT} are at nominal values; ON/OFF pin ON.
t_1	ON/OFF pin arbitrarily disabled; converter outputs fall to zero; turn-on inhibit delay period (100 ms typical) is initiated, and ON/OFF pin action is internally inhibited.
t_2	ON/OFF pin is externally re-enabled. **If (t_2- t_1) ≤ 100 ms**, external action of ON/OFF pin is locked out by start-up inhibit timer. **If (t_2- t_1) > 100 ms**, ON/OFF pin action is internally enabled.
t_3	Turn-on inhibit delay period ends. If ON/OFF pin is ON, converter begins turn-on; if off, converter awaits ON/OFF pin ON signal; see Figure 6.
t_4	End of converter turn-on delay.
t_5	Output voltage $V_{OUT}1$ reaches 100% of nominal value.
t_6	Output voltage $V_{OUT}2$ reaches 100% of nominal value.

For the condition, **(t_2 - t_1) ≤ 100 ms**, the total converter start-up time (t_6 - t_2) is typically 103 ms. For **(t_2 - t_1) > 100 ms**, start-up time will be typically 3 ms after release of ON/OFF pin.

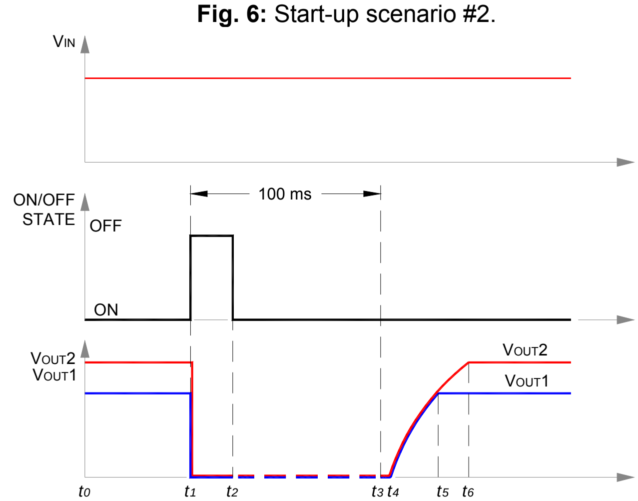

Fig. 7: Start-up scenario #3.

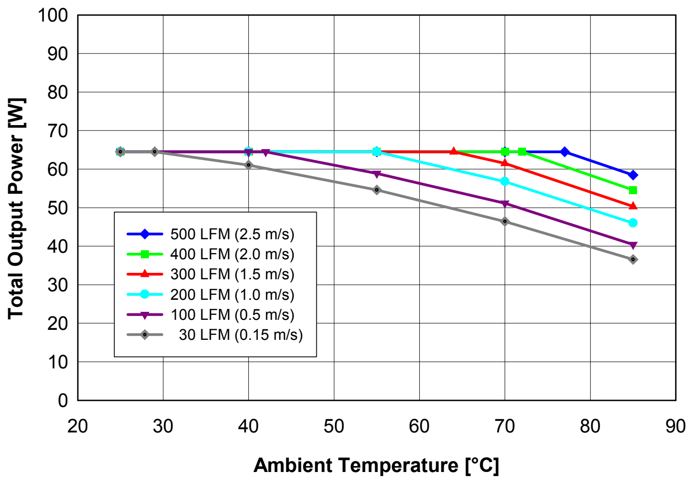

Fig. 8: Available output power for balanced load current (Iout1 = Iout2) vs. ambient air temperature and airflow rates for converter with D height pins mounted vertically with Vin = 48 V, air flowing from pin 3 to pin 1 and maximum FET temperature ≤ 120°C.

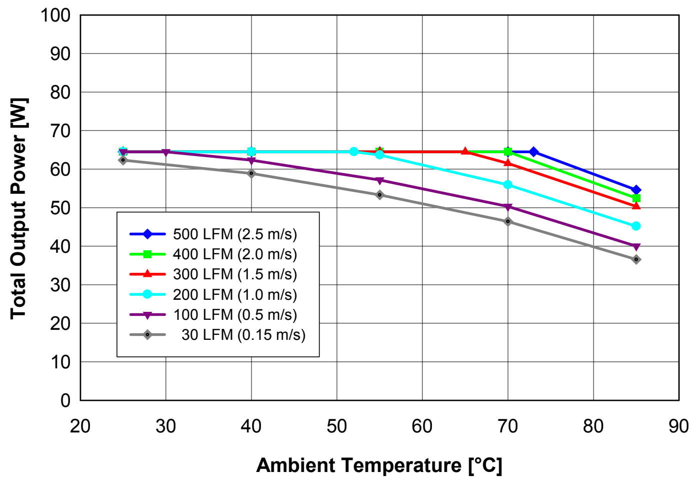

Fig. 9: Available output power for balanced load current (Iout1 = Iout2) vs. ambient air temperature and airflow rates for converter with D height pins mounted horizontally with Vin = 48 V, air flowing from pin 3 to pin 1 and maximum FET temperature ≤ 120°C.

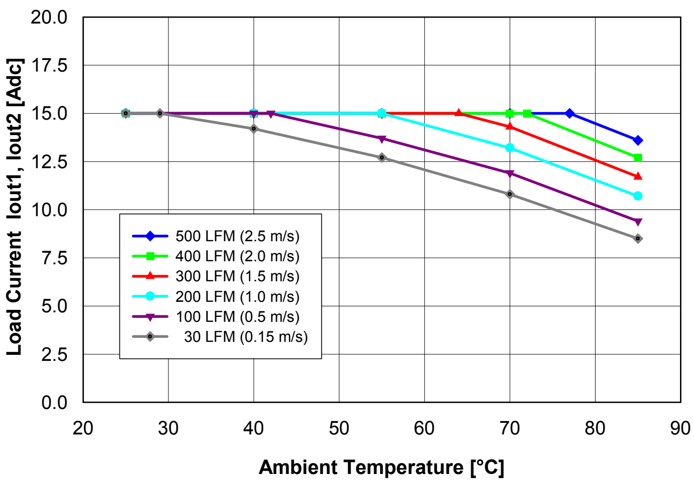

Fig. 10: Available balanced load current (Iout1 = Iout2) vs. ambient air temperature and airflow rates for converter with D height pins mounted vertically with Vin = 48 V, air flowing from pin 3 to pin 1 and maximum FET temperature ≤ 120°C.

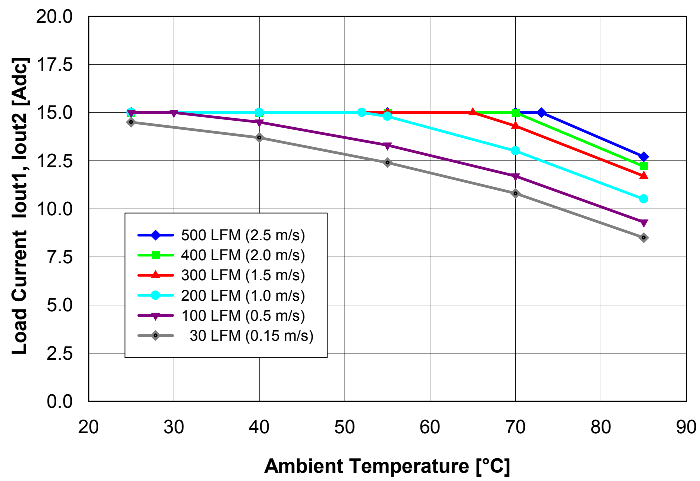

Fig. 11: Available balanced load current (Iout1 = Iout2) vs. ambient temperature and airflow rates for converter with D height pins mounted horizontally with Vin = 48 V, air flowing from pin 3 to pin 1 and maximum FET temperature ≤ 120°C.

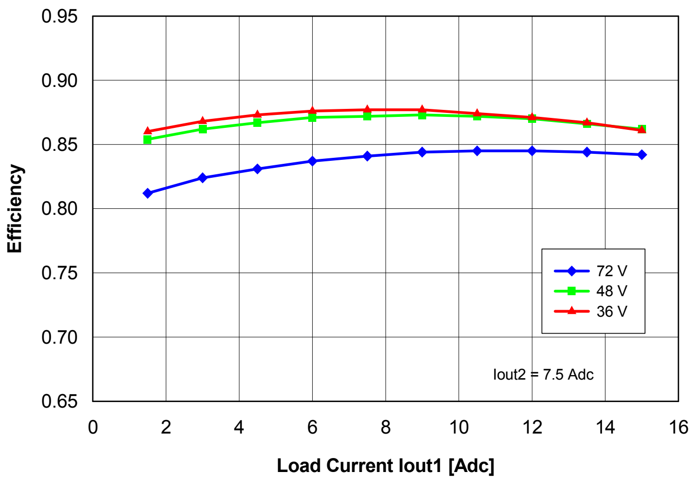

Fig. 12: Efficiency vs. load current Iout1 and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s), for Iout2 = 7.5 A and Ta = 25°C.

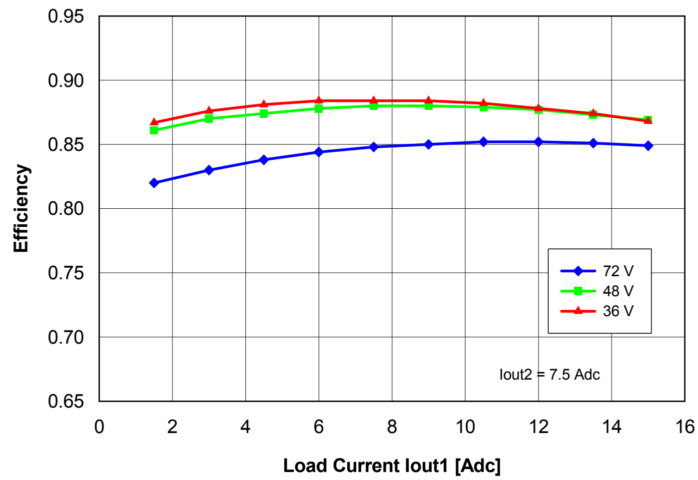

Fig. 13: Efficiency vs. load current Iout1 and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s), for Iout2 = 7.5 A and Ta = 25°C.

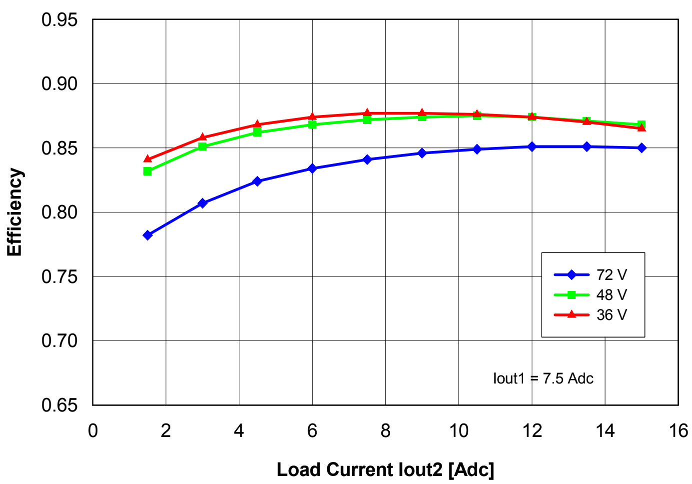

Fig. 14: Efficiency vs. load current Iout2 and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s), for Iout1 = 7.5 A and Ta = 25°C.

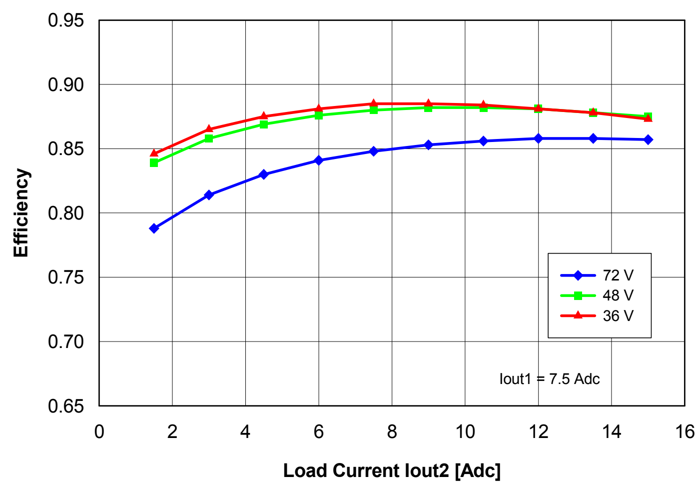

Fig. 15: Efficiency vs. load current Iout2 and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s), for Iout1 = 7.5 A and Ta = 25°C.

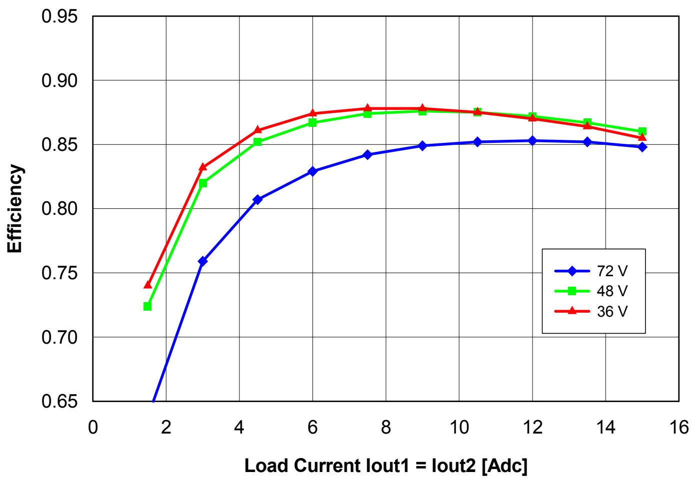

Fig. 16: Efficiency vs. balanced load current (Iout1 = Iout2) and input voltage for converter mounted vertically with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s) and Ta = 25°C.

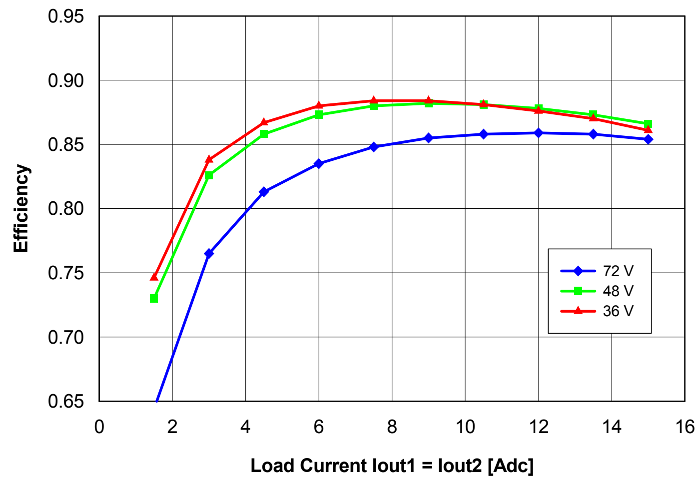

Fig. 17: Efficiency vs. balanced load current (Iout1 = Iout2) and input voltage for converter mounted horizontally with air flowing from pin 3 to pin 1 at a rate of 300 LFM (1.5 m/s) and Ta = 25°C.

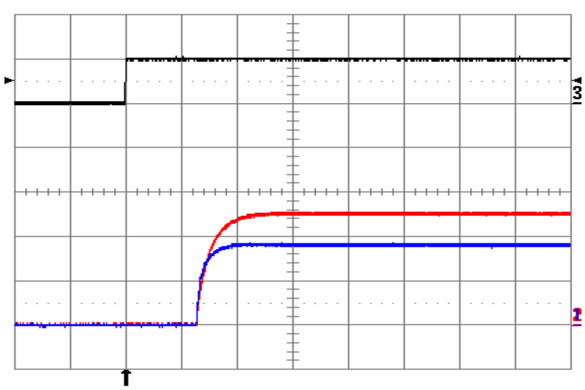

Fig. 18: Turn-on transient waveforms at no load current and Vin = 48 V, triggered via ON/OFF pin. Top trace: ON/OFF signal (5 V/div.). Bottom traces: Vout1 (blue, 1 V/div.), Vout2 (red, 1 V/div.). Time scale: 1 ms/div.

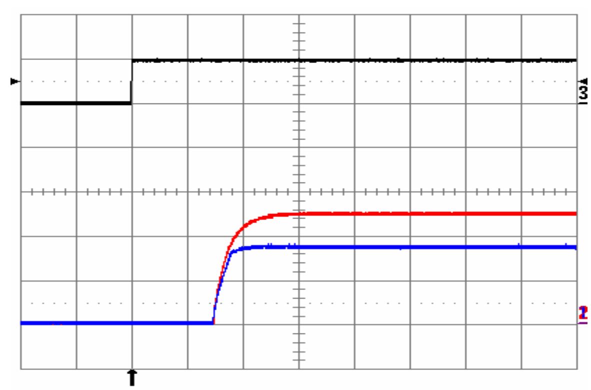

Fig. 19: Turn-on transient waveforms at full rated load current (resistive) and Vin = 48 V, triggered via ON/OFF pin. Top trace: ON/OFF signal (5 V/div.). Bottom traces: Vout1 (blue, 1 V/div.), Vout2 (red, 1 V/div.). Time scale: 1 ms/div.

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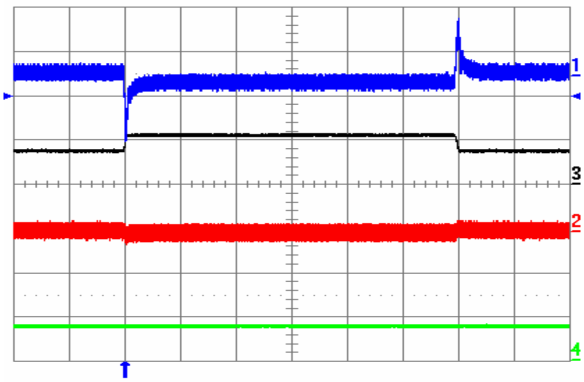

Fig. 20: Output voltage response to Iout1 load current step-change of 3.75 A (50%-75%-50%) at Iout2 = 7.5 A and Vin = 48 V. Ch1 = Vout1 (50 mV/div), Ch2 = Vout2 (50 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 0.1 A/µs, Co = 10 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

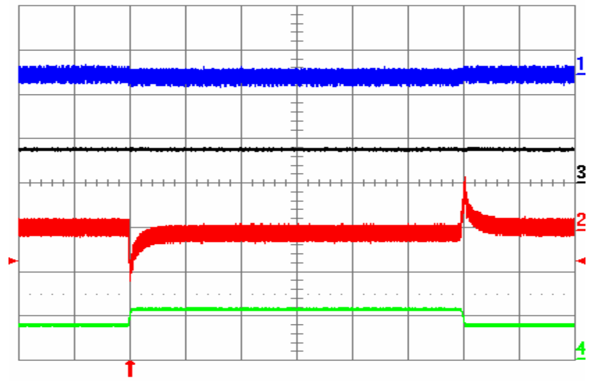

Fig. 21: Output voltage response to Iout2 load current step-change of 3.75 A (50%-75%-50%) at Iout1 = 7.5 A and Vin = 48 V. Ch1 = Vout1 (50 mV/div), Ch2 = Vout2 (50 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 0.1 A/µs, Co = 10 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

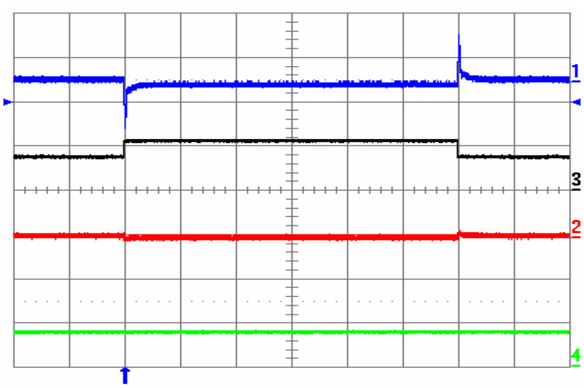

Fig. 22: Output voltage response to Iout1 load current step-change of 3.75 A (50%-75%-50%) at Iout2 = 7.5 A and Vin = 48 V. Ch1 = Vout1 (100 mV/div), Ch2 = Vout2 (100 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 5 A/µs, Co = 300 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

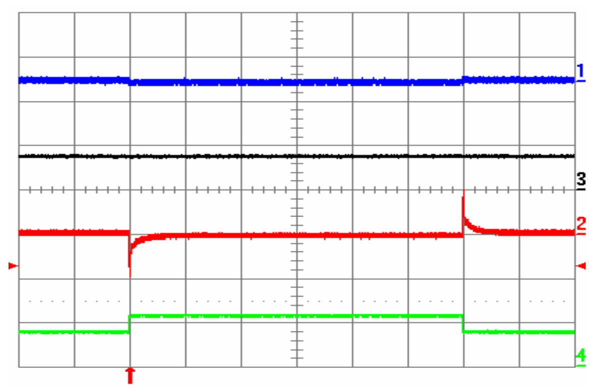

Fig. 23: Output voltage response to Iout2 load current step-change of 3.75 A (50%-75%-50%) at Iout1 = 7.5 A and Vin = 48 V. Ch1 = Vout1 (100 mV/div), Ch2 = Vout2 (100 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 5 A/µs, Co = 300 µF tantalum + 1 µF ceramic. Time scale: 0.5 ms/div.

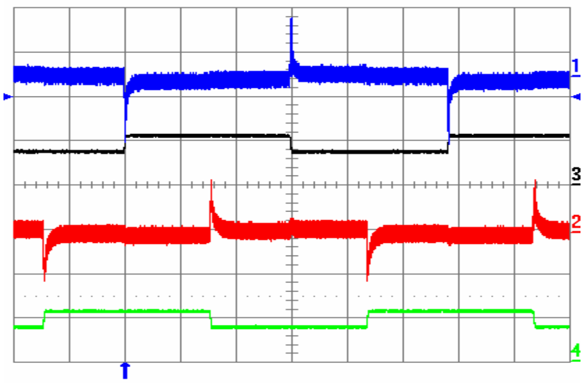

Fig. 24: Output voltage response to both Iout1 and Iout2 (out of phase) load current step-change of 3.75 A (50%-75%-50%) at Vin = 48 V. Ch1 = Vout1 (50 mV/div), Ch2 = Vout2 (50 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 0.1 A/µs, Co = 10 µF tantalum + 1 µF ceramic. Time scale: 1 ms/div.

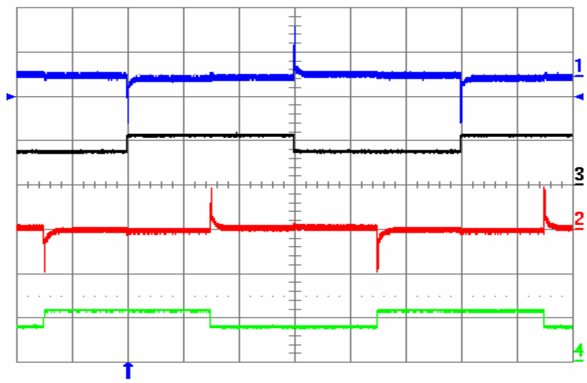

Fig. 25: Output voltage response to both Iout1 and Iout2 (out of phase) load current step-change of 3.75 A (50%-75%-50%) at Vin = 48 V. Ch1 = Vout1 (100 mV/div), Ch2 = Vout2 (100 mV/div), Ch3 = Iout1 (10 A/div.), Ch4 = Iout2 (10 A/div.). Current slew rate: 5 A/µs, Co = 300 µF tantalum + 1 µF ceramic. Time scale: 1 ms/div.

Note: The only cross-talk during transient is due to the common RETURN pin for both outputs.

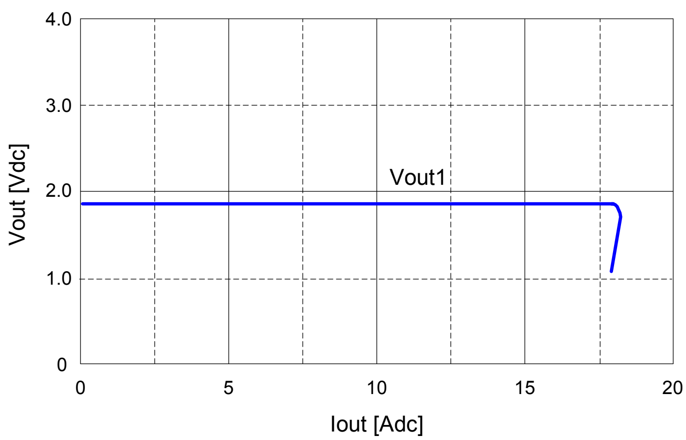

Fig. 26: Output voltage Vout1 vs. load current Iout1 showing current limit point and converter shutdown point. When Vout1 is in current limit, Vout2 is not affected until Vout1 reaches the shut-down threshold of 60% of its nominal value. Input voltage has almost no effect on Vout1 current limit characteristic.

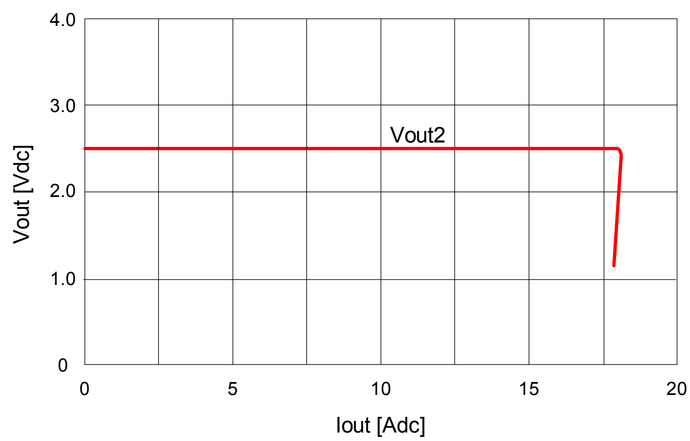

Fig. 27: Output voltage Vout2 vs. load current Iout2 showing current limit point and converter shutdown point. When Vout2 is in current limit, Vout1 is not affected until Vout2 reaches the shut-down threshold equal to Vout1 - 0.6 V. Input voltage has almost no effect on Vout2 current limit characteristic.

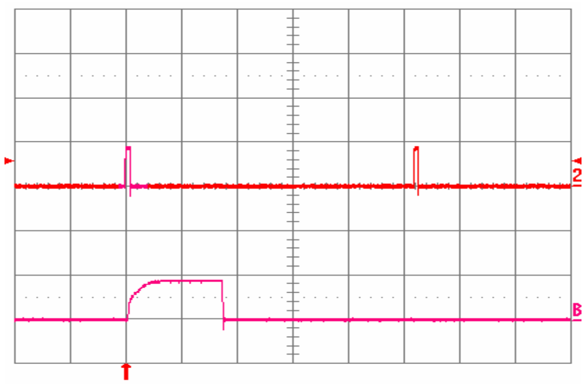

Fig. 28: Load current Iout1 into a 10 mΩ short circuit on Vout1 during restart, with Vout2 open (no load), at Vin = 48 V. Ch2 = Iout1 (20 A/div, 20 ms/div). ChB = Iout1 (20 A/div, 1 ms/div) is an expansion of the on-time portion of Iout1.

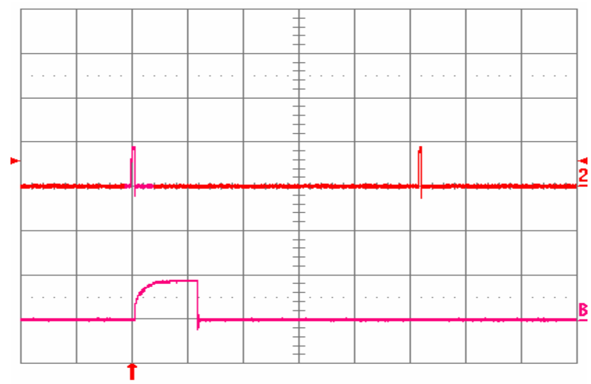

Fig. 29: Load current Iout2 into a 10 mΩ short circuit on Vout2 during restart, with Vout1 open (no load), at Vin = 48 V. Ch2 = Iout2 (20 A/div, 20 ms/div). ChB = Iout2 (20 A/div, 1 ms/div) is an expansion of the on-time portion of Iout2.

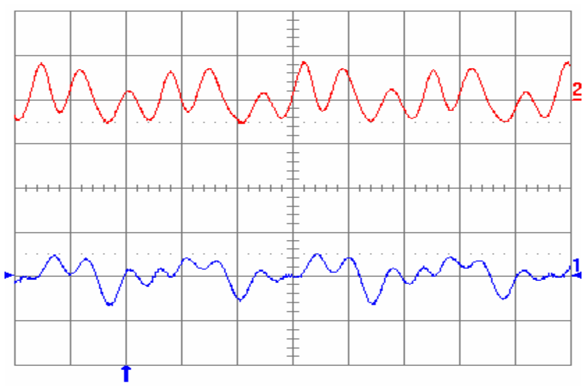

Fig. 30: Output voltage ripple at full rated load current into a resistive load on both outputs with Co = 1uF (ceramic) and Vin = 48 V. Ch2 = Vout2, Ch1 = Vout1 (both 20 mV/div). Time scale: 1 μs/div.

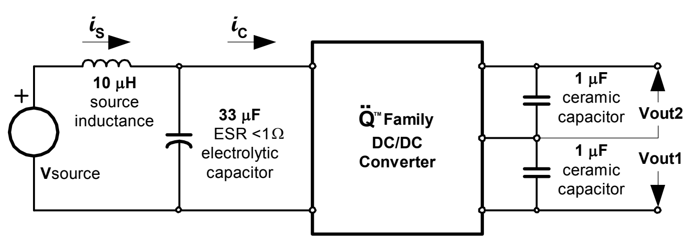

Fig. 31: Test setup for measuring input reflected ripple currents, i_c and i_s.

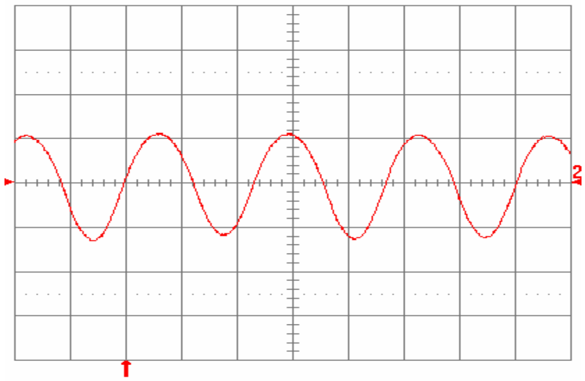

Fig. 32: Input reflected ripple current, i_c (100 mA/div), measured at input terminals at full rated load current on both outputs and Vin = 48 V. Refer to Fig. 31 for test setup. Time scale: 1 μs/div.

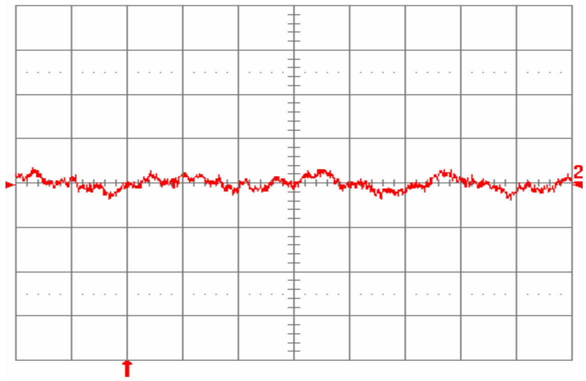

Fig. 33: Input reflected ripple current, i_s (10 mA/div), measured through 10 μH at the source at full rated load current on both outputs and Vin = 48 V. Refer to Fig. 31 for test setup. Time scale: 1μs/div.

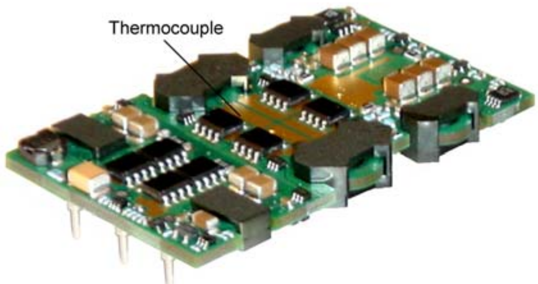

Fig. 34: Location of the thermocouple for thermal testing.