

Gate Driver Unit 2DU180206MR01

■Overview

2DU180206MR01 is a dual channel gate driver designed for Rohm's SiC power module BSM180D12P3C007.

Built-in isolated DC / DC converter and gate drive circuit, in addition, gate resistor and short circuit detection voltage have already been set.

Features

- ·Ideal for drive of SiC Power module BSM180D12P3C007(ROHM)
- •Gate resistor : $+8.2 \Omega / -4.5 \Omega (TYP)$
- ·Short circuit detection voltage : 4.5V(TYP)
- ·Constitution : Gate driver module (2DM180206CM) + PCB for power module connection
- ·ALL-IN-ONE (Built-in isolated DC / DC converter and gate drive circuit)
- ·ldeal for half bridge operation with dual output
- •Optimum gate voltage for driving SiC-MOSFET(+18V/-2V) / BSM180D12P3C007(ROHM)
- ·Low parasitic capacitance (about 15pF); highly resistant to common-mode noise.
- •Fast response : 100nsec(typ)
- $\cdot \, \text{The gate drive circuit used a magnetic isolator.}$
- ·Dielectric withstand voltage : AC2500V (1 second guarantee)
- \cdot Insulation distance (clearance / creepage) : 6mm/6mm
- $\cdot \text{DC/DC}$ converter input voltage : 15 ${\sim}24\text{V}$
- \cdot Signal input voltage : 5V
- ·Overload protection (DC/DC converter)
- ·Overheat protection (DC/DC converter)
- ·Desaturation protection (Gate drive circuit)
- ·Fault signal output function (Gate drive circuit)
- ·Miller clamp function (Gate drive circuit)
- ·Under-voltage lockout(UVLO) (Gate drive circuit)
- Filling structure

Application

Industrial inverter, PV inverter, etc...

■Ciruit Image







2DU180206MR01 Datasheet

■Circuit Diagram



■Pin Connection

CN301 : B2(3)B-EH(JST) For power supply

Pin No.	Name	Function							
1	Vin(+)	Power supply for DC/DC converter(+)							
2	N.C.	Unused							
3	Vin(-)	Power supply for DC/DC converter(-)							

CN302 : B12B-ZR-SM4-TF(JST) For signal

Pin No.	Name	СН	Function
T III NO.			T direction
1	GND2	2(H)	Ground for control circuit
2	INA2	2(H)	Control input A
3	INB2	2(H)	Control input B
4	RDY2	2(H)	Ready output
5	FLT2	2(H)	Fault output
6	XRST2	2(H)	Reset input
7	GND1	1(L)	Ground for control circuit
8	INA 1	1(L)	Control input A
9	INB1	1(L)	Control input B
10	RDY1	1(L)	Ready output
11	FLT1	1(L)	Fault output
12	XRST1	1(L)	Reset input

Connection on the power module

Name	СН	Explanation of pins
CL/DL	1(L)	Drain connection, Low side $*$
GL	1(L)	Gate connection, Low side
EL/SL	1(L)	Source connection, Low side
CH/DH	2(H)	Drain connection, High side *
GH	2(H)	Gate connection, High side
EH/SH	2(H)	Source connection, High side

* Connect to each drain terminal with a lead wire or the like.



■Parts list

Symbol	Description	Part No.	Manufacturer	Remark
D301-304	Diode	CMF05	TOSHIBA	Or equivalent
D305,306	Diode	RB050L-60	ROHM	Or equivalent
D307-310	Diode	OPEN		SOD-323
C301,302	Capacitor	OPEN		SMD1608
R301,302	Resistor	8.2 Ω J		SMD3264
R303,304	Resistor	10ΩJ		SMD3264
R305,306	Resistor	47kΩJ		SMD1608
R307,308	Resistor	6.8kΩJ		SMD1608
R309-312	Resistor	OPEN		SMD1608
R313	Resistor	0Ω		SMD2125
JC301,302	Jumper	0Ω		SMD1608
JC303,304	Jumper	OPEN		SMD1608
CN301	Connector	B2(3)B-EH	JST	
CN302	Connector	B12B-ZR-SM4-TF	JST	
MD301	Gate Driver Module	2DM180206CM	TAMURA	

■Mouting Drawing



Parts side





■I/O Condition Table

No	Statua				Input					Out	put	
INO.	No. Status	$V_{\rm 5VDC}$	$\rm V_{\rm OUTH}$	DESAT	XRST	INB	INA	CLAMP	OUT	CLAMP	FLT	RDY
1		0	UVLO	L	Х	Х	Х	Н	L	Hi–Z	Н	L
2	V _{OUTH} UVLO	0	UVLO	L	Х	Х	Х	L	L	L	Н	L
3	VOULH OVEO	0	UVLO	H	Х	Х	Х	Н	L	Hi–Z	L	L
4		0	UVLO	H	Х	Х	Х	L	L	L	L	L
5	DESAT	0	0	H	Х	Х	Х	Н	L	Hi–Z	L	H(*)
6	DLJAI	0	0	Τ	Х	Х	Х	L	L	L	L	H(*)
7	XRST	0	0	L	L	Х	Х	Н	L	Hi–Z	Н	H(*)
8	XI\01	0	0	L	L	Х	Х	L	L	L	Н	H(*)
9		0	0	L	Τ	Н	Х	Н	L	Hi–Z	Н	H(*)
10		0	0	L	Τ	Н	Х	L	L	L	Н	H(*)
11	Normal operation	0	0	L	Н	L	L	Н	L	Hi–Z	Н	H(*)
12		0	0	L	Н	L	L	L	L	L	Н	H(*)
13		0	0	L	Н	L	Н	Х	Н	Hi–Z	Η	H(*)

O : 5VDC or OUT(H) UVLO > UVLO, X : Don't care

(*) If the internal logic of high voltage side doesn't become the expected value, the RDY pin will become "L". And this stage is cleared automatically if the internal logic of high voltage side becomes the expected value.

■Absolute Maximum Ratings

lte	em	Symbol	Min	Max	Unit	Conditions · Note
Input voltage for DC/DC converter		V _{IN}	-0.3	28	Vdc	Between Vin(+) to Vin(-)
Input-side signal voltage		V_{SG}	-0.3	5.2	V	INA, INB, XRST, RDY, FLT
Maximum gate charg	Maximum gate charge		-	600	nC	
Ta=55℃		F _{SW}	-	100	kHz	Test load : 1.4Ω/30nF
Switching frequency	Ta=85℃	F _{SW}	-	35	kHz	
Short circuit detection pin voltage		V_{SD}	0	1000	V	
Maximum gate currer	nt	I _{GPEAK}	-3.5	2.5	А	Guaranteed by design
Input-side signal max	imum current	I _{SG}	-	5	mA	RDY, FLT
Operating temperatur	re range	Τ _{ΟΡ}	-40	85	C°	See the derating curve
Operating humidity		RH _{OP}	20	95	%RH	No condensation
Storage temperature	range	T _{stg}	-40	100	°C	
Storage humidity		RH _{STG}	5	95	%RH	No condensation

Recommended Operating Conditons

ltem	Symbol	Min	Max	Unit	Conditions.Note
Input voltage range for DC/DC converter	V _{IN}	13.5	26.4	Vdc	
Driver circuit number	Ν	-	2	-	
Logic high level input voltage	V_{SGH}	2	5	V	INA, INB ,XRST
Logic low level input voltage	V_{SGL}	0	0.8	V	INA, INB ,XRST
Source current of control signal	I _{SG}	20	-	mA	INA, INB, XRST, V_{SG} =5V
Minimum input pulse width	t _{INMSK}	_	60	ns	





■Ambient Temperature Derating Curve

Reduce the switching frequency according to the following temperature derating table.



■Electrical Specification (Vin=24V, Ta=25°C, Unless otherwise specified)

	Symbol	N 4.				
		Min	Тур	Max	Unit	Conditions · Note
	V_{START}	-	11.5	12.5	V	
	Effi	69	74	-	%	I _{OUTAVE} (CH1,2):100mA
	P _{STBY}	-	0.7	1	W	No load
)		17.5	18.5	19.5	V	$I_{OUTAVE}(CH1) = I_{OUTAVE}(CH2) = 10-130mA$
)	v ₁₊ ,v ₂₊	17.5	18.5	20.5	V	$I_{OUTAVE}(CH1) = I_{OUTAVE}(CH2) = 0-10mA$
)	V ₁₋ ,V ₂₋	-3	-2	-1	V	$I_{OUTAVE}(CH1) = I_{OUTAVE}(CH2) = 0-130mA$
.oad imbalance)	V ₁₊ ,V ₂₊	-	-	25	V	I _{OUTAVE} (CH1):100mA,I _{OUTAVE} (CH2):0mA
.oad imbalance)	V ₁₋ ,V ₂₋	-5	-	-	V	or I _{OUTAVE} (CH1):0mA,I _{OUTAVE} (CH2):100mA
	Symbol	Min	Тур	Max	Unit	Conditions · Note
ogic high level input voltage		2	-	5.2	V	INA, INB ,XRST
: voltage	V_{SGL}	0	-	0.8	V	INA, INB ,XRST
istance	R_{SGD}	-	270	-	Ω	INA, INB ,XRST
ance	R_{SGU}	-	5100	-	Ω	RDY, FLT
ne	t _{INMSK}	-	-	60	ns	INA, INB
e width	t _{XRSTMIN}	800	-	-	ns	
lgih)	V _{OUTH}	-	V _{DCDCOH} -0.5	-	V	No load
_ow)	V _{OUTL}	-	V _{DCDCOL} +0.1	-	V	No load
	Rg(ON)	-	8.2	-	0	
	Rg(OFF)	-	4.5	-	Ω	
се	R _{ONPRO}	0.2	0.5	0.9	Ω	I _{CLAMP} =40mA
urrent	I _{CLAMPL}	3	4.5	_	А	Guaranteed by design
d voltage	V _{CLPON}	V _{OUTL} +1.8	V _{OUTL} +2	V _{OUTL} +2.2	V	Guaranteed by design
ON time	t _{PON}	50	90	130	ns	
OFF time	t _{POFF}	50	90	130	ns	
	voltage istance ance ne width dgih) .ow) ce urrent d voltage ON time) $V_{1+}V_{2+}$) $V_{1-}V_{2-}$ oad imbalance) $V_{1+}V_{2+}$ oad imbalance) $V_{1-}V_{2-}$ Symbol t voltage V_{SGH} t voltage V_{SGL} istance R_{SGD} ance R_{SGD} ance R_{SGD} ance R_{SGU} t V_{NMSK} e width $t_{XRSTMIN}$ Hgih) V_{0UTH} .ow) V_{0UTL} Rg(ON) Rg(OFF) ce R_{ONPRO} urrent I_{CLAMPL} d voltage V_{CLPON} ON time t_{PON}) $V_{1+1}V_{2+}$ $\frac{17.5}{17.5}$) $V_{1-1}V_{2-}$ -3 oad imbalance) $V_{1+1}V_{2+}$ $-$ oad imbalance) $V_{1-1}V_{2-}$ -5 Symbol Min t voltage V_{SGH} 2 voltage V_{SGL} 0 istance R_{SGD} $-$ ance R_{SGD} $-$ ance R_{SGU} $-$ he t_{INMSK} $-$ e width $t_{XRSTMIN}$ 800 Hgih) V_{0UTH} $-$ ce R_{ONPRO} 0.2 urrent I_{CLAMPL} 3 d voltage V_{CLPON} $V_{0UTL}+1.8$ ON time t_{PON} 50) $V_{1+1}V_{2+}$ 17.5 18.5) $V_{1-1}V_{2-}$ -3 -2 oad imbalance) $V_{1+1}V_{2+}$ oad imbalance) $V_{1-1}V_{2-}$ -5 - Symbol Min Typ t voltage V_{SGH} 2 - voltage V_{SGL} 0 - istance R_{SGD} - 270 ance R_{SGD} - 270 ance R_{SGU} - 5100 ne t_{INMSK} e width $t_{XRSTMIN}$ 800 - Hgih) V_{OUTH} - V_{DCDCOH} -0.5 ow) V_{OUTL} - V_{DCDCOH} -0.5 ce R_{ONPRO} 0.2 0.5 urrent I_{CLAMPL} 3 4.5 d voltage V_{CLPON} V_{OUTL} +1.8 V_{OUTL} +2 ON time t_{PON} 50 90) $V_{1+}V_{2+}$ 17.5 18.5 19.5) $V_{1-}V_{2-}$ -3 -2 -1 oad imbalance) $V_{1+}V_{2+}$ 25 oad imbalance) $V_{1-}V_{2-}$ -5 Symbol Min Typ Max t voltage V_{SGH} 2 - 5.2 voltage V_{SGL} 0 - 0.8 istance R_{SGD} - 270 - ance R_{SGD} - 270 - ance R_{SGU} - 60 ance R_{SGU} - 5100 - ne $t_{ NMSK}$ 60 awidth $t_{XRSTMIN}$ 800 - M_{0UTH} - V_{DCDCOH} -0.5 - $M_{G}(OFF)$ - 4.5 - Rg(OFF) - 4.5 - Rg(OFF) - 4.5 - Rg(OFF) - 4.5 - Ce R_{ONPRO} 0.2 0.5 0.9 urrent l_{CLAMPL} 3 4.5 - d voltage V_{CLPON} V_{OUTL} +1.8 V_{OUTL} +2 V_{OUTL} +2.2 ON time t_{PON} 50 90 130) $V_{1+}V_{2+}$ $\frac{17.5}{17.5}$ $\frac{18.5}{18.5}$ $\frac{19.5}{20.5}$ V) $V_{1-}V_{2-}$ -3 -2 -1 V oad imbalance) $V_{1+}V_{2+}$ $ 25$ V oad imbalance) $V_{1-}V_{2-}$ -5 $ -$ V $V_{1-}V_{2-}$ -5 $ V$ $V_{1-}V_{2-}$ -5 $ V$ $V_{1-}V_{2-}$ -5 $ V$ $V_{1-}V_{2-}$ V_{2-} V_{2-} V $V_{2-}V_{2-}$ $V_{2-}V_{2-}$ V $V_{2-}V_{2-}$ $V_{2-}V_{2-}$ V $V_{2-}V_{2-}V_{2-}$ $V_{2-}V_{$



Protection

DC/DC converter block

ltem	Symbol	Min	Тур	Max	Unit	Conditions · Note
Overload protection	-	6	_	-	W	Auto recovery
Overheat protection	-	120	_	150	°C	Internal temperature

Gate drive block

ltem	Symbol	Min	Тур	Max	Unit	Conditions · Note
OUT(H) UVLO OFF voltage	V _{UVLOOHH}	11.3	12.3	13.3	٧	Guaranteed by design
OUT(H) UVLO ON voltage	$V_{\rm UVLOOHL}$	10.3	11.3	12.3	V	Guaranteed by design
Short circuit detection voltage	V_{SD}	-	4.5	-	V	Guaranteed by design
DESAT filter time	$t_{DESATFIL}$	0.16	0.25	0.34	US	Guaranteed by design
DESAT delay time(OUT)	t _{desatout}	0.31	0.38	0.45	us	Guaranteed by design
DESAT delay time(FLT)	t _{desatflt}	0.34	0.42	0.5	US	Guaranteed by design
DESAT low voltage	V_{DESATL}	-	0.1	0.22	V	I _{DESAT} =1mA
DESAT leading edge blanking	t _{DESTLEB}	0.28	0.4	0.52	us	Guaranteed by design
RDY output low voltage	V_{RDYL}	-	0.08	0.15	V	I _{RDY} =5mA
FLT output low voltage	V_{FLTL}	_	0.08	0.15	V	I _{FLT} =5mA

■Insulation

ltem	Specification	Conditions · Note
Between Input-Output	•	·
Dielectric withstand voltage	AC2500V	1min, Cutoff 2mA
Test dielectric withstand voltage	AC2500V	1sec, Cutoff 2mA
Insulation resistance	$100M\Omega$ or more	DC500V
Minimum clearance distances	6mm MIN	
Minimum creepage distances	6mm MIN	
Between Ch1-Ch2	•	·
Dielectric withstand voltage	None	
Test dielectric withstand voltage	None	
Insulation resistance	None	
Minimum clearance distances	5.5mm MIN	
Minimum creepage distances	5.5mm MIN	



■Pin Function

 \cdot Vin(+), Vin(-) (Power supply pin for DC/DC converter)

•GND(Ground pin for drive curcuit)

·INA, INB, XRST(Control input pin, XRST input pin)

The INA, INB and XRST pin is a pin used to determine output logic.

And, holding of the fault signal is canceled by rising of L \rightarrow H of the XRST pin input signal.

XRST	INB	INA	OUT
L	Х	Х	L
Н	Н	Х	L
Н	L	L	L
Н	L	Н	Н

$\cdot \mathsf{FLT}(\mathsf{Fault} \ \mathsf{output} \ \mathsf{pin})$

The FLT pin is an open drain pin used to output a fault signal when desaturation function is activated, and will be cleared at the rising edge of FLT.

Status			
While in normal operation	Н		
When desaturation function is activated	L		

·RDY(Ready output pin)

The RDY pin shows the status of three internal protection features which are 5VDC UVLO, OUT(H) UVLO, and output state

feedback (OSFB). The term 'output state feedback' shows whether output internal logic is high or low corresponds to input logic or not.

Status			
While in normal operation			
5VDC UVLO or OUT(H) UVLO or Output internal logic feedback	L		

·CL/DL(Low side MOSFET Drain connection pin)

 $\ensuremath{\mathsf{CL}}\xspace/\ensuremath{\mathsf{DL}}\xspace$ is a land to be connected to the low side MOSFET drain of the power device.

·GL(Low side MOSFET Gate connection pin)

GL is a land to be connected to the low side MOSFET gate of the power device.

•EL/SL(Low side MOSFET Source connection pin)

 $\ensuremath{\mathsf{EL/SL}}$ is a land to be connected to the low side MOSFET source of the power device.

·CH/DH(High side MOSFET Drain connection pin)

CH/DH is a land to be connected to the high side MOSFET drain of the power device.

·GH(High side MOSFET Gate connection pin)

GH is a land to be connected to the high side MOSFET gate of the power device.

•EH/SH(Low side MOSFET Source connection pin)

EH/SH is a land to be connected to the high side MOSFET source of the power device.





Description Of Protection

1. Gate voltage rise prevention function

If OUT=L and the CLAMP pin voltage < VCLPON, the internal MOSFET of the CLAMP pin turns on.

OUT	CLAMP	Internal MOSFET of the CLAMP pin
L	Less than V_{CLPON}	ON
L	Not less than $V_{\mbox{\tiny CLPON}}$	OFF
Н	Х	OFF



Timing chart of Miller clamp function

2. Undervoltage Lockout (UVLO) function

The control circuit incorporates the undervoltage lockout (UVLO) function both on the OUT(H) sides. When the OUT(H) voltage drops to the UVLO ON voltage, the OUT pin and the RDY pin both will output the "L"signal. When the OUT(H) voltage rises to the UVLO OFF voltage, these pins will be reset. To prevent malfunctions due to noises, mask time $t_{UVLO1MSK}$ and $t_{UVLO2MSK}$ are set on both input and output sides.

3. Desaturation protection function(DESAT), Fault signal output function

When the DESAT pin voltage exceeds VDESAT, the DESAT function will be activated.

When the DESAT function is activated, the OUT pin voltage will be set to the "L" level, and then the FLT pin voltage to the "L" level. When the rising edge is put in the XRST pin, the DESAT function will be released.





■Reliability

ltem	Test condition and acceptance criterion			
Exposure in high temperature	100℃, 240H, ※			
Exposure in low temperature	−40°C, 240H, ※			
Exposure in high temperature and high humidity	60℃, 90~95%RH, 240H, ※			
Thermal shock	-40°C/30min to 100°C/30min, 500cycles, ※			
Low temperature operation	Input voltage:DC24V, Output current:Rated Load			
	-40°C, 240H,			
High temperature operation	Input voltage:DC24V, Output current:Rated Load			
	85°C, 240H, 💥			
high temperature	Input voltage:DC24V, Output current:Rated Load			
and high humidity operation	60°C, 90∼95%RH, 240H,			
Vibration	Vibration amplitude:1.5mm(peak to peak), Vibration Frequency:10 to 55Hz, Sweeping:1min.			
	In each X, Y and Z direction:once, 120min. 💥			
Impact	Acceleration:490m/s ² (50G), Operating time:11ms			
	In each \pm X, Y and Z direction:3 times, $$ $$			

% After each test, exposure at room temperature and humidity condition for 24 hours.

There shall be no abnormality on the electrical specification and appearance.



2DU180206MR01 Datasheet

■Outline Dimensional Drawing





■Product Weight 89g(TYP)



2DU180206MR01 Datasheet

Recommended Soldering Condition

 $\cdot \, \text{Soldering}$ condition of hand work

: 350°C(MAX) Less than 4sec

■Storage Conditions

ltem	Min	Max	Unit	Conditions · Note
Storage temperature	-25	60	°C	A packing state

%If you want to use past the long period there is a concern that the solder non-wetting by terminal oxidation to occur. Therefore, please use from taking enough tests.

■Usage Cautions

- Always mount fuse on the plus side of input for ensuring safety because the fuse is not built-in the product.
 Please select the fuse considering conditions such as steady current, inrush current, and ambient temperature.
 When using a fuse having large rated current or high capacity input electrolytic condenser, by combining another converter and input line and input electrolytic condenser, fuse may not blow off in the case of abnormality.
 Do not combine high voltage line and fuse.
- This product is designed to be best when it drives two devices to have the same gate capacitance simultaneously.
 Because it leads to the "output unstable" and "output accuracy deterioration".
 If you want to use to drive only one of the devices, because of the output voltage accuracy deterioration prevention, please configure the dummy gate circuit (resistor and capacitor) to consume the equivalent of the power and the drive side.
- This product is to transmit the signal of the insulating part by the magnetic coupling.
 Therefore, if you use this product in a strong magnetic field in, there is a possibility of malfunction.
 In that case, connect the capacitor between the GND terminal of this product and a metal enclosure.
- Make sure the rise/fall time of the input signal is 500ns or less.
- Please confirm with the device supplier for the detail such as the screw type, material, torque force that tighten to device.



■Important Notice

- The content of this information is subject to change without prior notice for the purpose of improvements, etc. Ensure that you are in possession of the most up-to-date information when using this product.
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- The circuit examples and part constants listed in this document are provided as reference for the verification of characteristics. You are to perform design, verification, and judgment at your own responsibility, taking into account the various conditions.
- TAMURA has evaluated the efficiency and performance of this product in a usage environment determined by us.
 Depending on your usage environment or usage method, there is the possibility that this product will not perform sufficiently as shown in the specifications, or may malfunction.
 When applying this product to your devices or systems, please ensure that you conduct evaluations of their state when integrated with this product. You are responsible for judging its applicability.
 TAMURA bears no responsibility whatsoever for any problems with your devices,

systems or this product which are caused by your usage environment or usage method.

- TAMURA Corporation constantly strives to improve quality and reliability, but malfunction or failures are bound to occur with some probability in power products. To ensure that failures do not cause accidents resulting in injury or death, fire accidents, social damage, and so on, you are to thoroughly verify the safety of their designs in devices and/or systems, at your own responsibility.
- This product is intended for use in consumer electronics (electric home appliances, business equipment, Information equipment, communication terminal equipment, measuring devices, and so on.) If considering use of this product in equipment or devices that require high reliability (medical devices, transportation equipment, traffic signal control equipment, fire and crime prevention equipment, aeronautics and space devices, nuclear power control, fuel control, in-vehicle equipment, safety devices, and so on), please consult a TAMURA sales representative in advance. Do not use this product for such applications without written permission from TAMURA Corporation.
- This product is intended for use in environments where consumer electronics are commonly used. It is not designed for use in special environments such as listed below, and if such use is considered, you are to perform thorough safety and reliability checks at your own responsibility.
 - Use in liquids such as water, oil, chemical solutions, or organic solvents, and use in locations where the product will be exposed to such liquids.
 - · Use that involves exposure to direct sunlight, outdoor exposure, or dusty conditions.
 - · Use in locations where corrosive gases such as salt air, C12, H2S, NH3, SO2, or NO2, are present.
 - · Use in environments with strong static electricity or electromagnetic radiation.
 - · Use that involves placing inflammable material next to the product.
 - Use of this product either sealed with a resin filling or coated with resin.
 - Use of water or a water soluble detergent for flux cleaning.
 - · Use in locations where condensation is liable to occur.
- This product is not designed to resist radiation.
- This product is not designed to be connected in series or parallel.
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