74ALVC16836A

20-bit registered driver with inverted register enable; 3-state

Rev. 2 — 12 September 2018 Product data sheet

1. General description

The 74ALVC16836A is a 20-bit universal bus driver. Data flow is controlled by active low output enable ($\overline{OE}$), active low latch enable ($\overline{LE}$) and clock inputs (CP).

When $\overline{LE}$ is LOW, the A to Y data flow is transparent. When $\overline{LE}$ is HIGH and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

When $\overline{OE}$ is LOW the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip-flop.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines at 85°C
- Input diodes to accommodate strong drivers
- Complies with JEDEC standard no. 8-1A
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC16836ADGG	−40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

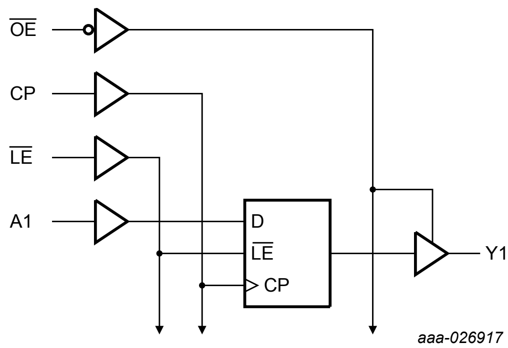


Fig. 1. Logic diagram

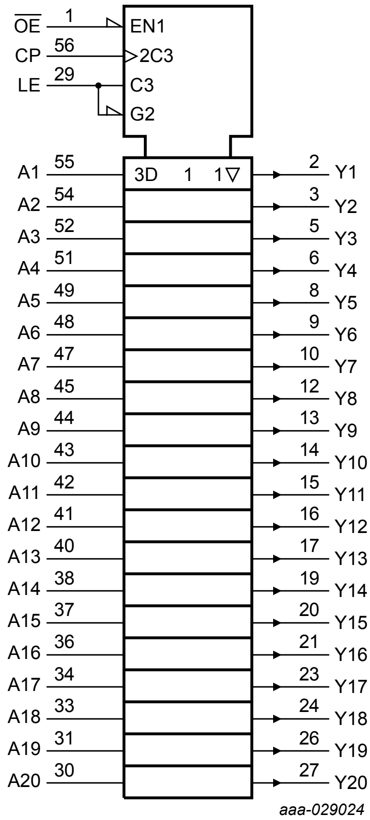


Fig. 2. Logic symbol (IEEE/IEC)

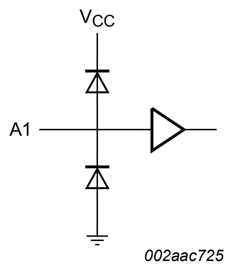


Fig. 3. Typical input (data or control)

5. Pinning information

5.1. Pinning

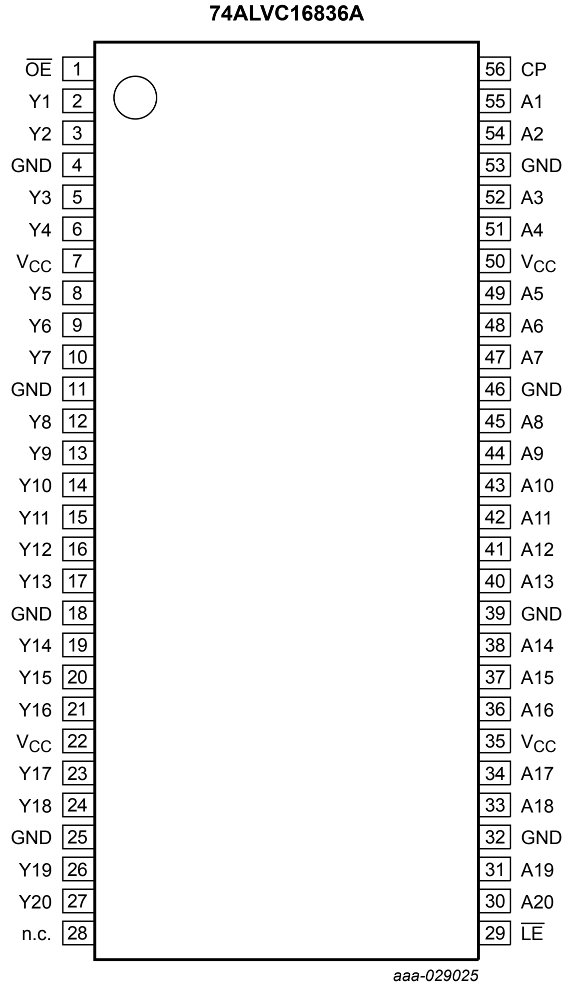


Fig. 4. Pin configuration TSSOP56 (SOT364-1)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20	55, 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31, 30	data inputs
Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18, Y19, Y20	2, 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26, 27	data outputs
n.c.	28	no connection
$\overline{LE}$	29	latch enable input (active LOW)
$\overline{OE}$	1	output enable input (active LOW)
CP	56	clock input (LOW-to-HIGH, edge-triggered)
GND	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function table [1]

Input				Output
$\overline{OE}$	$\overline{LE}$	CP	An	Yn
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y_0 [2]
L	H	L	X	Y_0 [3]

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state;
↑ = LOW-to-HIGH clock transition.

[2] Y_0 = Output level before the indicated steady-state input conditions were established, provided that CP is high before $\overline{LE}$ goes low.

[3] Y_0 = Output level before the indicated steady-state input conditions were established.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	For control inputs	[1]	-0.5	+4.6	V
		For data inputs	[1]	-0.5	V_{CC} + 0.5	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
$I_{O\ (sink/source)}$	output sink or source current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For TSSOP56 package: P_{tot} derates linearly with 8 mW/K above 55 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		V_{CC} = 2.5 V; C_L = 30 pF	2.3	-	2.7	V
		V_{CC} = 3.3 V; C_L = 50 pF	3.0	-	3.6	V
		LOW-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	operating in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.3 V to 3.6 V; I_O = -100 μA	V_{CC} - 0.2	V_{CC}	-	V
		V_{CC} = 2.3 V; I_O = -6 mA	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		V_{CC} = 2.3 V; I_O = -12 mA	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		V_{CC} = 2.7 V; I_O = -12 mA	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		V_{CC} = 3.0 V; I_O = -12 mA	V_{CC} - 0.6	V_{CC} - 0.09	-	V
		V_{CC} = 3.0 V; I_O = -24 mA	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.3 V to 3.6 V; I_O = 100 μA	-	GND	0.20	V
		V_{CC} = 2.3 V; I_O = 6 mA	-	0.07	0.40	V
		V_{CC} = 2.3 V; I_O = 12 mA	-	0.15	0.70	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	0.14	0.40	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	0.27	0.55	V
I_I	input leakage current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	5	μA
I_{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	10	μA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	40	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	150	750	μA
C_I	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance		-	8.0	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V

10. Dynamic characteristics

Table 7. Dynamic characteristics

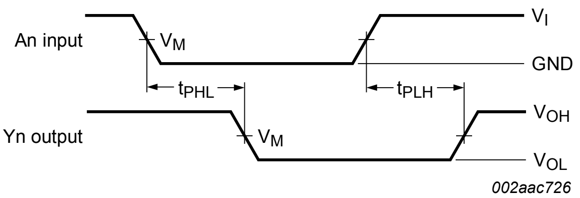
Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 11.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
t_{pd}	propagation delay	An to Yn; see Fig. 5	[2]				
		V_{CC} = 2.3 V to 2.7 V		1.0	2.4	4.2	ns
		V_{CC} = 2.7 V		1.3	2.7	4.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	2.3	3.6	ns
		$\overline{LE}$ to Yn; see Fig. 6					
		V_{CC} = 2.3 V to 2.7 V		1.3	2.8	4.5	ns
		V_{CC} = 2.7 V		1.3	2.8	4.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.6	4.2	ns
		CP to Yn; see Fig. 8					
		V_{CC} = 2.3 V to 2.7 V		1.4	2.8	5.0	ns
		V_{CC} = 2.7 V		1.3	2.7	4.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.5	4.2	ns
t_{en}	enable time	$\overline{OE}$ to Yn; see Fig. 10	[3]				
		V_{CC} = 2.3 V to 2.7 V		1.4	2.2	4.0	ns
		V_{CC} = 2.7 V		1.4	3.0	4.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.1	2.3	4.4	ns
t_{dis}	disable time	$\overline{OE}$ to Yn; see Fig. 10	[4]				
		V_{CC} = 2.3 V to 2.7 V		1.4	2.0	4.5	ns
		V_{CC} = 2.7 V		1.4	3.1	4.3	ns
		V_{CC} = 3.0 V to 3.6 V		1.3	2.8	4.3	ns
t_W	pulse width	CP HIGH or LOW; V_{CC} = 2.3 V to 3.6 V; see Fig. 8		2.0	-	-	ns
		$\overline{LE}$ HIGH; V_{CC} = 2.3 V to 3.6 V; see Fig. 6		2.0	-	-	ns
t_{su}	set-up time	An to CP; V_{CC} = 2.3 V to 3.6 V; see Fig. 9		1.0	-	-	ns
		An to $\overline{LE}$; V_{CC} = 2.3 V to 3.6 V; see Fig. 7		1.5	-	-	ns
t_h	hold time	An to CP; see Fig. 9					
		V_{CC} = 2.3 V to 2.7 V		0.6	0.2	-	ns
		V_{CC} = 2.7 V		0.6	0.3	-	ns
		V_{CC} = 3.0 V to 3.6 V		0.9	0.3	-	ns
		An to $\overline{LE}$; see Fig. 7					
		V_{CC} = 2.3 V to 2.7 V		1.4	0.4	-	ns
		V_{CC} = 2.7 V		1.7	0.4	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.4	0.3	-	ns
f_{max}	maximum frequency	CP; see Fig. 8					
		V_{CC} = 2.3 V to 2.7 V		150	300	-	MHz
		V_{CC} = 2.7 V		200	350	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	300	-	MHz

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[5]				
		transparent mode; output enabled		-	13	-	pF
		transparent mode; output disabled		-	3	-	pF
		clocked mode; output enabled		-	22	-	pF
		clocked mode; output disabled		-	15	-	pF

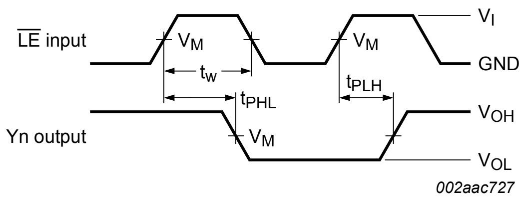
[1] Typical values are measured at T_{amb} = 25 °C
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] t_{en} is the same as t_{PZH} and t_{PZL}.
[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



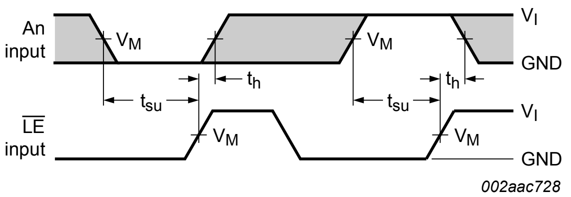
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Input (An) to output (Yn) propagation delay



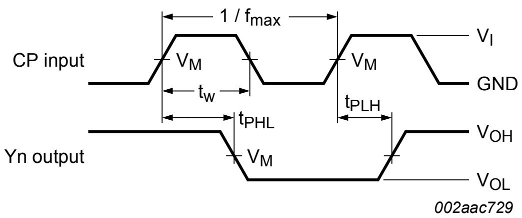
Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. $\overline{LE}$ input pulse width, $\overline{LE}$ input to Yn output propagation delays



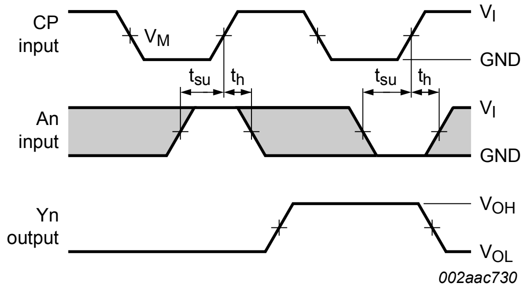
Measurement points are given in Table 8.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Data set-up and hold times, An input to $\overline{LE}$ input



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. CP input to Yn output propagation delays, clock pulse width and maximum clock frequency

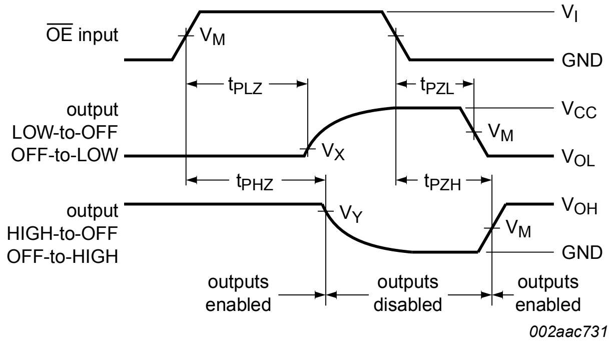


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 9. Data set-up and hold times, An input to CP input



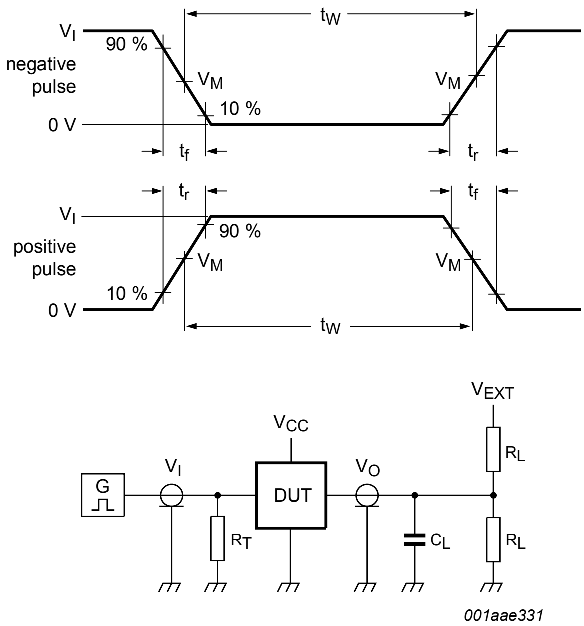
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 10. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
≤ 2.3 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

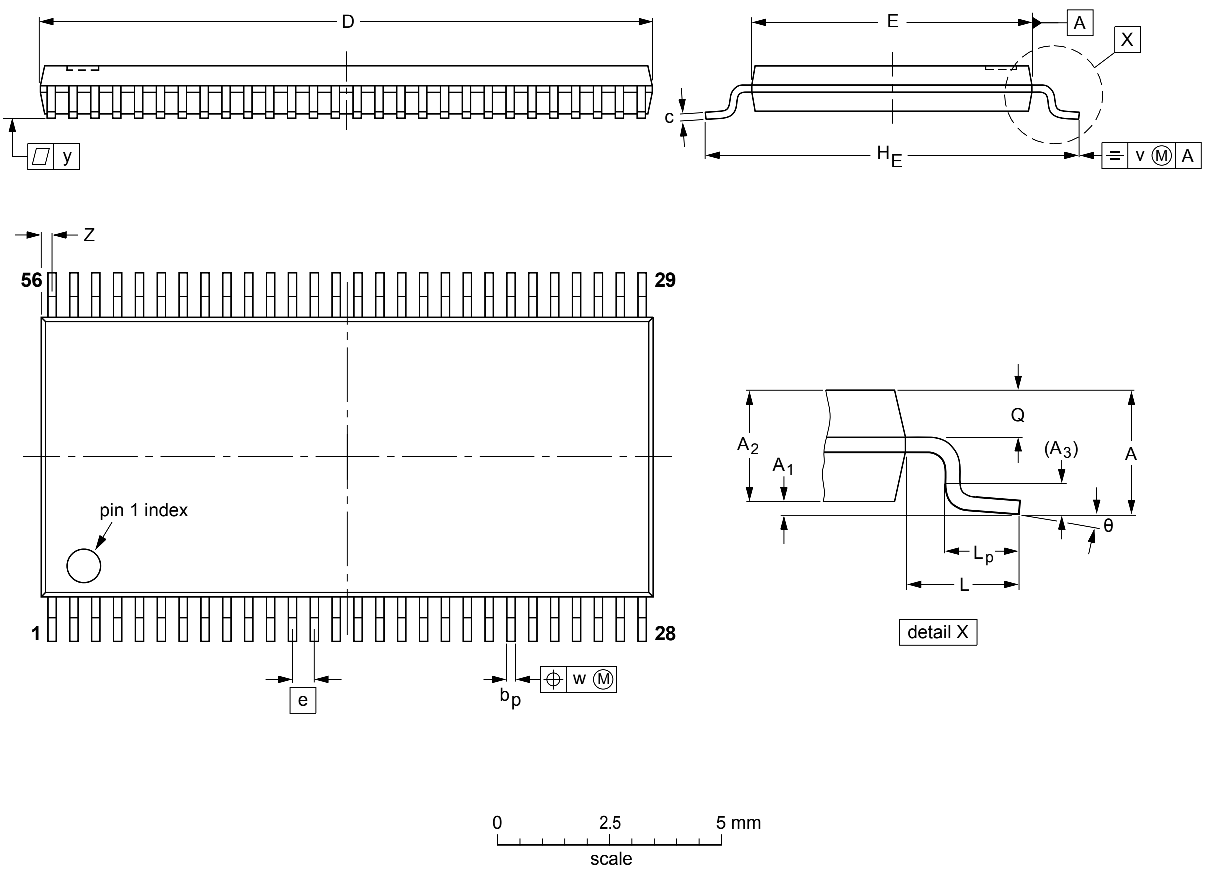
Fig. 11. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
≤ 2.3 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 12. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC16836A v.2	20180912	Product data sheet	-	74ALVC16836A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVC16836A v.1	20000314	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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