



# MX575ANS200M000

## Ultra-low Jitter 200MHz LVDS XO

### ClockWorks™ FUSION

### General Description

The MX575ANS200M000 is an ultra-low phase jitter XO with LVDS output optimized for high line rate applications.

### Features

- 200MHz LVDS
- Typical phase noise:
  - 100fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

### Absolute Maximum Ratings

Supply Voltage (VIN).....+3.6V  
 Lead Temperature (soldering, 10s).....260°C  
 Storage Temperature (T<sub>s</sub>).....125°C  
 ESD Rating (HBM).....2kV

### Operating Ratings

Supply Voltage (VIN).....+2.375V to +3.63V  
 Ambient Temperature (TA).....-40°C to +85°C

### Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 100 Ohms between Q and /Q.<sup>1</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				90	mA
F0	Center Frequency			200		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		220 100		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time				300	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage VOH max = VCM max + 1/2 VOD max	LVDS output levels	1.248	1.375	1.602	V
VOL	Output Low Voltage VOL min = VCM min - 1/2 VOD max	LVDS output levels	0.898	1.025	1.252	V
VOD	Output Differential Voltage		247	350	454	mV
VCM	Common Mode Output Voltage		1.125	1.2	1.375	V

#### Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.

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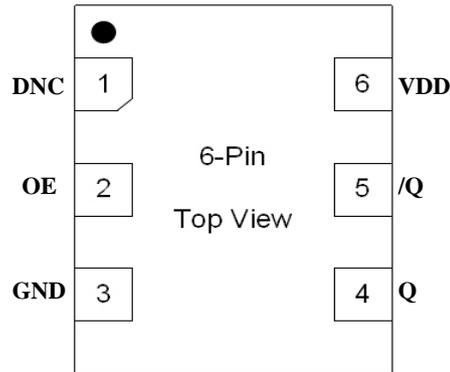
Revision 1.0  
[tcghelp@micrel.com](mailto:tcghelp@micrel.com) or (408) 955-1690

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX575ANS200M000	MX575AN	S200M000	Tube	6-Pin 7mm x 5mm LGA
MX575ANS200M000 TR	MX575AN	S200M000	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

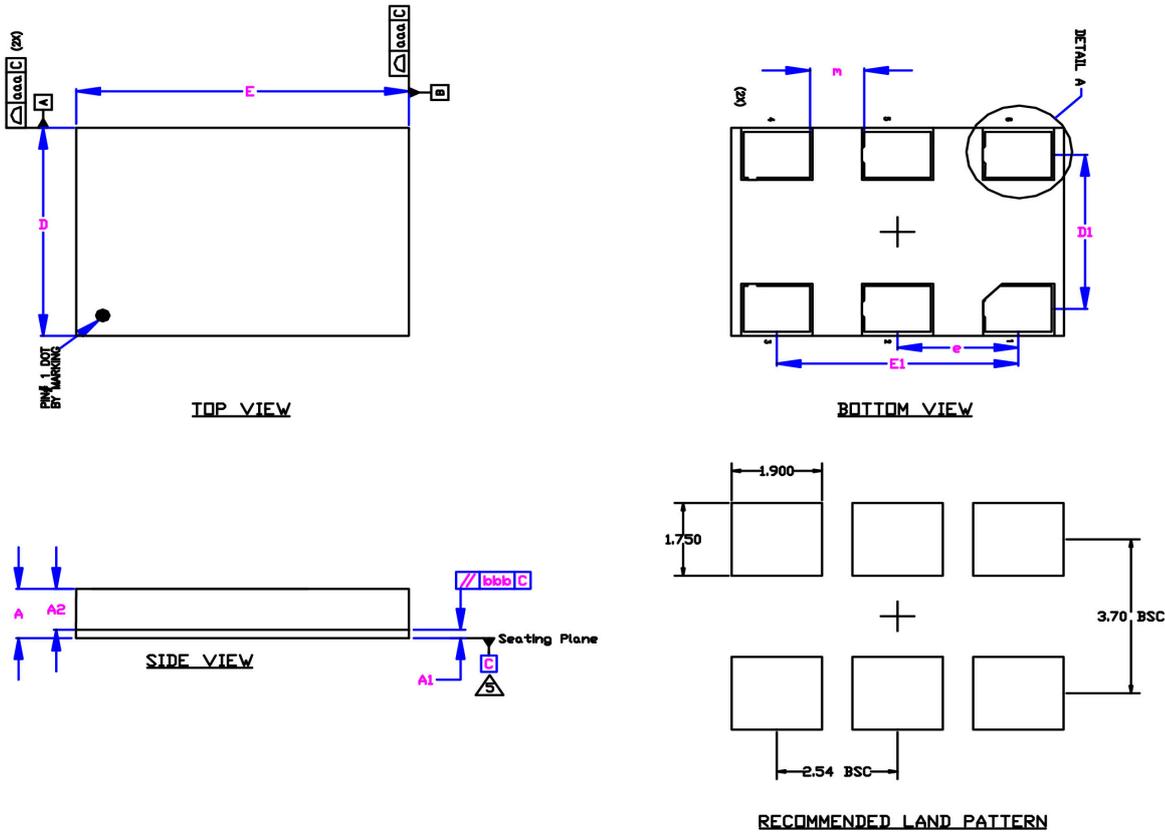
## Pin Configuration



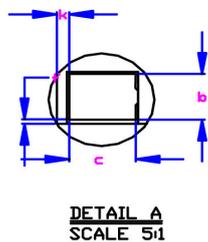
## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	DNC			Make no connection, leave floating.
2	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVDS	Clock Output Frequency = 200MHz
6	VDD	PWR		Power Supply

# Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



Dimensional Tol.			
aaa			0.10
bbb			0.07
Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.26	1.33	1.40
A1	0.19	0.23	0.27
A2	1.070	1.100	1.130
D	4.9	5.0	5.1
D1		3.7	BSC
E	6.9	7.0	7.1
E1		5.0	BSC
b	0.15	0.18	0.21
c	1.35	1.4	1.45
e		2.54	BSC
f	0.15	0.18	0.21
k	0.21	0.26	0.31
m	1.19	1.14	1.19
n		36	



- Notes
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
  2. Dimensions are in millimeters.
  3. 'e' represents the basic LGA pitch
  4. 'n' is the maximum no. of Land for a specified Package.
  5. Package warp shall be 0.05 max.
  6. Substrate base is BT Resin
  7. The Pin#1 corner must be identified on top side only.
  8. Reference Jeduc Spec M1-22
  9. Land pattern tolerance is 0.05mm unless otherwise specified

### 6-Pin LGA (7x5mm)

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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