



## **High-Speed Quad Monolithic SPST CMOS Analog Switch**

#### **DESCRIPTION**

The DG271B high speed quad single-pole single-throw analog switch is intended for applications that require low on-resistance, low leakage currents, and fast switching speeds.

Built on the Vishay Siliconix' proprietary high voltage silicon gate process to achieve superior on/off performance, each switch conducts equally well in both directions when on, and blocks up to the supply voltage when off. An epitaxial layer prevents latchup.

The DG271B has a redesign internal regulator which improves start-up over the DG271.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

#### **FEATURES**

Fast switching t<sub>ON</sub>: 55 ns
Low charge injection: 5 pC

Low r<sub>DS(on)</sub>: 32 Ω

• TTL/CMOS compatible

Low leakage: 50 pA

# Pb-free Available

RoHS

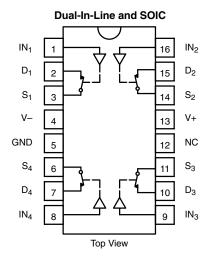
#### **BENEFITS**

- · Fast settling times
- Reduced switching glitches
- · High precision

#### **APPLICATIONS**

- · High-speed switching
- Sample/hold
- · Digital filters
- · Op amp gain switching
- · Flight control systems
- · Automatic test equipment
- Choppers
- · Communication systems

#### **FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION**



TRUTH TABLE				
Logic	Switch			
0	ON			
1	OFF			

 $\begin{array}{l} \text{Logic "0"} \leq 0.8 \ V \\ \text{Logic "1"} \geq 2.4 \ V \end{array}$ 

<sup>\*</sup> Pb containing terminations are not RoHS compliant, exemptions may apply.

## Vishay Siliconix



ORDERING INFORMATION			
Temp. Range	Package	Part Number	
0 °C to 70 °C	16-Pin Plastic DIP	DG271BCJ-E3	
- 40 °C to 85 °C	16-Pin Narrow SOIC	DG271BDY-E3	
		DG271BDY-T1-E3 (with Tape and Reel)	

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter		Limit	Unit	
V+ to V-		44		
GND to V-		25	V	
Digital Inputs <sup>a</sup> V <sub>S</sub> , V <sub>D</sub>		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	V	
Current, Any Terminal		30	mA	
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	IIIA	
Storage Temperature	(DY Suffix)	- 65 to 150	°C	
	(CJ Suffix)	- 65 to 125		
Davier Dissipation (Pages as)b	16-Pin Plastic DIP <sup>c</sup>	470	mW	
Power Dissipation (Package) <sup>b</sup>	16-Pin Plastic Narrow SOIC <sup>d</sup>	600	11177	

#### Notes:

- a. Signals on  $S_X$ ,  $D_X$ , or  $IN_X$  exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings. b. All leads welded or soldered to PC board.
- c. Derate 6.5 mW/°C above 75 °C.
- d. Derate 7.6 mW/°C above 75 °C.





SPECIFICATIONS <sup>a</sup>							
		Test Conditions Unless Specified V+ = 15 V, V- = - 15 V		<b>C</b> , D 0 °C - 40 °C		°C	
Parameter	Symbol	$V_{IN} = 2.4 \text{ V}, 0.8 \text{ V}^{f}$	Temp.a	Min.d	Typ.c	Max. <sup>d</sup>	Unit
Analog Switch	<del>-</del>		<u> </u>	Į.		I.	
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		Full	- 15		15	٧
Drain-Source On-Resistance	r <sub>DS(on)</sub>	$I_S = 1 \text{ mA}, V_D = \pm 10 \text{ V}$	Room Full		32	50 75	Ω
Switch Off Leakage Current	I <sub>S(off)</sub>	$V_D = \pm 14 \text{ V}, V_S = \pm 14 \text{ V}$	Room Full	- 1 - 20	± 0.05	1 20	
Owner on Leakage outlent	I <sub>D(off)</sub>	VD = ± 14 V, VS = ± 14 V	Room Full	- 1 - 20	± 0.05	1 20	nA
Channel On Leakage Current	I <sub>D(on)</sub> + I <sub>S(on)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	Room Full	- 1 - 20	± 0.05	1 20	
Digital Control	<u> </u>			I.		l.	
Input Current with Voltage High	I <sub>INH</sub>	V <sub>IN</sub> = 2 V	Full	- 1	0.010	1	
input Current with voltage riigh	INH	V <sub>IN</sub> = 15 V	Full	- 1	0.010	1	μΑ
Input Current with Voltage Low	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	Full	- 1	0.010	1	
Dynamic Characteristics	_						
Turn-On Time	t <sub>ON</sub>	V <sub>S</sub> = ± 10 V	Room Full		55	65 80	ns
Turn-Off Time	t <sub>OFF</sub>	See Figure 3	Room Full		50	65 80	
Charge Injection	Q	$C_L = 1 \text{ nF, } V_S = 0 \text{ V, } V_{gen} = 0 \text{ V, } R_{gen} = 0 \Omega$ See Figure 3	Room		- 5		pC
Source-Off Capacitance	C <sub>S(off)</sub>	V <sub>S</sub> = 0 V, V <sub>IN</sub> = 5 V	Room		8		
Drain-Off Capacitance	C <sub>D(off)</sub>	f = 1 MHz	Room		8		pF
Channel On Capacitance	C <sub>D(on)</sub>	$V_D = V_S = 0 \text{ V}, V_{IN} = 0 \text{ V}$	Room		30		
Off-Isolation	OIRR	$C_L = 10 \text{ pF, } R_L = 1 \text{ k}\Omega$	Room		85		dB
Crosstalk	X <sub>TALK</sub>	f = 100 kHz, See Figures 4 and 5	Room		100		uБ
Power Supply							
Positive Supply Current	l+	All Channels On or Off	Room Full		5.5	7.5 9	mA
Negative Supply Current	l-	V <sub>IN</sub> = 5 V or 0 V	Room Full	- 6 - 8	- 3.4		1117 (

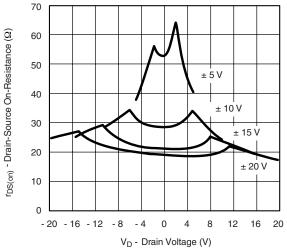
#### Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25  $^{\circ}$ C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.

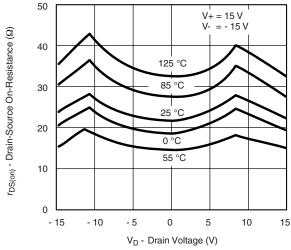
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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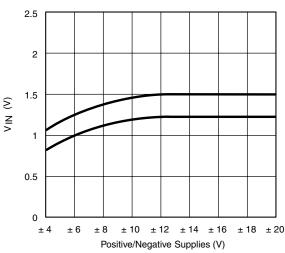
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



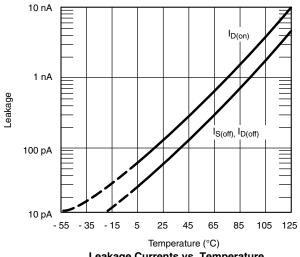
 $r_{DS(on)}$  vs.  $V_D$  and Power Supply Voltages



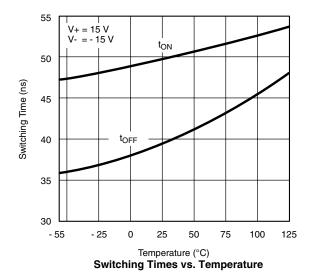
r<sub>DS(on)</sub> vs. V<sub>D</sub> and Temperature



Input Switching Threshold vs. Supply Voltage



Leakage Currents vs. Temperature



55 50 Switching Time (ns) 45  $t_{ON}$ 40 35 30 ± 4 ± 6 ± 8 ± 10 ± 12 ±14 ±16 ±18 ±20

Supply Voltage (V) Switching Time vs. Power Supply Voltage



#### **SCHEMATIC DIAGRAM** Typical Channel

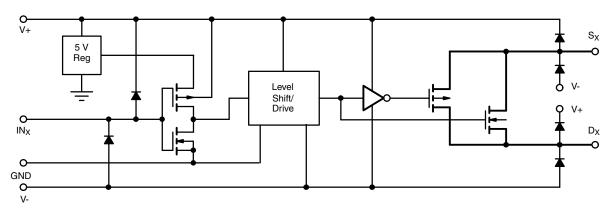


Figure 1.

#### **TEST CIRCUITS**

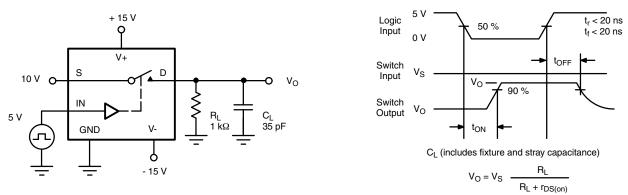
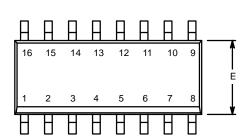


Figure 2. Switching Time

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?70966">http://www.vishay.com/ppg?70966</a>.

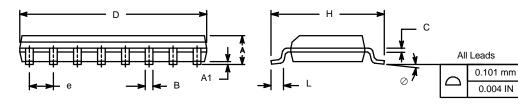


SOIC (NARROW): 16-LEAD JEDEC Part Number: MS-012



	MILLIMETERS		INC	HES	
Dim	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.38	0.51	0.015	0.020	
С	0.18	0.23	0.007	0.009	
D	9.80	10.00	0.385	0.393	
Е	3.80	4.00	0.149	0.157	
е	1.27 BSC		0.050	BSC	
Н	5.80	6.20	0.228	0.244	
L	0.50	0.93	0.020	0.037	
0	0°	8°	0°	8°	
ECN: S-03946—Rev. F, 09-Jul-01					

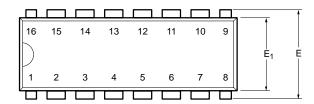
DWG: 5300

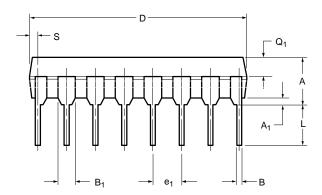


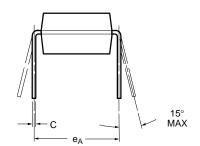
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PDIP: 16-LEAD





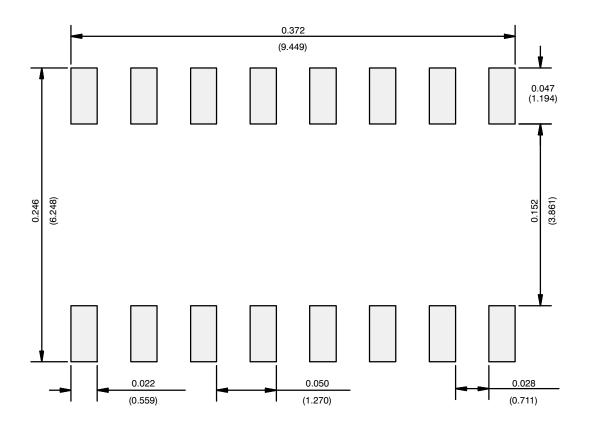


	MILLIMETERS		INC	HES	
Dim	Min	Max	Min	Max	
Α	3.81	5.08	0.150	0.200	
A <sub>1</sub>	0.38	1.27	0.015	0.050	
В	0.38	0.51	0.015	0.020	
B <sub>1</sub>	0.89	1.65	0.035	0.065	
С	0.20	0.30	0.008	0.012	
D	18.93	21.33	0.745	0.840	
Е	7.62	8.26	0.300	0.325	
E <sub>1</sub>	5.59	7.11	0.220	0.280	
e <sub>1</sub>	2.29	2.79	0.090	0.110	
e <sub>A</sub>	7.37	7.87	0.290	0.310	
L	2.79	3.81	0.110	0.150	
$Q_1$	1.27	2.03	0.050	0.080	
S	0.38	1.52	.015	0.060	
ECN: S-03946—Rev. D, 09-Jul-01					

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#### **RECOMMENDED MINIMUM PADS FOR SO-16**



Recommended Minimum Pads Dimensions in Inches/(mm)

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