EVBUM2275/D

KAI-2001 / KAI-2020 / KAI-2093 Imager Board User's Manual

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EVAL BOARD USER'S MANUAL

Description

The KAI−2001/KAI−2020/KAI−2093 Imager Evaluation Board, referred to in this document as the Imager Board, is designed to be used as part of a two−board set, used in conjunction with a Timing Generator Board. ON Semiconductor offers an Imager Board / Timing Generator Board package that has been designed and configured to operate with the KAI−2001, KAI−2020, and KAI−2093 Image Sensors.

The Timing Generator Board generates the timing signals necessary to operate the CCD, and provides the power required by the Imager Board. The timing signals, in LVDS format, and the power, are provided to the Imager Board via the interface connector (J4). In addition, the Timing Generator Board performs the processing and digitization of the analog video output of the Imager Board.

The Imager Board has been designed to operate KAI−2001, KAI−2020, and KAI−2093 with the specified performance at nominal operating conditions. (See the appropriate performance specifications for details).

For testing and characterization purposes, the Imager Board provides the ability to adjust many of the CCD bias voltages and CCD clock level voltages by adjusting potentiometers on the board. The Imager Board provides the means to modify other device operating parameters (e.g., CCD reset clock pulse width) by populating components differently on the board.

Some circuitry on the Imager Board (e.g., remote DAC control of bias and clock level voltages) is intended for ON Semiconductor test purposes only, and may not be populated.

INPUT REQUIREMENTS

Table 1. POWER REQUIREMENTS

Power Supplies	Minimum	Typical	Maximum	Units
+5 V_MTR Supply	4.9	5.0	5.1	V
		800		mA
−5 V_MTR Supply	−5.1	−5.0	−4.9	V
		200		mA
VPLUS Supply	18	20	21	V
		250		mA
VMINUS Supply	−21	−20	−18	V
		250		mA

Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Signal	Comments
IMAGER_IN0	0	±0.1	2.4	V	AMP_ENABLE	Output Amplifier Enable
IMAGER_IN1	0	±0.1	2.4	V	H1A	H1A clock
IMAGER_IN2	0	±0.1	2.4	V	H1B	H1B clock
IMAGER_IN3	0	±0.1	2.4	V	H2A	H2A clock
IMAGER_IN4	0	±0.1	2.4	V	H2B	H2B clock
IMAGER_IN5	0	±0.1	2.4	V	RESET	Reset clock
IMAGER_IN6	0	±0.1	2.4	V	V1	V1 clock

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Table 2. SIGNAL LEVEL REQUIREMENTS

Input Signals (LVDS)	V_{min}	$V_{threshold}$	V_{max}	Units	Signal	Comments
IMAGER_IN7	0	±0.1	2.4	V	V2	V2 clock
IMAGER_IN8	0	±0.1	2.4	V		(not used)
IMAGER_IN9	0	±0.1	2.4	V	V3RD	V2 Clock 3rd level
IMAGER_IN10	0	±0.1	2.4	V	FDG	Fast Dump clock
IMAGER_IN11	0	±0.1	2.4	V	VES	Electronic Shutter clock

ARCHITECTURE OVERVIEW

The following sections describe the functional blocks of the Imager Board (Refer to Figure 1).

Power Filtering and Regulation

Power is supplied to the Imager Board via the J4 interface connector. The power supplies are de−coupled and filtered with ferrite beads and capacitors to suppress noise. Voltage regulators are used to create the +15 V and –15 V supplies from the VPLUS and VMINUS supplies.

LVDS Receivers / TTL Buffers

LVDS timing signals are input to the Imager Board via the J4 interface connector. These signals are shifted to TTL levels before being sent to the CCD clock drivers.

CCD Pixel−Rate Clock Drivers (H1, H2 & Reset Clocks)

The pixel rate CCD clock drivers utilize two fast switching transistors that are designed to translate TTL−level input clock signals to the voltage levels required by the CCD. The high level and low levels of the CCD clocks are set by potentiometers, and are buffered by operational amplifiers configured as voltage followers.

Reset Clock One−Shot

The pulse width of the RESET_CCD clock may be set by U13, a programmable One−Shot. The One−Shot can be configured to provide a RESET_CCD clock signal with a pulse width from 5 ns to 15 ns. If pulse width control functionality is provided by the Timing Board, the One−Shot may be removed and bypassed by installing R147.

CCD VCLK Drivers

The vertical clock (VCLK) drivers consist of MOSFET driver IC’s. These drivers are designed to translate the TTL−level clock signals to the voltage levels required by the CCD. The high, middle, and low voltage levels of the vertical clocks are set by potentiometers buffered by operational amplifiers. The VHIGH and VLOW op−amps have a gain of 1.25, to allow the magnitude of the voltages to be adjusted to 12.5 V when using DAC control.

The current sources for these voltage levels are high current (up to 600 mA) transistors. The V2_CCD high level clock voltage is switched from V_MID to V_HIGH once per frame to transfer the charge from the photodiodes to the vertical CCDs.

The V1 clock driver is a 2−level driver circuit, switching between VMID and VLOW voltage levels.

CCD FDG Driver

The Fast Dump clock drivers consist of a transistor that will switch the voltage on the FD pin of the CCD from FDG_LOW to FDG_HIGH during Fast Dump Gate operations. When not in operation, or when the Fast Dump Gate feature is not being utilized, the FDG pin of the CCD is held at FDG_LOW. The FDG_HIGH and FDG_LOW voltage levels of the FDG driver are set by potentiometers, buffered by operational amplifiers configured as voltage followers. The KAI−2093 image sensor does not have the Fast Dump Gate feature. To support this device, the Imager Board must be configured so that the CCD pin 11 is 0.0 V. To accomplish this, R91 is removed, and R79 is installed.

VSUB/VES Circuit

The quiescent CCD substrate voltage (VSUB) is set by a potentiometer and resistor divider network. The VSUB voltage is buffered by an operational amplifier configured with a gain of 1.40, to allow the voltage to be adjusted to nearly 14.0 V. A blocking diode prevents the VSUB bias circuitry from being damaged by the higher−voltage electronic shutter pulse.

For electronic shutter operation, the VES signal drives a transistor amplifier circuit that AC−couples the voltage difference between the VPLUS and VMINUS supplies onto the Substrate voltage. This creates the necessary potential to clear all charge from the photodiodes, thereby acting as an electronic shutter to control exposure.

VDD Bias Voltage

The VDDL and VDDR video output amplifier supplies in the CCD are coupled directly to the +15 V regulated supply on the Imager Board. The Imager Board contains optional circuitry that allows this voltage to be adjusted through the Alternate VDD bias circuit.

The Imager Board contains optional Amplifier Enable circuitry to control a switch that switches the VDD voltage from +15 V to ALT_VDD.

CCD Image Sensor

This evaluation board supports the KAI−2001, KAI−2020, and KAI−2093 Image Sensors.

Emitter−Follower

The VOUT_LEFT_CCD and VOUT_RIGHT_CCD video output signals are buffered using bipolar junction transistors in the emitter−follower configuration. These circuits also provide the necessary 5 mA current sink for the CCD output circuits. The voltage gain of this stage is approximately 0.96.

Line Drivers

The buffered VOUT_LEFT_CCD and VOUT_RIGHT_CCD signals are AC−coupled and driven from the Imager Board by operational amplifiers in a non−inverting configuration. The operational amplifiers are configured to have a gain of 1.25, which yields an overall gain of 0.6 when driving the properly terminated 75 Ω video coaxial cabling from the SMB connector. This is done to prevent overloading the AFE on the Timing Board.

The video output of either channel may be multiplexed to the VOUT_MUX output. The multiplexer is controlled by the VIDEO_MUX signal. This circuitry is for ON Semiconductor use only, and is not enabled.

ESD Bias Voltage

The RESET and HCLK gates on the KAI−2001, KAI−2020, and KAI−2093 CCDs are protected from ESD damage by internal circuitry. The ESD bias voltage is set by a potentiometer, buffered by an operational amplifier configured as a voltage follower. The ESD bias voltage must be more negative than any of the protected gates during operation and powerup. In order to ensure these conditions are met, diodes are connected external to the CCD between the protected gates and VESD, and between VSUB and VESD.

It is also recommended that during powerup of the Timing Board and Imager Board, the VMINUS supply is applied before, or simultaneously with, the other power supplies. For more information, refer to the appropriate CCD Image Sensor Device Performance Specifications.

OPERATIONAL SETTINGS

The Imager board is configured to operate the KAI−2001/KAI−2020/KAI−2093 Image Sensor under the following operating conditions:

DC Bias Voltages

The following voltages are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 3 correspond to the device specification nominal settings at the time of this document's publication, and are subject to change. The Min and Max voltages in the table indicate the approximate adjustable voltage range on the imager board. These values may exceed the specified CCD operating conditions. See the appropriate device specifications for details.

Table 3. DC BIAS VOLTAGES

Description	Symbol	Min	KAI−2001 / KAI−2020 Nominal	KAI−2093 Nominal	Max	Units	Potentiometer	Notes
Output Gate	OG	−5.0	−2.0	−2.5	−0.5	V	R26	
Reset Drain	RD	7.0	12.0	10.5	14.0	V	R25	
Output Amplifier Supply	VDD		15.0	15.0		V	Fixed	
Alternate Amplifier Supply	ALT_VDD	6.0			11.0	V	R28	
Ground	GND		0.0	0.0		V	Fixed	
Substrate	SUB	7.0	Vab	Vab	13.0	V	R17	1
ESD Protection	ESD	−6.0	−7.0	−7.0	−11.0	V	R27	

1. The recommended VSUB voltage is specified for each CCD image sensor, and is labeled on the device container as VAB.

Clock Voltages

The following clock voltage levels are fixed, or adjusted with a potentiometer as noted. The nominal values listed in Table 4 correspond to the device specification nominal settings at the time of this document¿s publication, and are subject to change. The Min and Max voltages in the table indicate the approximate adjustable voltage range on the imager board. These values may exceed the specified CCD operating conditions. See the appropriate device specification for details.

Table 4. CLOCK VOLTAGES

Description	Symbol	Level	Min	KAI−2001 / KAI−2020 Nom	KAI−2093 Nom	Max	Unit	Potentiometer	Notes
Horizontal CCD Clock	Hxx_CCD	Low	−7.5	−4	−4	−1	V	R146	2
		High	−5	1	1	5	V	R129	3
Vertical CCD Clock	Vx_CCD	Low	−12	−9	−9	−6.5	V	R66	4
	Vx_CCD	Mid	−3	0	−1.5	3	V	R107	5
	V2_CCD	High	6.5	8	8	12	V	R83	
Reset Clock	RESET_CCD	Low	−7.5	−3.5	−3.5	−1	V	R166	
		High	0.5	1.5	1.5	5	V	R158	
Fast Dump Clock	FDG_CCD	Low	−11	−9	0	−4	V	R108	6
		High	2.5	5	0	5	V	R93	6
VDD	+15 V	High		15	15		V	Fixed	

2. The H1A_CCD, H1B_CCD, H2A_CCD, and H2B_CCD low levels are controlled by the same potentiometer (R146).
3. The H1A_CCD, H1B_CCD, H2A_CCD, and H2B_CCD high levels are controlled by the same potentiometer (R129).
4. V1_CCD and V2_CCD low levels are controlled by the same potentiometer (R66).
5. V1_CCD and V2_CCD mid levels are controlled by the same potentiometer (R107).
6. The KAI−2093 has no Fast Dump Gate; CCD pin 11 is 0.0 V. To accomplish this, R91 is removed, and R79 is installed.

Reset Clock Pulse Width

The pulse width of RESET_CCD may be set by configuring P[2..0], the inputs to the programmable one−shot U13. P[2..0] can be tied high or low to achieve the desired pulse width by populating the resistors R156, R157, R160, and R161 accordingly. This feature is optional, as the RESET pulsewidth may also be controlled from the Timing Board. In that case, U13 is removed, and R147 is installed to bypass this circuitry.

Table 5. RESET CLOCK PULSE WIDTH

Pulse Width	P0	P1	P2	R156	R157	R160	R161	Notes
15 ns	0	0	0	IN	OUT	IN	OUT	
5 ns	1	0	0	OUT	IN	IN	OUT	Default Setting
7.5 ns	0	1	0	IN	OUT	OUT	IN	
10 ns	1	1	0	OUT	IN	OUT	IN	

BLOCK DIAGRAM AND PERFORMANCE DATA

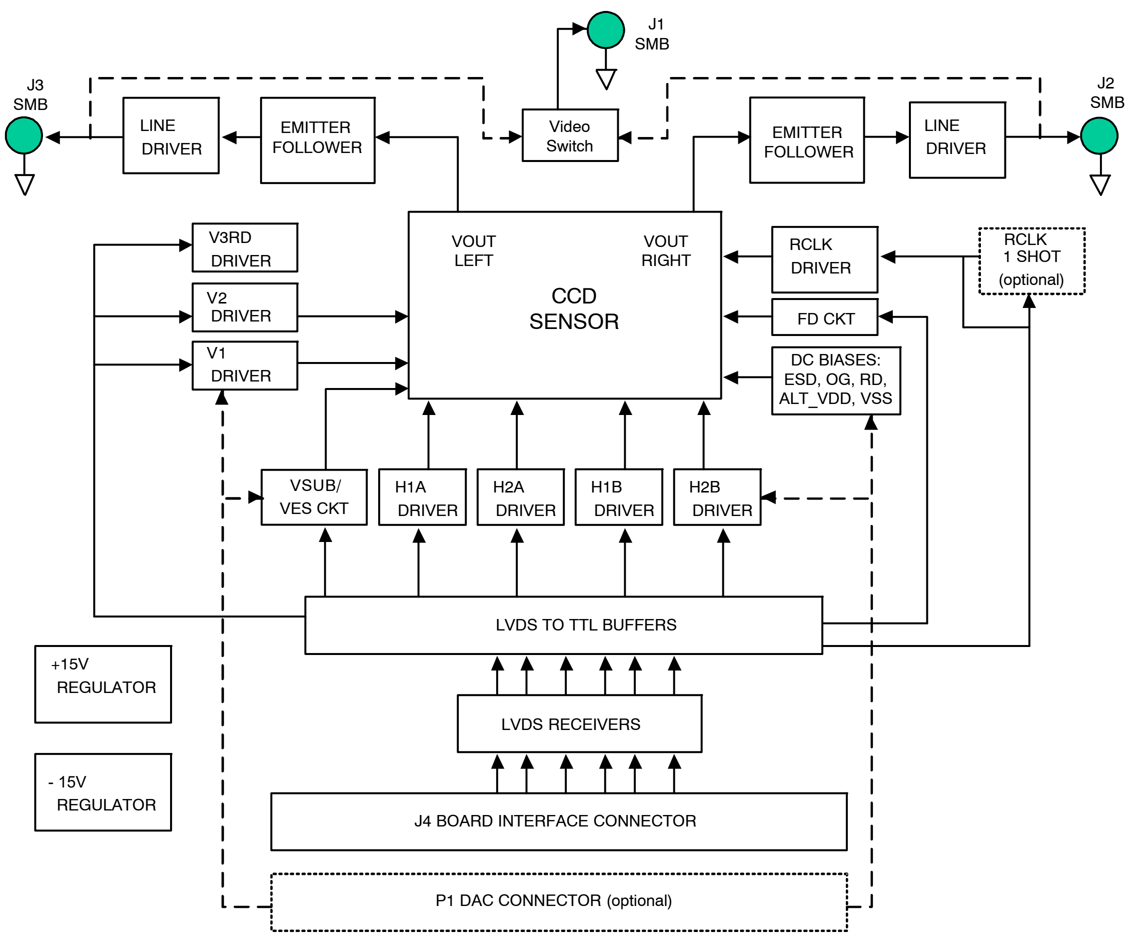

Figure 1. KAI−2001/KAI−2020/KAI−2093 Imager Board Block Diagram

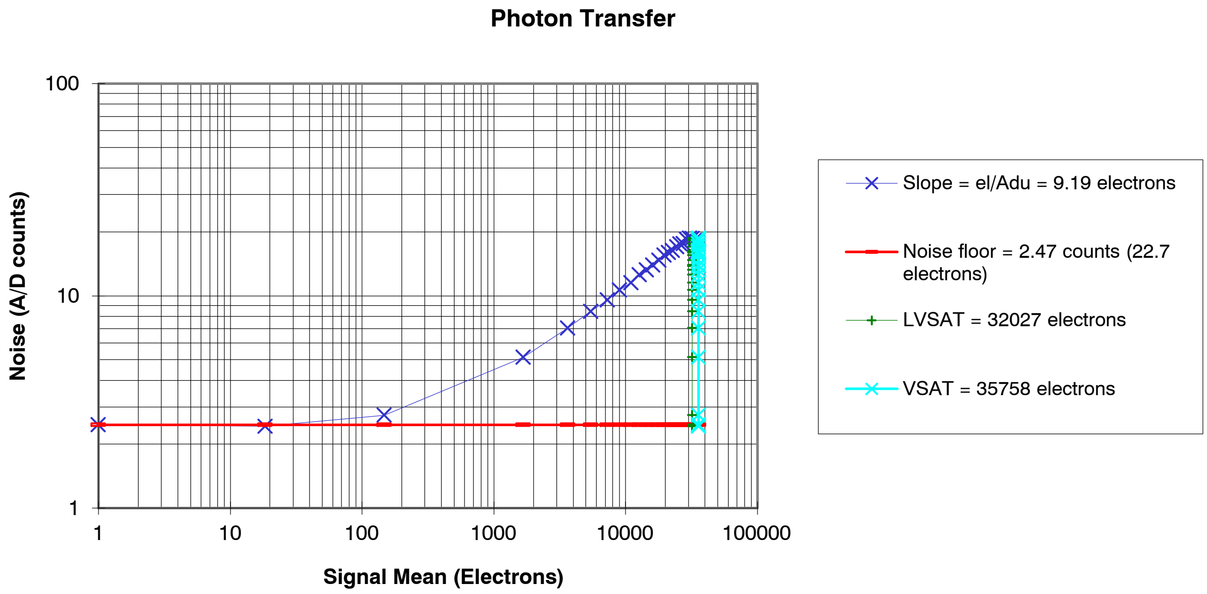

Figure 2. KAI−2020 Measured Performance − Dynamic Range and Noise Floor

CONNECTOR ASSIGNMENTS AND PINOUTS

SMB Connectors J1, J2 and J3

The emitter−follower buffered VOUT_LEFT and VOUT_RIGHT signals are driven from the Imager Board via the SMB connectors J3 and J2, respectively. VOUT_LEFT is the primary output from the CCD; VOUT_RIGHT is only used when the CCD is clocked in dual−channel mode. Coaxial cable with a characteristic impedance of 75 Ω should be used to connect the imager board to the Timing Generator Board to match the series and terminating resistors used on these boards. J1 is an auxiliary SMB connector driven from a relay. The relay switches between the VOUT_LEFT and VOUT_RIGHT signals, allowing one video connection to transmit either output.

Table 6. J4 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	AGND	4	AGND
5	IMAGER_IN11+	6	IMAGER_IN11−
7	AGND	8	AGND
9	IMAGER_IN10+	10	IMAGER_IN10−
11	AGND	12	AGND
13	IMAGER_IN9+	14	IMAGER_IN9−
15	AGND	16	AGND
17	IMAGER_IN8+	18	IMAGER_IN8−
19	AGND	20	AGND
21	IMAGER_IN7+	22	IMAGER_IN7−
23	AGND	24	AGND
25	IMAGER_IN6+	26	IMAGER_IN6−
27	AGND	28	AGND
29	IMAGER_IN5+	30	IMAGER_IN5−
31	AGND	32	AGND
33	IMAGER_IN4+	34	IMAGER_IN4−
35	AGND	36	AGND
37	IMAGER_IN3+	38	IMAGER_IN3−

Table 6. J4 INTERFACE CONNECTOR PIN ASSIGNMENTS

Pin	Signal	Pin	Signal
39	AGND	40	AGND
41	IMAGER_IN2+	42	IMAGER_IN2−
43	AGND	44	AGND
45	IMAGER_IN1+	46	IMAGER_IN1−
47	N.C.	48	N.C.
49	AGND	50	AGND
51	N.C.	52	N.C.
53	VMINUS_MTR	54	VMINUS_MTR
55	N.C.	56	N.C.
57	AGND	58	AGND
59	IMAGER_IN0+	60	IMAGER_IN0−
61	−5 V_MTR	62	−5 V_MTR
63	IMAGER_IN15+	64	IMAGER_IN15−
65	AGND	66	AGND
67	IMAGER_IN14+	68	IMAGER_IN14−
69	+5 V_MTR	70	+5 V_MTR
71	IMAGER_IN13+	72	IMAGER_IN13−
73	AGND	74	AGND
75	IMAGER_IN12+	76	IMAGER_IN12−
77	VPLUS_MTR	78	VPLUS_MTR
79	N.C.	80	N.C.

Warnings and Advisories

ON Semiconductor is not responsible for customer damage to the Imager Board or Imager Board electronics. The customer assumes responsibility and care must be taken when probing, modifying, or integrating the ON Semiconductor Evaluation Board Kits.

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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