

SNx4AC244 Octal Buffers/Drivers with 3-State Outputs

1 Features

- Operation of 2-V to 6-V V_{CC}
- Inputs accept voltages to 6 V
- Max t_{pd} of 7.5 ns at 5 V

2 Description

These octal buffers and line drivers are designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Package Information

PART NUMBER	PACKAGE ¹	BODY SIZE (NOM)
SN74AC244	DB (SSOP, 20)	7.2 mm × 5.3 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
	N (PDIP, 20)	24.33 mm × 6.35 mm
	NS (SOP, 20)	12.60 mm × 5.30 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm

1. For all available packages, see the orderable addendum at the end of the data sheet.

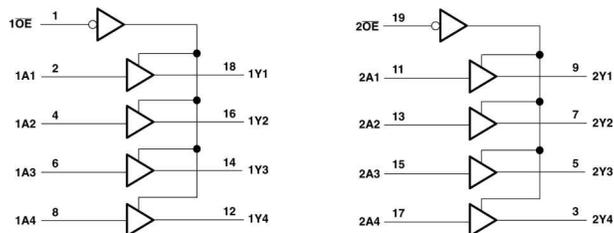


Figure 2-1. Logic Diagram (Positive Logic)



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3 Revision History

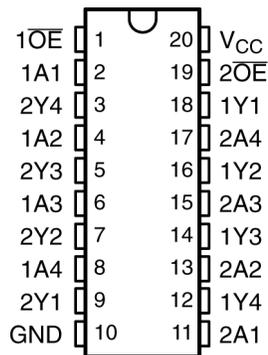
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (October 2003) to Revision F (May 2023)

Page

- Added *Package Information* table, *Pin Functions* table, and *Thermal Information* table..... 1

4 Pin Configuration and Functions



**Figure 4-1. SN54AC244 J or W Package
SN74AC244 DB, DW, N, NS, or PW Package (Top
View)**

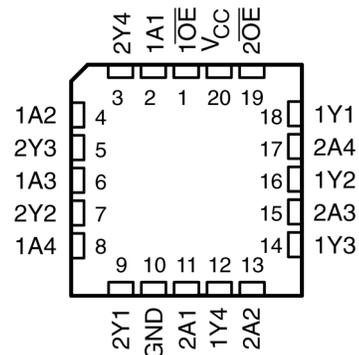


Figure 4-2. SN54AC244 FK Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE ¹	DESCRIPTION
NAME	NO.		
1A1	2	I	Input
1A2	4	I	Input
1A3	6	I	Input
1A4	8	I	Input
1 OE	1	I	Output enable
1Y1	18	O	Output
1Y2	16	O	Output
1Y3	14	O	Output
1Y4	12	O	Output
2A1	11	I	Input
2A2	13	I	Input
2A3	15	I	Input
2A4	17	I	Input
2 OE	19	I	Output enable
2Y1	9	O	Output
2Y2	7	O	Output
2Y3	5	O	Output
2Y4	3	O	Output
GND	10	—	Ground
V _{CC}	20	—	Power pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I ¹	Input voltage range	-0.5	$V_{CC}+0.5$	V
V_O ¹	Output voltage range	-0.5	$V_{CC}+0.5$	V
I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	Input clamp current		± 20	mA
I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	Output clamp current,		± 20	mA
I_O ($V_O = 0$ or V_{CC})	Continuous output current		± 50	mA
	Continuous current through V_{CC} or GND		± 200	mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions

(see [Note 1](#))

		SN54AC244		SN74AC244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	6	2	6	V
V_{IH}	High-level input voltage	$V_{CC} = 3\text{ V}$	2.1	2.1		V
		$V_{CC} = 4.5\text{ V}$	1.15	1.15		
		$V_{CC} = 5.5\text{ V}$	1.85	1.85		
V_{IL}	Low-level input voltage	$V_{CC} = 3\text{ V}$		0.9	0.9	V
		$V_{CC} = 4.5\text{ V}$		1.35	1.35	
		$V_{CC} = 5.5\text{ V}$		1.65	1.65	
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3\text{ V}$		-12	-12	mA
		$V_{CC} = 4.5\text{ V}$		-24	-24	
		$V_{CC} = 5.5\text{ V}$		-24	-24	
I_{OL}	Low-level output current	$V_{CC} = 3\text{ V}$		12	12	mA
		$V_{CC} = 4.5\text{ V}$		24	24	
		$V_{CC} = 5.5\text{ V}$		24	24	
$\Delta t/\Delta v$	Input transition rise or fall rate		8		8	ns/V
T_a	Operating free-air temperature	-55	125	-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		SNx4AC244					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 PINS					
R _{θJA}	Junction-to-ambient thermal resistance	70	58	69	60	83	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AC244		SN74AC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	3 V	2.9			2.9		2.9	V	
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	I _{OH} = -12 mA	3 V	2.56			2.4		2.46		
		4.5 V	3.86			3.7		3.76		
	I _{OH} = -24 mA	5.5 V	4.86			4.7		4.76		
		I _{OH} = -50 mA ⁽¹⁾	5.5 V				3.85			
I _{OH} = -75 mA ⁽¹⁾	5.5 V						3.85			
V _{OL}	I _{OL} = 50 μA	3 V			0.1		0.1	0.1	V	
		4.5 V			0.1		0.1	0.1		
		5.5 V			0.1		0.1	0.1		
	I _{OL} = 12 mA	3 V			0.36		0.5	0.44		
		4.5 V			0.36		0.5	0.44		
	I _{OL} = 24 mA	5.5 V			0.36		0.5	0.44		
		I _{OL} = 50 mA ⁽¹⁾	5.5 V				1.65			
I _{OL} = 75 mA ⁽¹⁾	5.5 V						1.65			
I _I	Data inputs	V _I = V _{CC} or GND			±0.1		±1	±1	μA	
	Control inputs	V _I = V _{CC} or GND	5.5 V		±0.1		±1	±1		
I _{OZ}	V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}		5.5 V		±0.25		±5	±2.5	μA	
I _{CC}	V _I = V _{CC} or GND,	I _O = 0	5.5 V		4		80	40	μA	
C _i	V _I = V _{CC} or GND		5 V		2.5				pF	

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

5.5 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC244		SN74AC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	2	6.5	9	1	12.5	1.5	10	ns
t_{PHL}			2	6.5	9	1	12	2	10	
t_{PZH}	\overline{OE}	Y	2	6	10.5	1	11.5	1.5	11	ns
t_{PZL}			2.5	7.5	10	1	13	2	11	
t_{PHZ}	\overline{OE}	Y	3	7	10	1	12.5	1.5	10.5	ns
t_{PLZ}			2.5	7.5	10.5	1	13	2.5	11.5	

5.6 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Figure 6-1](#))

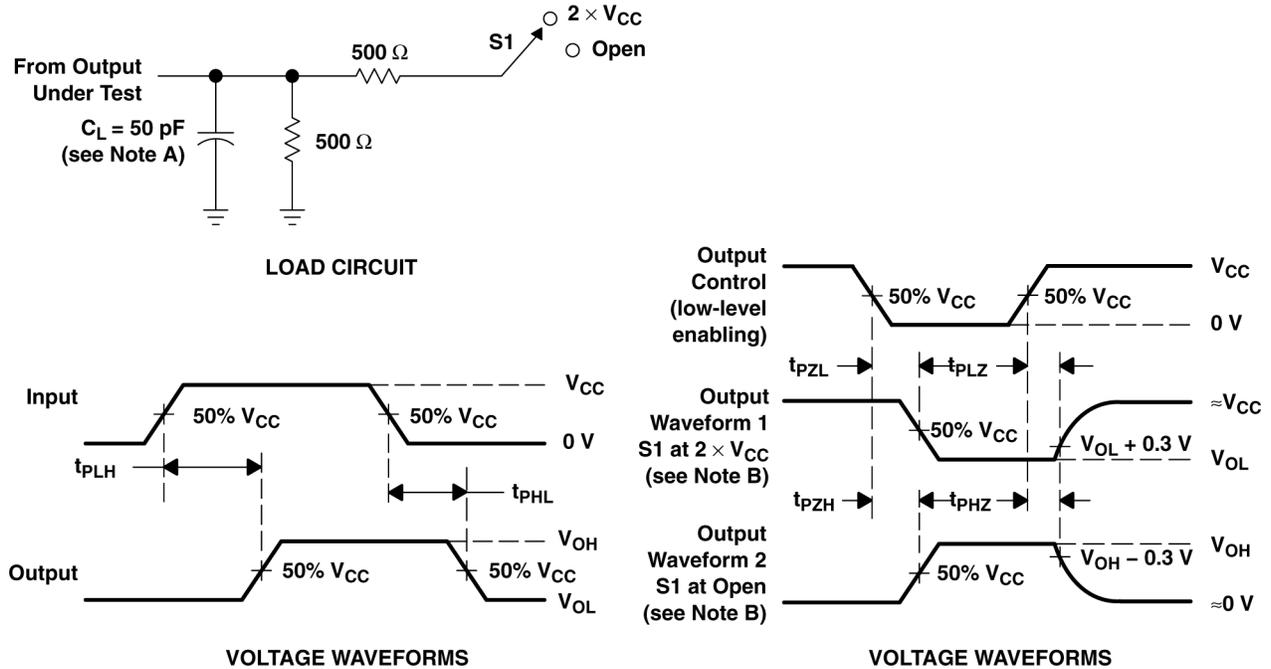
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN54AC244		SN74AC244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	5	7	7	9.5	1	7.5	ns
t_{PHL}			1.5	5	7	7	9	1	7.5	
t_{PZH}	\overline{OE}	Y	1.5	5	7	7	9	1.5	8	ns
t_{PZL}			1.5	5.5	8	8	10.5	1.5	8.5	
t_{PHZ}	\overline{OE}	Y	2.5	6.5	9	9	10.5	1	9.5	ns
t_{PLZ}			2	6.5	9	9	11	2	9.5	

5.7 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per buffer/driver	$C_1 = 50\text{ pF}$, $f = 1\text{ MHz}$	45	pF

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open

7 Detailed Description

7.1 Overview

The 'AC244 devices are organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes noninverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

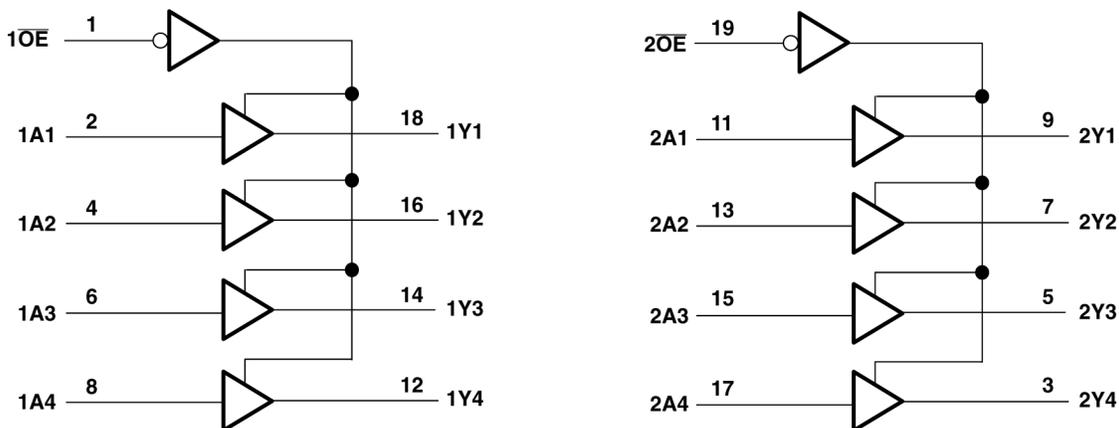


Figure 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

Table 7-1. Function Table (Each Buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-87552012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87552012A SNJ54AC 244FK	Samples
5962-8755201RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201RA SNJ54AC244J	Samples
5962-8755201SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201SA SNJ54AC244W	Samples
5962-8755201VRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201VR A SNV54AC244J	Samples
5962-8755201VSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201VS A SNV54AC244W	Samples
SN74AC244DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC244N	Samples
SN74AC244NE4	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AC244N	Samples
SN74AC244NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SN74AC244PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AC244	Samples
SNJ54AC244FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-87552012A SNJ54AC 244FK	Samples
SNJ54AC244J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201RA SNJ54AC244J	Samples
SNJ54AC244W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8755201SA SNJ54AC244W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AC244, SN54AC244-SP, SN74AC244 :

● Catalog : [SN74AC244](#), [SN54AC244](#)

● Automotive : [SN74AC244-Q1](#), [SN74AC244-Q1](#)

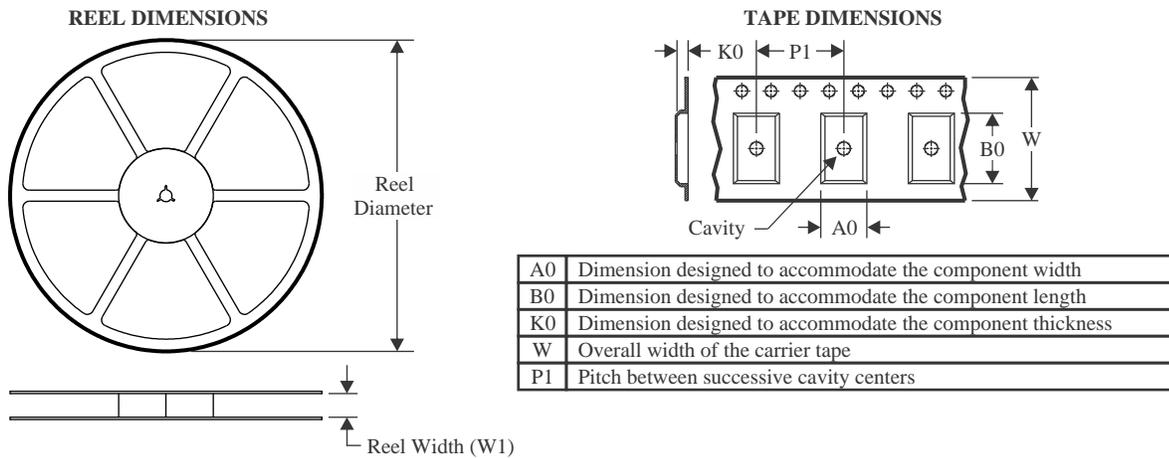
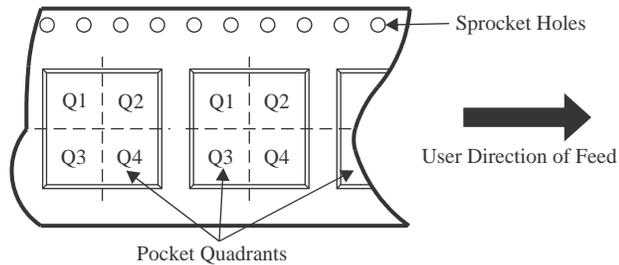
● Enhanced Product : [SN74AC244-EP](#), [SN74AC244-EP](#)

● Military : [SN54AC244](#)

- Space : [SN54AC244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


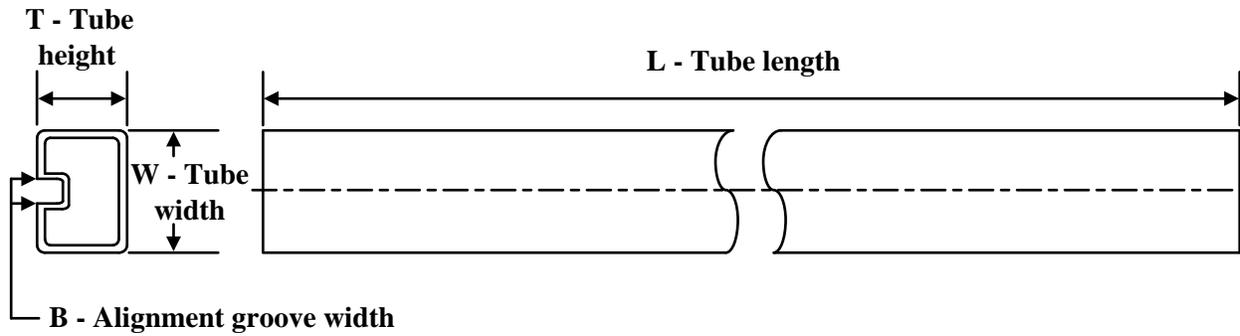
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AC244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AC244NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AC244PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC244DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AC244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AC244NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AC244PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


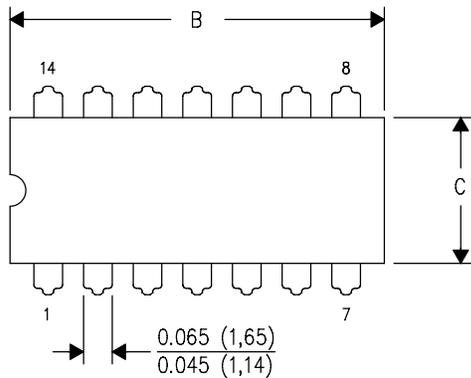
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-87552012A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-8755201SA	W	CFP	20	1	506.98	26.16	6220	NA
5962-8755201VSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74AC244N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AC244NE4	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AC244FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54AC244W	W	CFP	20	1	506.98	26.16	6220	NA

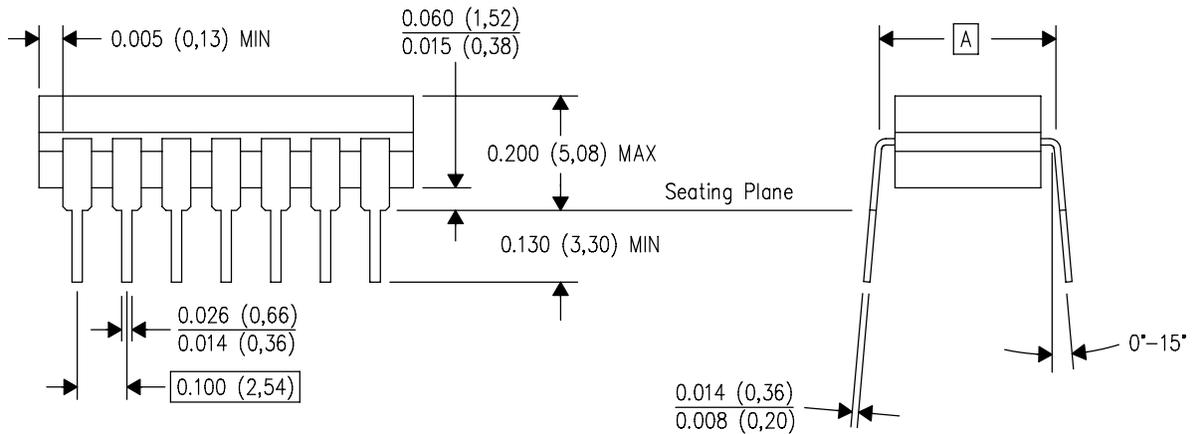
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

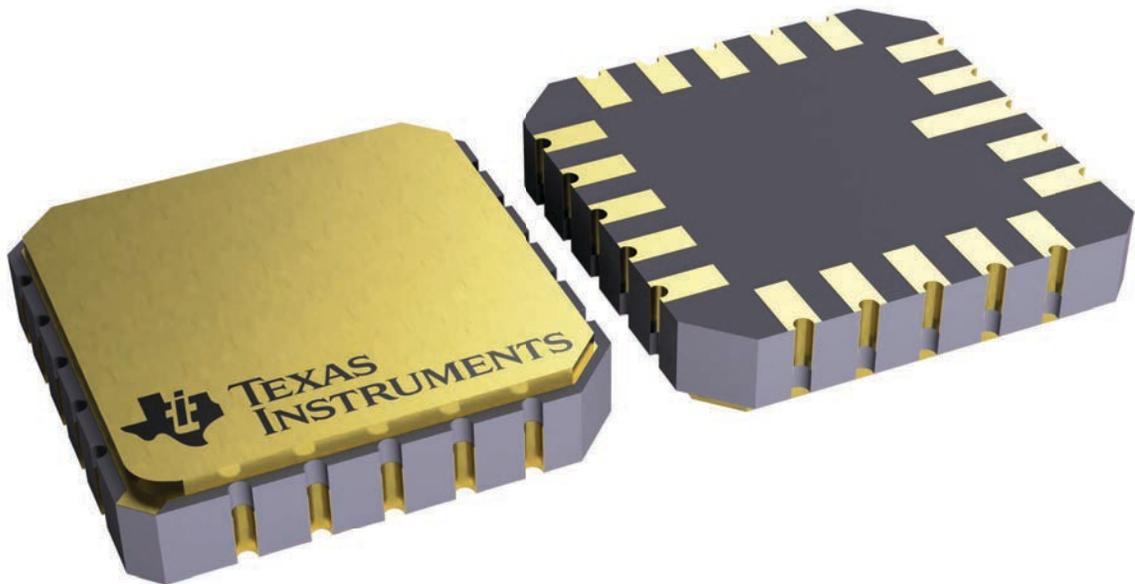
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

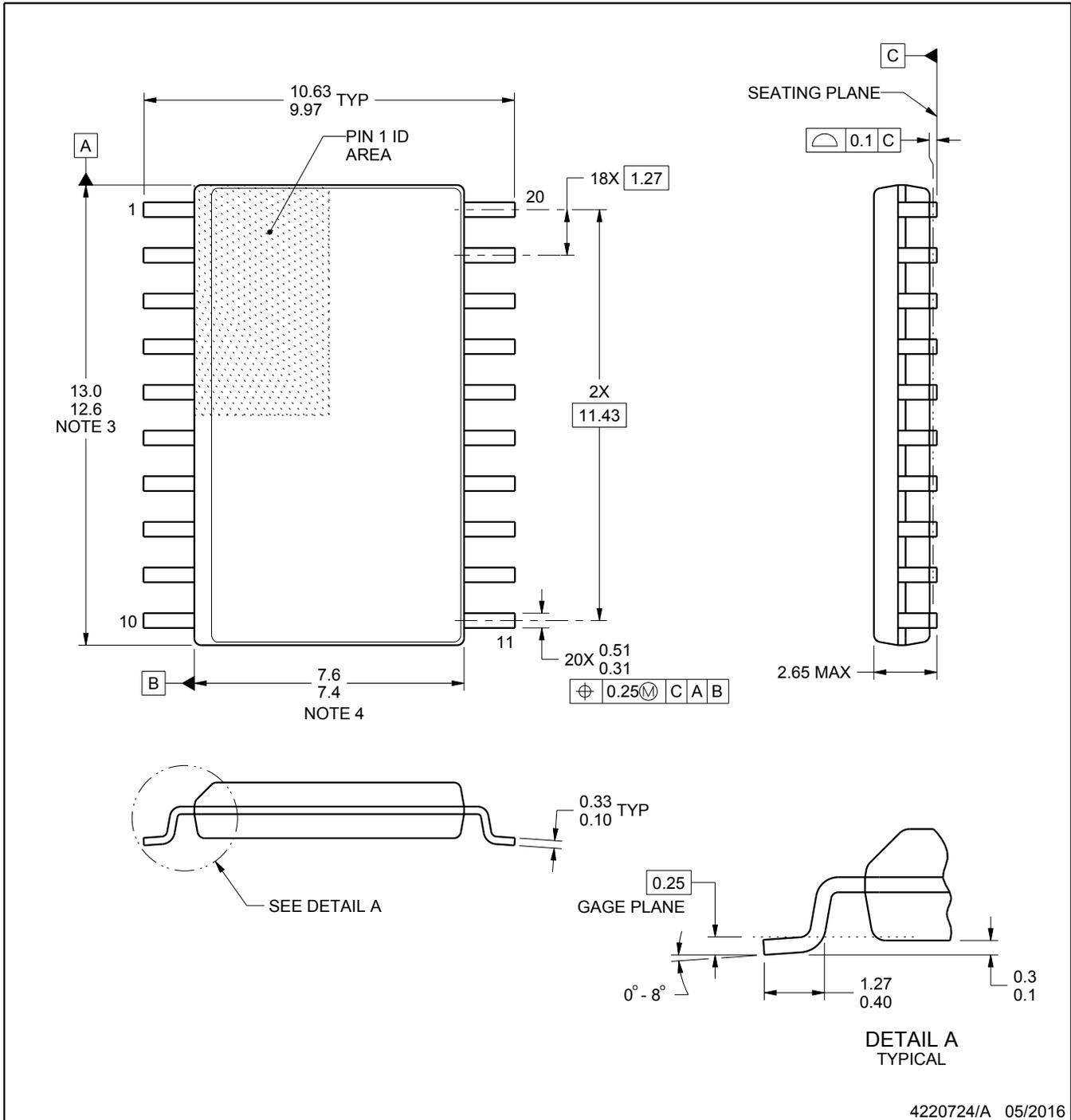
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

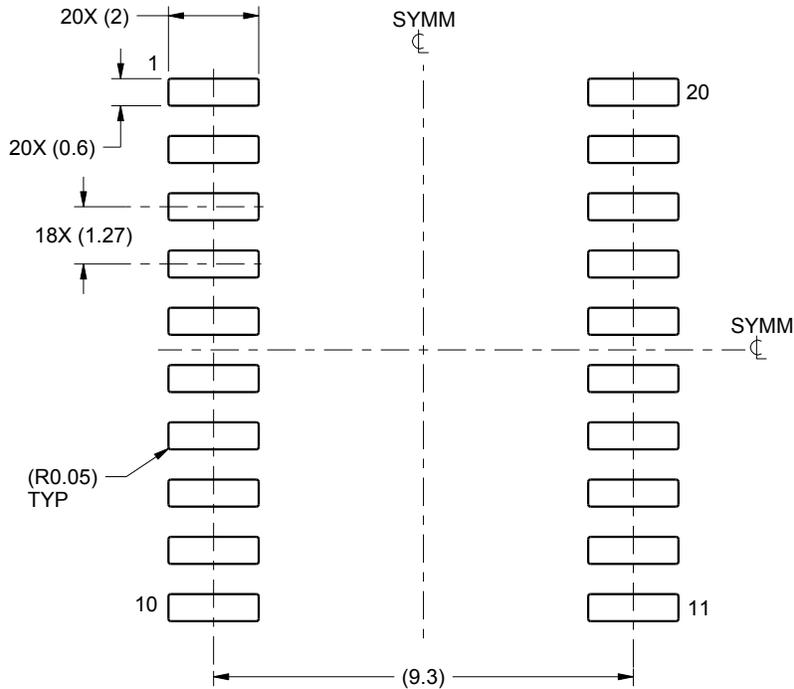
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

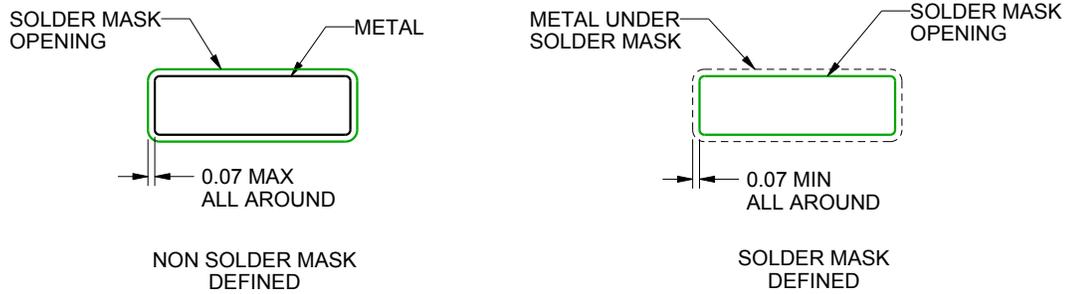
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

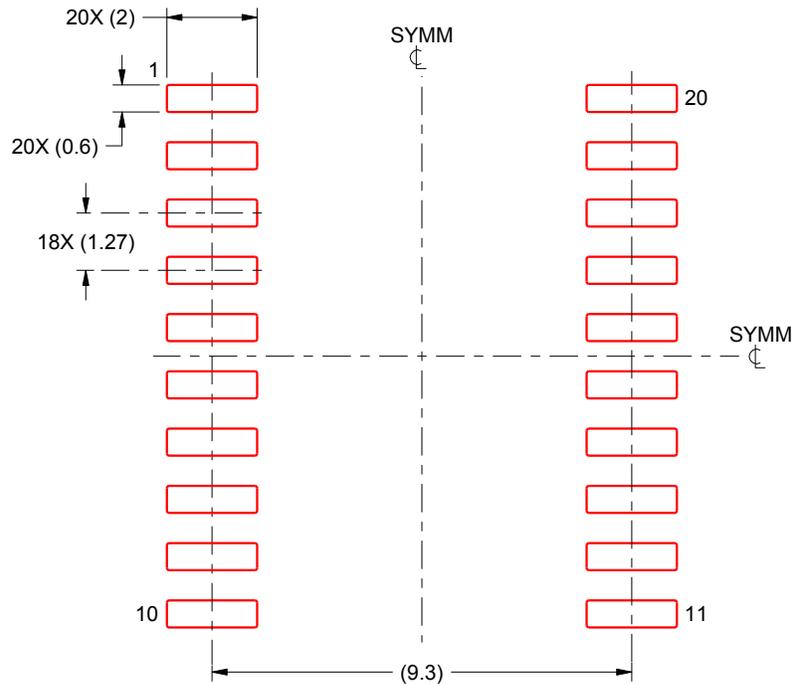
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

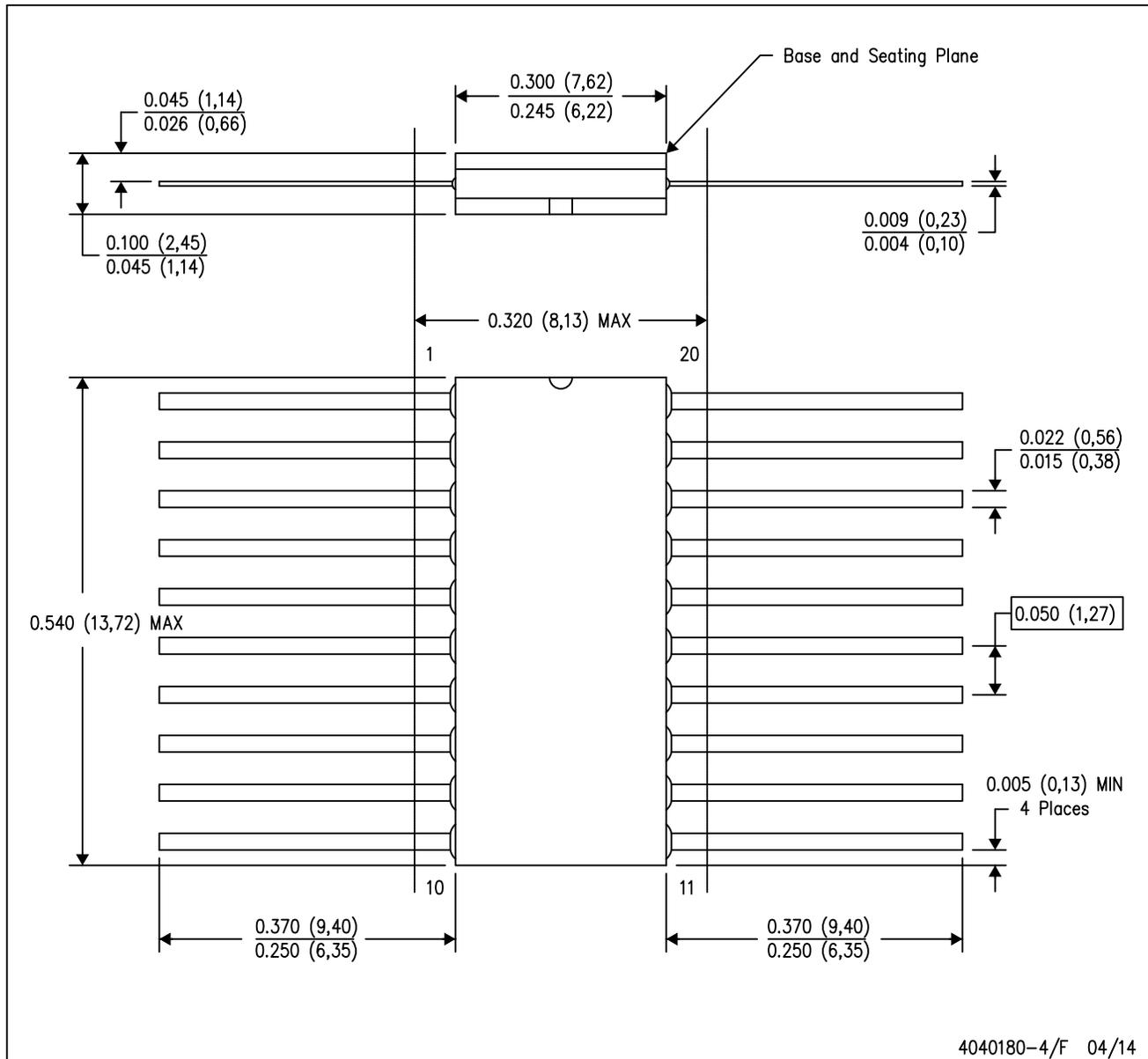
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

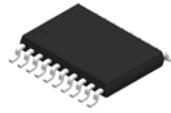
CERAMIC DUAL FLATPACK



4040180-4/F 04/14

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

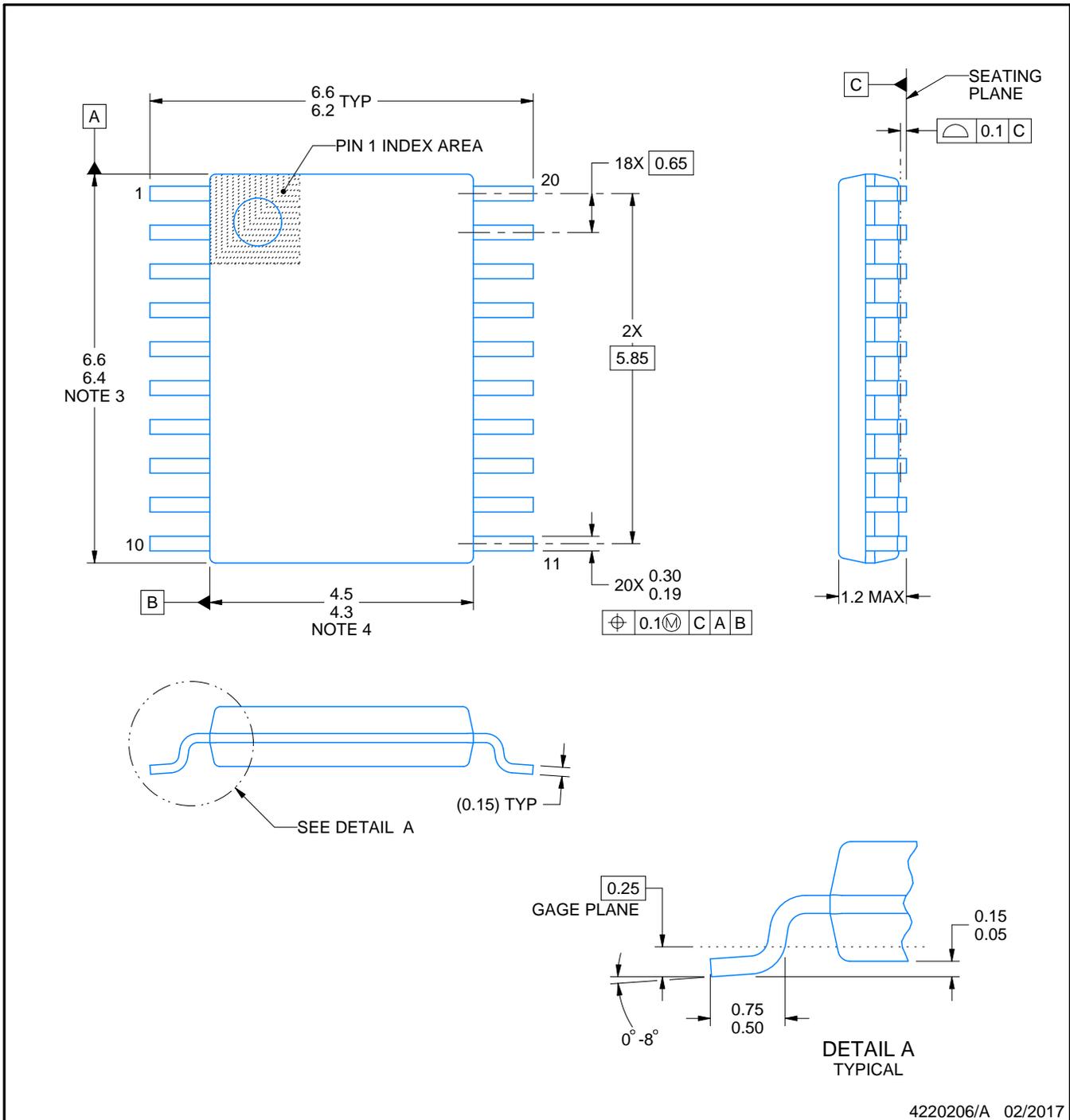
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

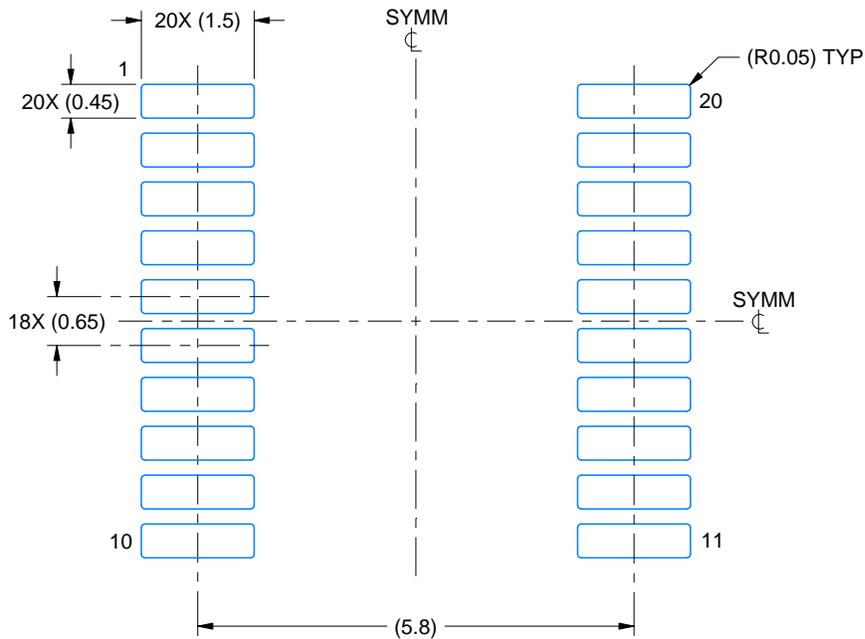
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

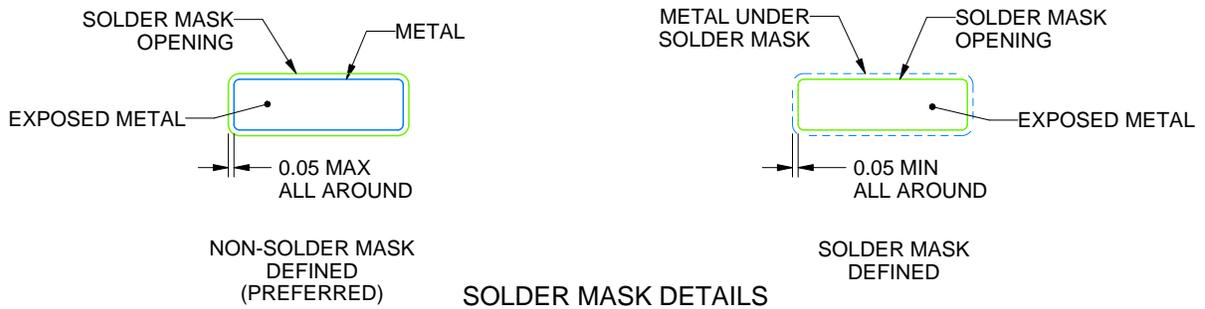
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

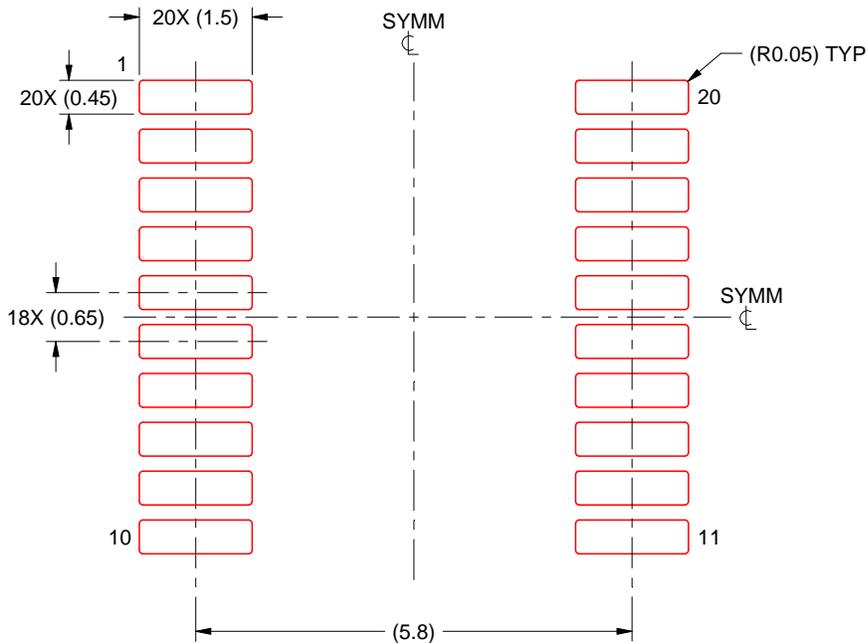
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

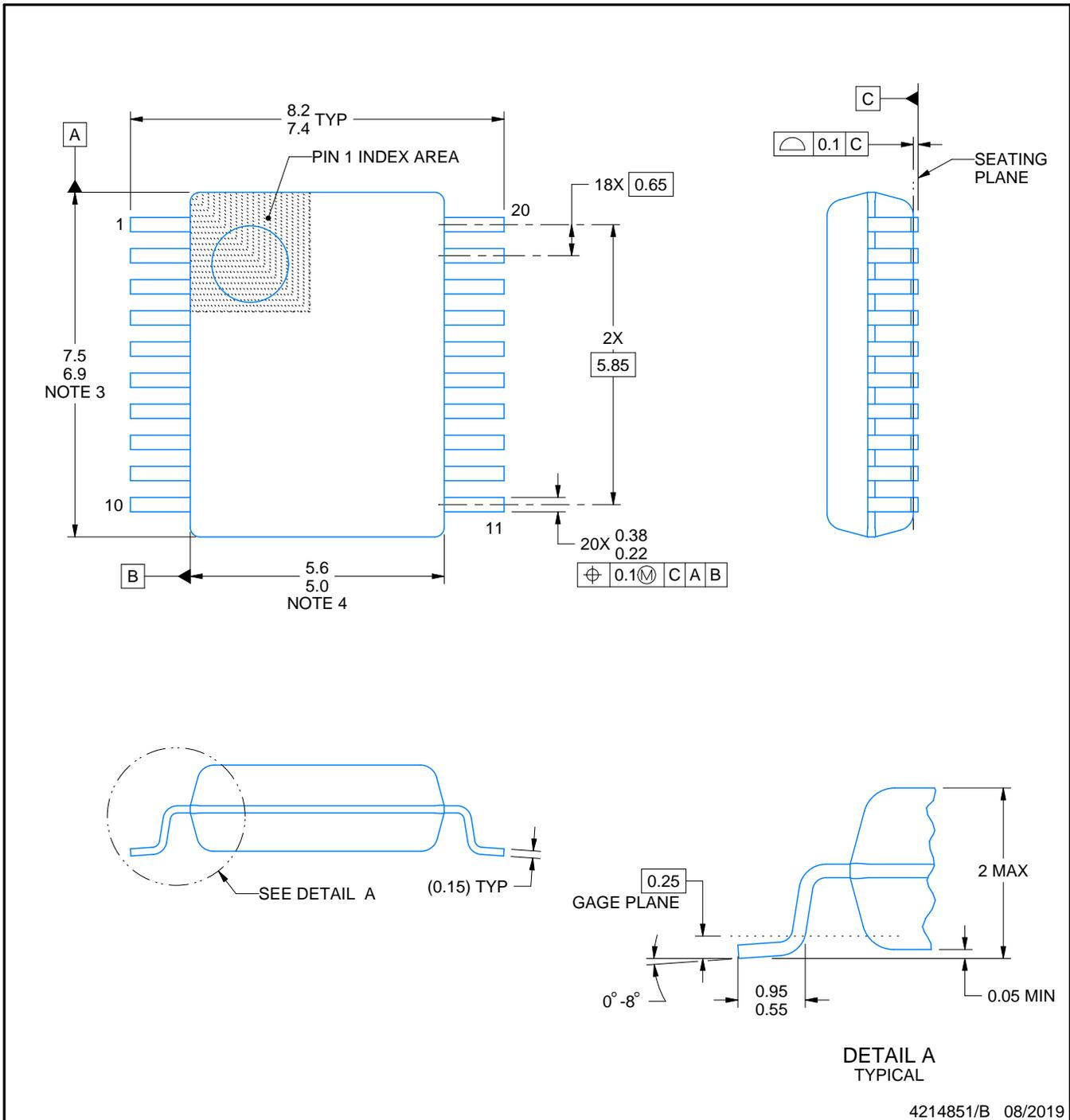
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

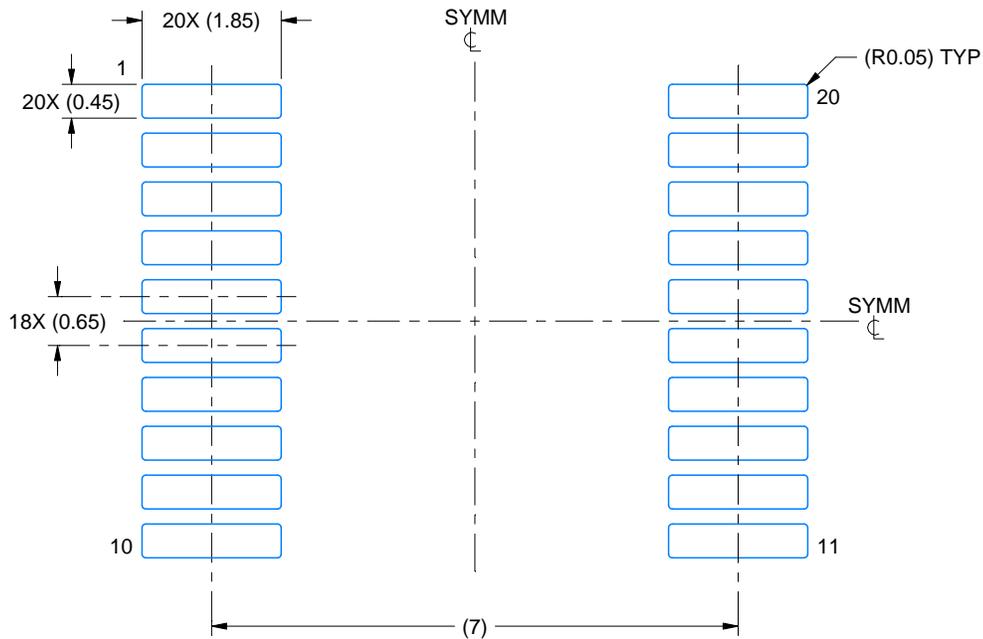
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

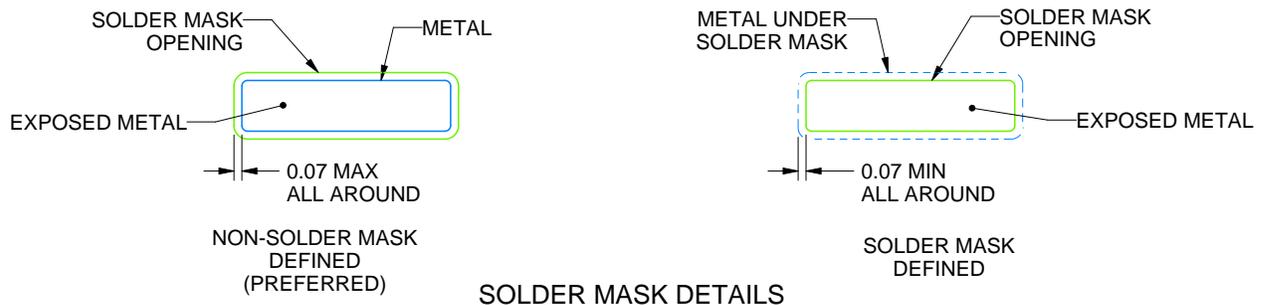
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

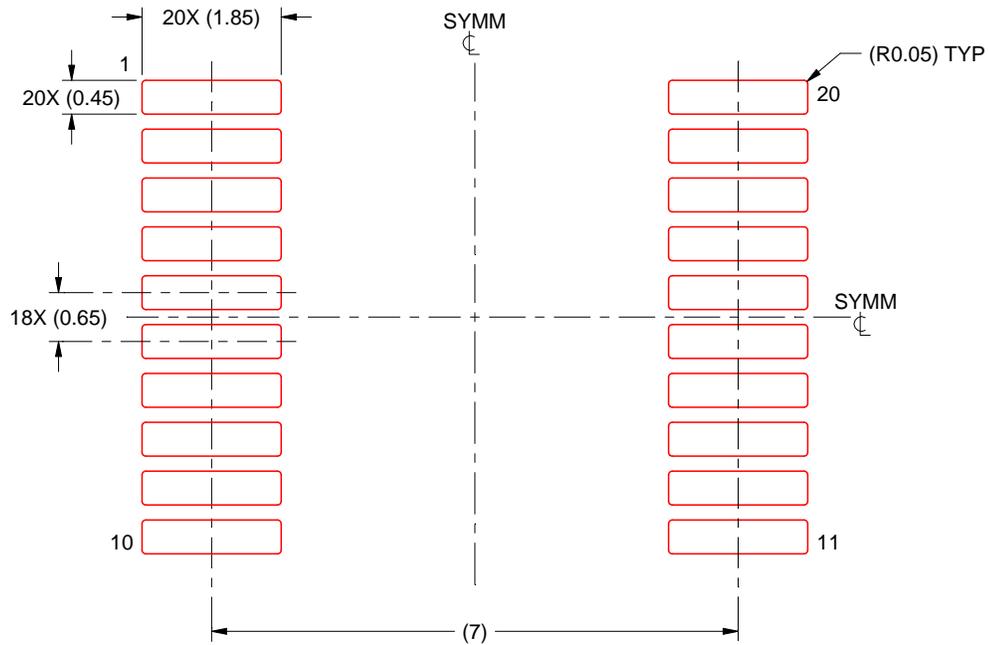
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

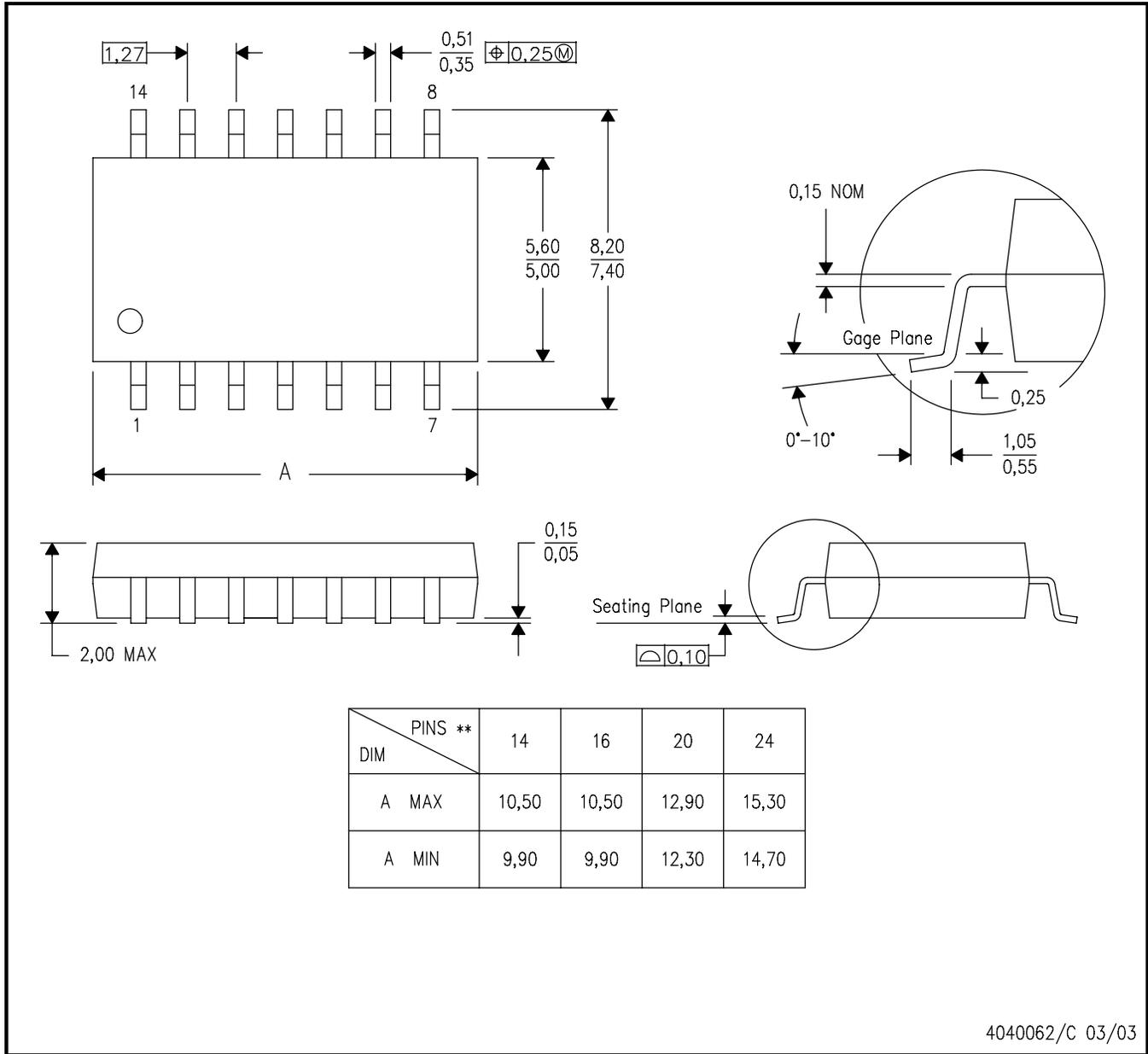
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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