Description

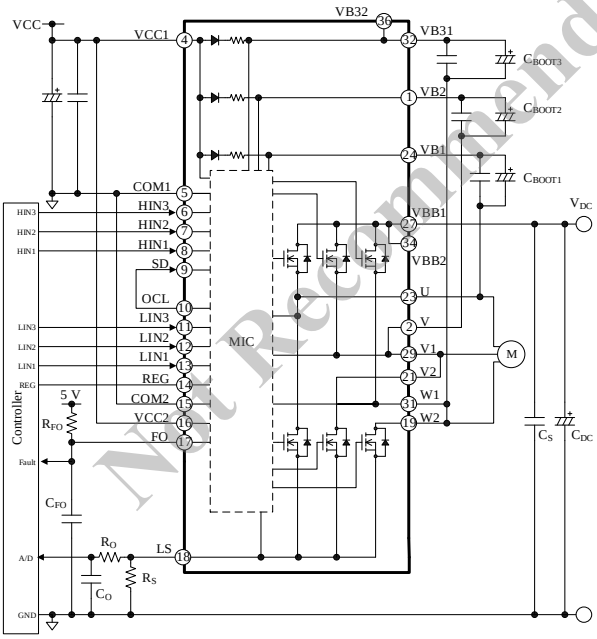
The SX68000MH series are high voltage 3-phase motor drivers in which transistors, a pre-drive circuit, and bootstrap circuits (diodes and resistors) are highly integrated.

These products can optimally control the inverter systems of low- to medium-capacity motors that require universal input standards.

Features

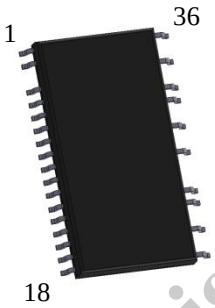
- Built-in Bootstrap Diodes with Current Limiting Resistors (60 Ω)
- CMOS-compatible Input (3.3 V or 5 V)
- Pb-free (RoHS Compliant)
- Fault Signal Output at Protection Activation (FO Pin)
- High-side Shutdown Signal Input (SD Pin)
- Protections Include:
  Overcurrent Limit (OCL): Auto-restart
  Overcurrent Protection (OCP): Auto-restart
  Undervoltage Lockout for Power Supply
  High-side (UVLO_VB): Auto-restart
  Low-side (UVLO_VCC): Auto-restart
  Thermal Shutdown (TSD): Auto-restart

Typical Application



Package

SOP36



Not to scale

Selection Guide

V_{DSS}	I_O	Part Number
250 V	2.0 A	SX68001MH
500 V	2.5 A	SX68003MH

Applications

- Fan Motor for Air Conditioner
- Fan Motor for Air Purifier and Electric Fan

Contents

1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Rating	Unit	Remarks
Power MOSFET Breakdown Voltage	V_{DSS}	V_{CC} = 15 V, I_D = 100 µA, V_{IN} = 0 V	250	V	SX68001MH
			500		SX68003MH
Logic Supply Voltage	V_{CC}	VCC1–COM1, VCC2–COM2	20	V	
	V_{BS}	VB1–U; VB2–V, VB2–V1; VB31–W1, VB32–W1	20		
Output Current (DC) (1)	I_O	T_C = 25 °C, T_J < 150 °C	2	A	SX68001MH
			2.5		SX68003MH
Output Current (Pulse)	I_{OP}	T_C = 25 °C, T_J < 150 °C, P_W ≤ 100 µs	3	A	SX68001MH
			3.75		SX68003MH
Regulator Output Current	I_{REG}		35	mA	
Input Voltage	V_{IN}	HINx, LINx, FO, SD	−0.5 to 7	V	
Allowable Power Dissipation	P_D	T_C = 25 °C	3	W	
Operating Case Temperature(2)	$T_{C(OP)}$		−20 to 100	°C	
Junction Temperature(3)	T_J		150	°C	
Storage Temperature	T_{STG}		−40 to 150	°C	

(1) Should be derated depending on an actual case temperature. See Section 14.4.
(2) Refers to a case temperature measured during IC operation.
(3) Refers to the junction temperature of each chip built in the IC, including the control IC, transistors, and fast recovery diodes.

2. Recommended Operating Conditions

Unless specifically noted, COM1 = COM2 = COM.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Main Supply Voltage	V_{DC}	VBBx–LS	—	150	200	V	SX68001MH
		VBBx–LS	—	300	400		SX68003MH
Logic Supply Voltage	V_{CC}	VCC1–COM1, VCC2–COM2	13.5	—	16.5	V	
	V_{BS}	VB1–U; VB2–V, VB2–V1; VB31–W1, VB32–W1	13.5	—	16.5	V	
Input Voltage (HINx, LINx, SD, FO)	V_{IN}		0	—	5.5	V	
Minimum Input Pulse Width	$t_{IN(MIN)ON}$		0.5	—	—	µs	
	$t_{IN(MIN)OFF}$		0.5	—	—	µs	
Dead Time of Input Signal	t_{DEAD}		1.5	—	—	µs	
FO Pin Pull-up Resistor	R_{FO}		3.3	—	10	kΩ	
FO Pin Pull-up Voltage	V_{FO}		3.0	—	5.5	V	
FO Pin Noise Filter Capacitor	C_{FO}		0.001	—	0.01	µF	
Bootstrap Capacitor	C_{BOOT}		1	—	—	µF	
Shunt Resistor	R_S	$I_P \leq 3$ A	0.37	—	—	Ω	SX68001MH
		$I_P \leq 3.75$ A	0.3	—	—		SX68003MH
RC Filter Resistor	R_O		—	—	100	Ω	
RC Filter Capacitor	C_O		1000	—	10000	pF	
PWM Carrier Frequency	f_C		—	—	20	kHz	
Operating Case Temperature	$T_{C(OP)}$		—	—	100	°C	

3. Electrical Characteristics

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless specifically noted, T_A = 25 °C, V_{CC} = 15 V, COM1 = COM2 = COM.

3.1 Characteristics of Control Parts

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Power Supply Operation							
Logic Operation Start Voltage	$V_{CC(ON)}$	VCC1–COM1, VCC2–COM2	10.5	11.5	12.5	V	
	$V_{BS(ON)}$	VB1–U; VB2–V, VB2–V1; VB31–W1, VB32–W1	9.5	10.5	11.5	V	
Logic Operation Stop Voltage	$V_{CC(OFF)}$	VCC1–COM1, VCC2–COM2	10.0	11.0	12.0	V	
	$V_{BS(OFF)}$	VB1–U; VB2–V, VB2–V1; VB31–W1, VB32–W1	9.0	10.0	11.0	V	
Logic Supply Current	I_{CC}	I_{REG} = 0 A	—	4.6	8.5	mA	
	I_{BS}	HINx = 5 V; VBx pin current in 1-phase operation	—	140	400	µA	
Input Signal							
High Level Input Threshold Voltage (HINx, LINx, SD)	V_{IH}	Output ON	—	2.0	2.5	V	
Low Level Input Threshold Voltage (HINx, LINx, SD)	V_{IL}	Output OFF	1.0	1.5	—	V	
FO Pin High Level Input Threshold Voltage	$V_{IH(FO)}$	Output ON	—	2.0	2.5	V	
FO Pin Low Level Input Threshold Voltage	$V_{IL(FO)}$	Output OFF	1.0	1.5	—	V	
High Level Input Current (HINx, LINx)	I_{IH}	V_{IN} = 5 V	—	230	500	µA	
Low Level Input Current (HINx, LINx)	I_{IL}	V_{IN} = 0 V	—	—	2	µA	
Fault Signal Output							
FO Pin Voltage at Fault Signal Output	V_{FOL}	V_{FO} = 5 V, R_{FO} = 10 kΩ	0	—	0.5	V	
FO Pin Voltage in Normal Operation	V_{FOH}	V_{FO} = 5 V, R_{FO} = 10 kΩ	4.8	—	—	V	
Protection							
OCL Pin Output Voltage (L)	$V_{OCL(L)}$		0	—	0.5	V	
OCL Pin Output Voltage (H)	$V_{OCL(H)}$		4.5	—	5.5	V	
Current Limit Reference Voltage	V_{LIM}		0.6175	0.6500	0.6825	V	
OCP Threshold Voltage	V_{TRIP}		0.9	1.0	1.1	V	
OCP Hold Time	t_P		20	25	—	µs	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
OCP Blanking Time	$t_{BK(OCP)}$		—	2	3.5	µs	
Current Limit Blanking Time	$t_{BK(OCL)}$		—	2	3.5	µs	
TSD Operating Temperature	T_{DH}	I_{REG} = 0 mA; without heatsink	135	150	165	°C	
TSD Releasing Temperature	T_{DL}	I_{REG} = 0 mA; without heatsink	105	120	135	°C	
Regulator Output Voltage	V_{REG}	I_{REG} = 0 mA to 35 mA	6.75	7.5	8.25	V	

3.2 Bootstrap Diode Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Bootstrap Diode Leakage Current	I_{LBD}	V_R = 250 V	—	—	10	µA	SX68001MH
		V_R = 500 V	—	—	10		SX68003MH
Bootstrap Diode Forward Voltage	V_{FB}	I_{FB} = 0.15 A	—	1.0	1.3	V	
Bootstrap Diode Series Resistor	R_{BOOT}		48	60	72	Ω	

3.3 Thermal Resistance Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remarks
Junction-to-Case Thermal Resistance(1)	R_{J-C}	All power MOSFETs operating(2)	—	—	10	°C/W	
Junction-to-Ambient Thermal Resistance	R_{J-A}	All power MOSFETs operating(2)	—	—	35	°C/W	

(1) Refers to a case temperature at the measurement point described in Figure 3-1.
(2) Mounted on a CEM-3 glass (1.6 mm in thickness, 35 µm in copper foil thickness), and measured under natural air cooling without silicone potting.

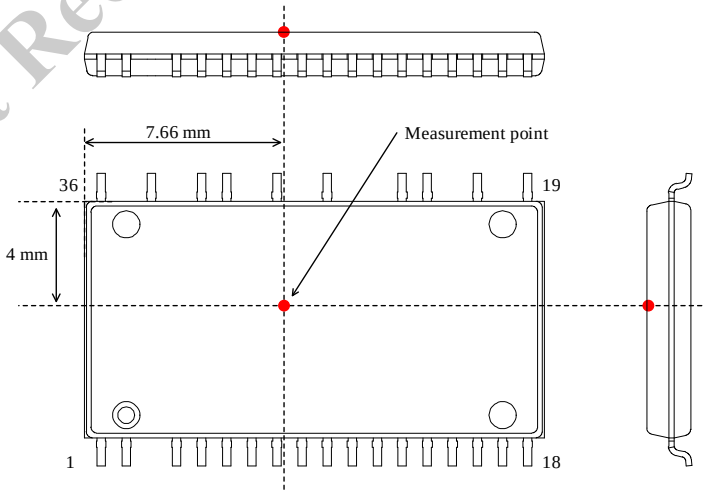


Figure 3-1. Case Temperature Measurement Point

3.4 Transistor Characteristics

Figure 3-2 provides the definitions of switching characteristics described in this and the following sections.

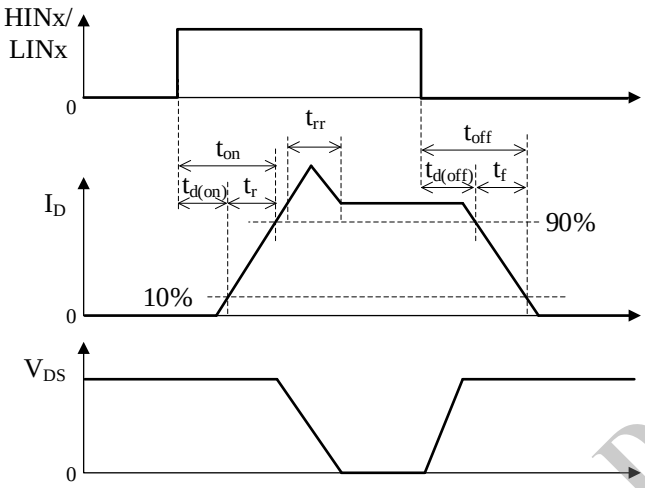


Figure 3-2. Switching Characteristics Definitions

3.4.1 SX68001MH

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 250 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.0 A, V_{IN} = 5 V	—	1.25	1.5	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =1.0 A, V_{IN} = 0 V	—	1.1	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, V_{CC} = 15 V, I_D = 1.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	75	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	800	—	ns
Rise Time	t_r		—	45	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	720	—	ns
Fall Time	t_f		—	40	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 150 V, V_{CC} = 15 V, I_D = 1.0 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	70	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	750	—	ns
Rise Time	t_r		—	50	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	660	—	ns
Fall Time	t_f		—	20	—	ns

3.4.2 SX68003MH

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 500 V, V_{IN} = 0 V	—	—	100	μA
Drain-to-Source On-resistance	$R_{DS(ON)}$	I_D = 1.25 A, V_{IN} = 5 V	—	2.0	2.4	Ω
Source-to-Drain Diode Forward Voltage	V_{SD}	I_{SD} =1.25 A, V_{IN} = 0 V	—	1.0	1.5	V
High-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 1.25 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	135	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	940	—	ns
Rise Time	t_r		—	100	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	975	—	ns
Fall Time	t_f		—	45	—	ns
Low-side Switching						
Source-to-Drain Diode Reverse Recovery Time	t_{rr}	V_{DC} = 300 V, V_{CC} = 15 V, I_D = 1.25 A, V_{IN} = 0→5 V or 5→0 V, T_J = 25 °C, inductive load	—	135	—	ns
Turn-on Delay Time	$t_{d(on)}$		—	900	—	ns
Rise Time	t_r		—	105	—	ns
Turn-off Delay Time	$t_{d(off)}$		—	905	—	ns
Fall Time	t_f		—	35	—	ns

4. Mechanical Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit	Remarks
Package Weight		—	1.4	—	g	

5. Truth Table

Table 5-1 is a truth table that provides the logic level definitions of operation modes.

In the case where HINx and LINx signals in each phase are high at the same time, both the high- and low-side transistors become on (simultaneous on-state). Therefore, HINx and LINx signals, the input signals for the HINx and LINx pins, require dead time setting so that such a simultaneous on-state event can be avoided.

After the IC recovers from a UVLO_VCC condition, the low-side transistors resume switching in accordance with the input logic levels of the LINx signals (level-triggered), whereas the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

After the IC recovers from a UVLO_VB condition, the high-side transistors resume switching at the next rising edge of an HINx signal (edge-triggered).

Table 5-1. Truth Table for Operation Modes

Mode	HINx	LINx	High-side Transistor	Low-side Transistor
Normal Operation	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	ON
	H	H	ON	ON
Shutdown Signal Input FO = “L”	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Undervoltage Lockout for High-side Power Supply (UVLO_VB)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	OFF
	H	H	OFF	OFF
Overcurrent Protection (OCP)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF
Overcurrent Limit (OCL) (OCL = SD)	L	L	OFF	OFF
	H	L	OFF	OFF
	L	H	OFF	ON
	H	H	OFF	ON
Thermal Shutdown (TSD)	L	L	OFF	OFF
	H	L	ON	OFF
	L	H	OFF	OFF
	H	H	ON	OFF

6. Block Diagram

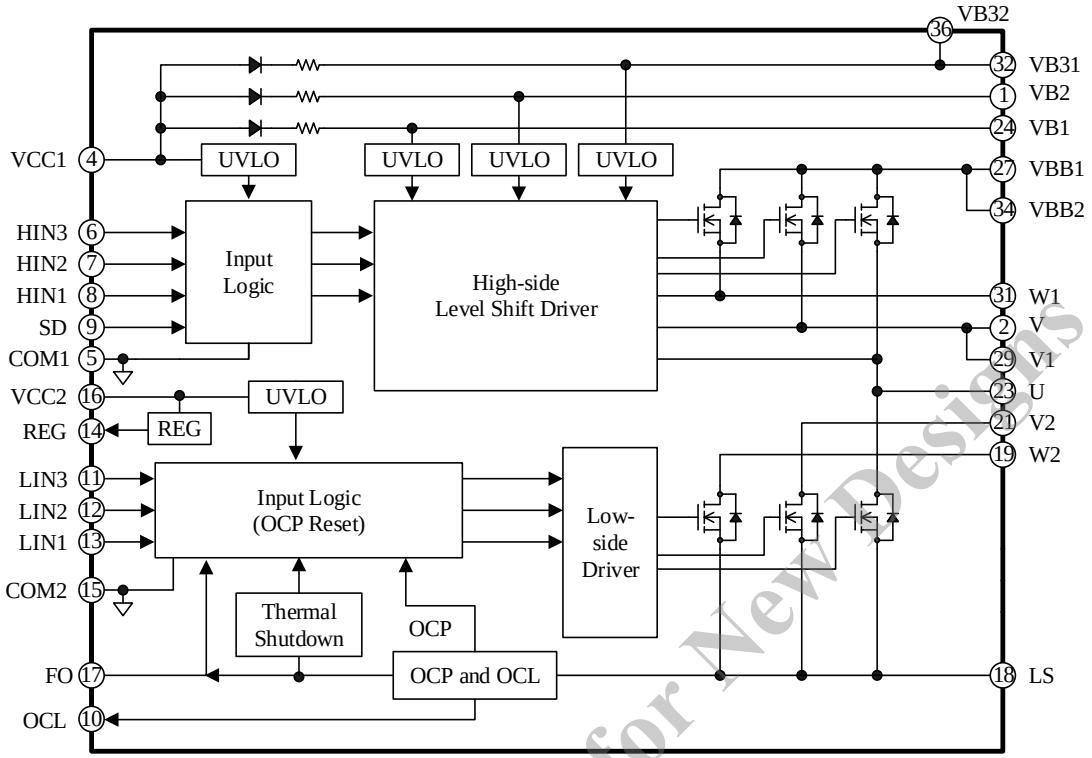
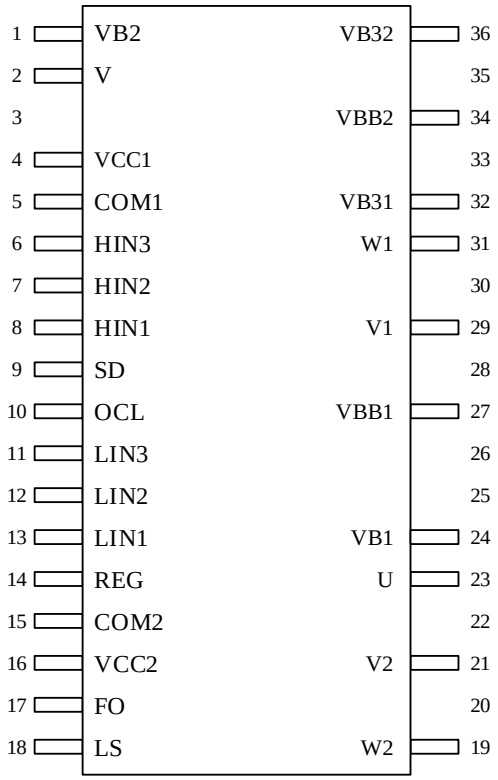


Figure 6-1. SX68000MH Block Diagram

7. Pin Configuration Definitions



Pin Number	Pin Name	Description
1	VB2	V-phase high-side floating supply voltage input
2	V	V-phase bootstrap capacitor connection
3	—	Pin removed
4	VCC1	High-side logic supply voltage input
5	COM1	High-side logic ground
6	HIN3	Logic input for W-phase high-side gate driver
7	HIN2	Logic input for V-phase high-side gate driver
8	HIN1	Logic input for U-phase high-side gate driver
9	SD	High-side shutdown signal input
10	OCL	Overcurrent limit signal input
11	LIN3	Logic input for W-phase low-side gate driver
12	LIN2	Logic input for V-phase low-side gate driver
13	LIN1	Logic input for U-phase low-side gate driver
14	REG	Regulator output
15	COM2	Low-side logic ground
16	VCC2	Low-side logic supply voltage input
17	FO	Fault signal output and shutdown signal input
18	LS	Power MOSFET source
19	W2	W-phase output (connected to W1 externally)
20	—	Pin removed
21	V2	V-phase output (connected to V1 externally)
22		Pin removed
23	U	U-phase output
24	VB1	U-phase high-side floating supply voltage input
25	—	Pin removed
26	—	Pin removed
27	VBB1	Positive DC bus supply voltage (connected to VBB2 externally)
28	—	Pin removed
29	V1	V-phase output (connected to V2 externally)
30	—	Pin removed
31	W1	W-phase output (connected to W2 externally)
32	VB31	W-phase high-side floating supply voltage input
33	—	Pin removed
34	VBB2	Positive DC bus supply voltage (connected to VBB1 externally)
35	—	Pin removed
36	VB32	W-phase high-side floating supply voltage input

8. Typical Application

CR filters and Zener diodes should be added to your application as needed. This is to protect each pin against surge voltages causing malfunctions, and to avoid the IC being used under the conditions exceeding the absolute maximum ratings where critical damage is inevitable. Then, check all the pins thoroughly under actual operating conditions to ensure that your application works flawlessly.

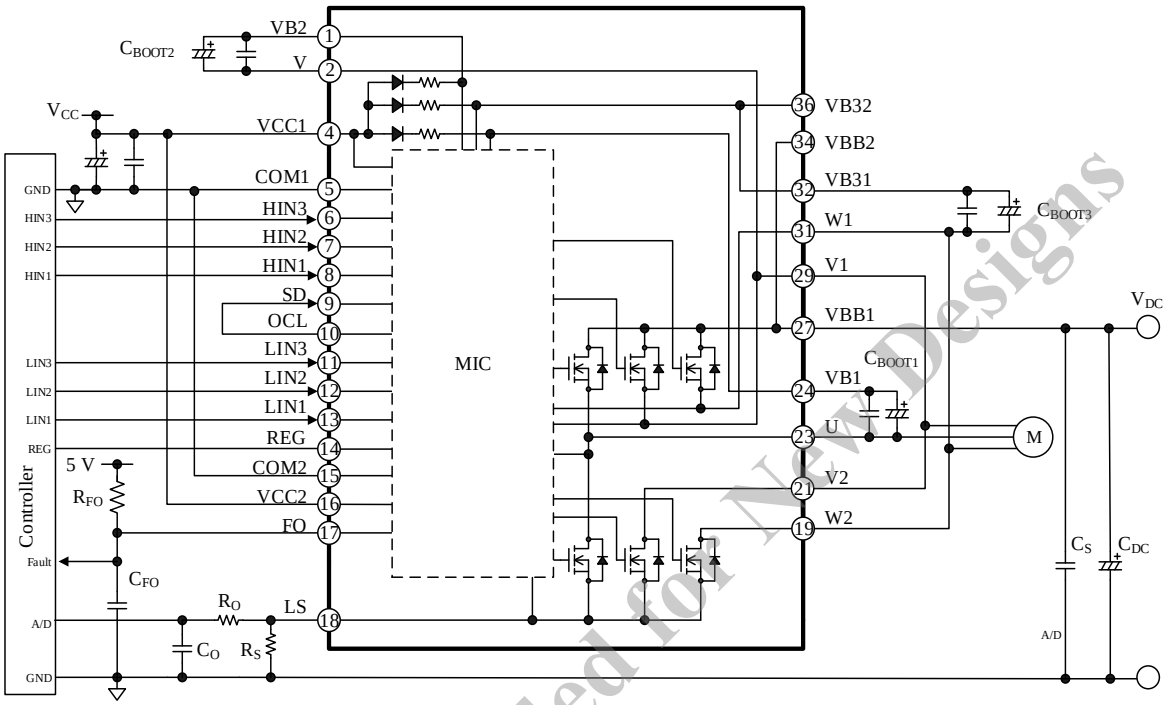
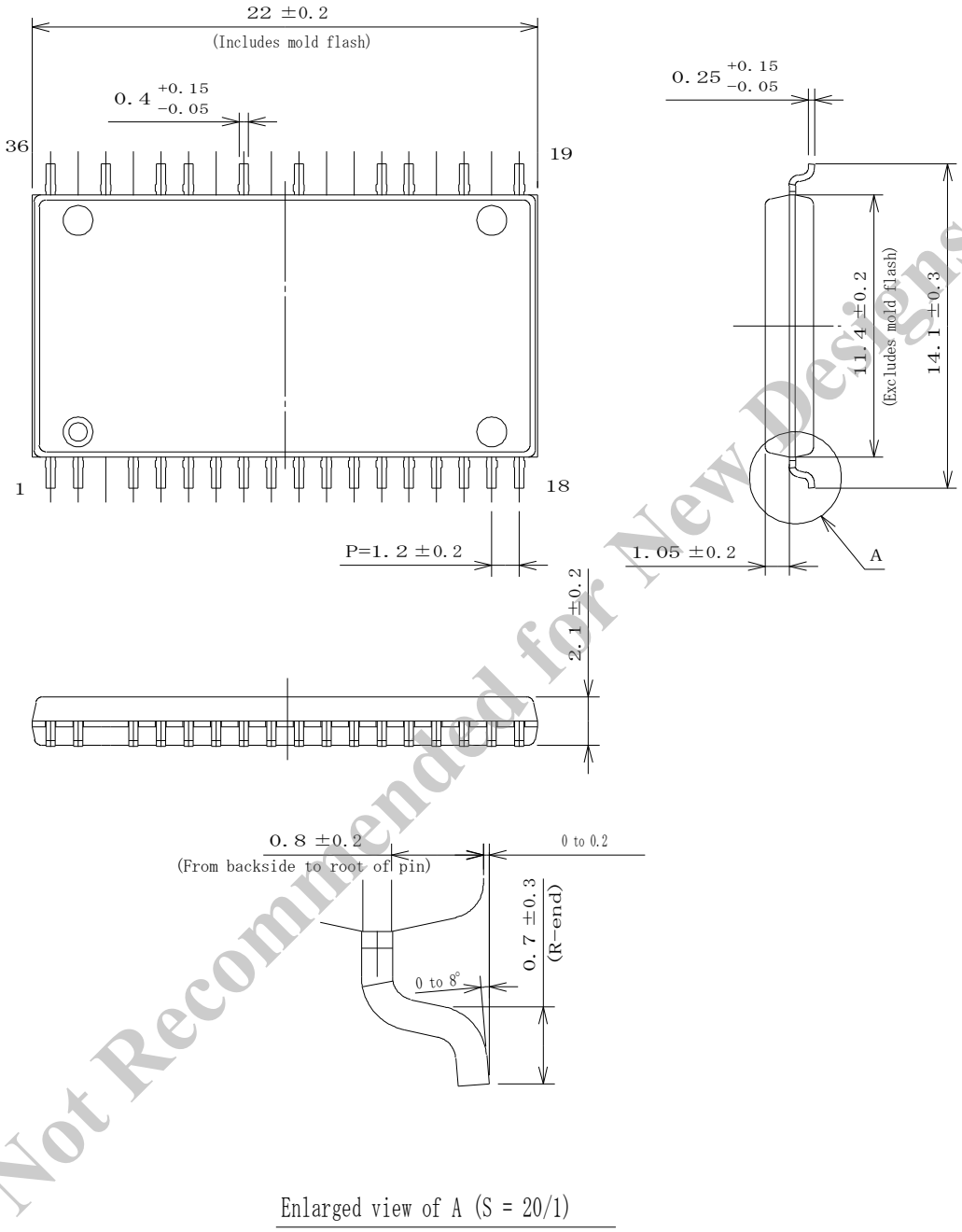


Figure 8-1. SX68000MH Typical Application

9. Physical Dimensions

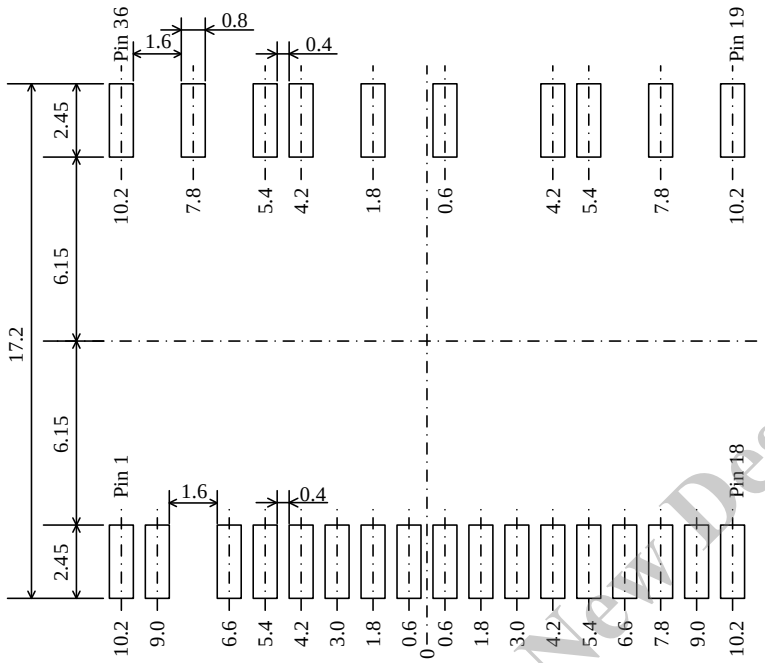
● **SOP36 Package**



NOTES:

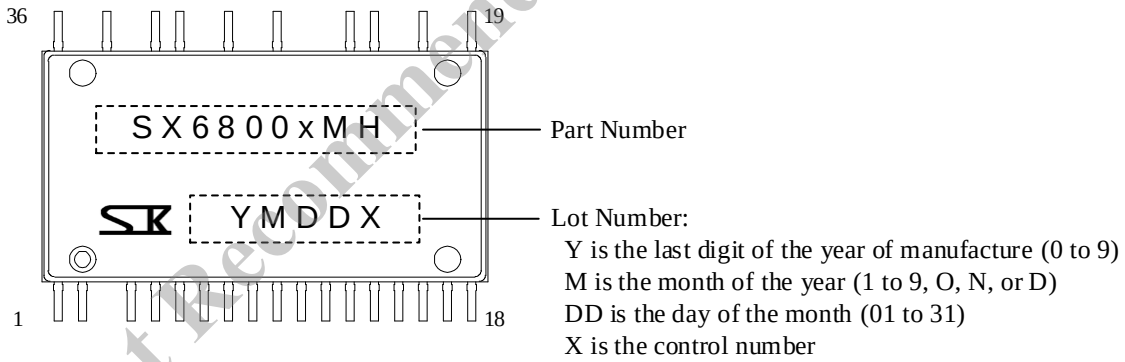
- Dimensions in millimeters
- Pb-free (RoHS compliant)
- Reflow (MSL3)
  Preheat: 180 °C / 90 ± 30 s
  Solder heating: 250 °C / 10 ± 1 s (260 °C peak, 2 times)

● **Land Pattern Example**



Unit: mm

10. Marking Diagram



11. Functional Descriptions

Unless specifically noted, this section uses the following definitions:

- All the characteristic values given in this section are typical values.
- For pin and peripheral component descriptions, this section employs a notation system that denotes a pin name with the arbitrary letter "x", depending on context. Thus, "the VCCx pin" is used when referring to either or both of the VCC1 and VCC2 pins.
- The COM1 pin is always connected to the COM2 pin.

11.1 Turning On and Off the IC

The procedures listed below provide recommended startup and shutdown sequences. To turn on the IC properly, do not apply any voltage on the VBBx, HINx, and LINx pins until the VCCx pin voltage has reached a stable state ($V_{CC(ON)} \geq 12.5$ V).

It is required to fully charge bootstrap capacitors, C_{BOOTx}, at startup (see Section 11.2.2).

To turn off the IC, set the HINx and LINx pins to logic low (or "L"), and then decrease the VCCx pin voltage.

11.2 Pin Descriptions

11.2.1 U, V, V1, V2, W1, and W2

These pins are the outputs of the three phases, and serve as the connection terminals to the 3-phase motor. Do not connect the 3-phase motor to the V pin. The V1 and W1 pins must be connected to the V2 and W2 pins on a PCB, respectively.

The U, V (V1), and W1 pins are the grounds for the VB1, VB2, and VB31 (VB32) pins.

The U, V, and W1 pins are connected to the negative nodes of bootstrap capacitors, C_{BOOTx}. The V pin is internally connected to the V1 pin.

Since high voltages are applied to these output pins (U, V, V1, V2, W1, and W2), it is required to take measures for insulating as follows:

- Keep enough distance between the output pins and low-voltage traces.
- Coat the output pins with insulating resin.

11.2.2 VB1, VB2, VB31, and VB32

These pins are connected to bootstrap capacitors for the high-side floating supply.

In actual applications, use either of the VB31 or VB32 pin because they are internally connected.

Voltages across the VBx and these output pins should be maintained within the recommended range (i.e., the Logic Supply Voltage, V_{BS}) given in Section 2.

A bootstrap capacitor, C_{BOOTx}, should be connected in each of the traces between the VB1 and U pins, the VB2 and V pins, the VB31 (VB32) and W1 pins.

For proper startup, turn on the low-side transistor first, then fully charge the bootstrap capacitor, C_{BOOTx}.

For the capacitance of the bootstrap capacitors, C_{BOOTx}, choose the values that satisfy Equations (1) and (2). Note that capacitance tolerance and DC bias characteristics must be taken into account when you choose appropriate values for C_{BOOTx}.

$$C_{BOOTx}(\mu F) > 800 \times t_{L(OFF)} \quad (1)$$

$$1\ \mu F \leq C_{BOOTx} \leq 220\ \mu F \quad (2)$$

In Equation (1), let $t_{L(OFF)}$ be the maximum off-time of the low-side transistor (i.e., the non-charging time of C_{BOOTx}), measured in seconds.

Even while the high-side transistor is off, voltage across the bootstrap capacitor keeps decreasing due to power dissipation in the IC. When the VBx pin voltage decreases to $V_{BS(OFF)}$ or less, the high-side undervoltage lockout (UVLO_VB) starts operating (see Section 11.3.3.1). Therefore, actual board checking should be done thoroughly to validate that voltage across the VBx pin maintains over 11.0 V ($V_{BS} > V_{BS(OFF)}$) during a low-frequency operation such as a startup period.

As Figure 11-1 shows, a bootstrap diode, D_{BOOTx}, and a current-limiting resistor, R_{BOOTx}, are internally placed in series between the VCC1 and VBx pins. Time constant for the charging time of C_{BOOTx}, τ, can be computed by Equation (3):

$$\tau = C_{BOOTx} \times R_{BOOTx}\ , \quad (3)$$

where C_{BOOTx} is the optimized capacitance of the bootstrap capacitor, and R_{BOOTx} is the resistance of the current-limiting resistor (60 Ω ± 20%).

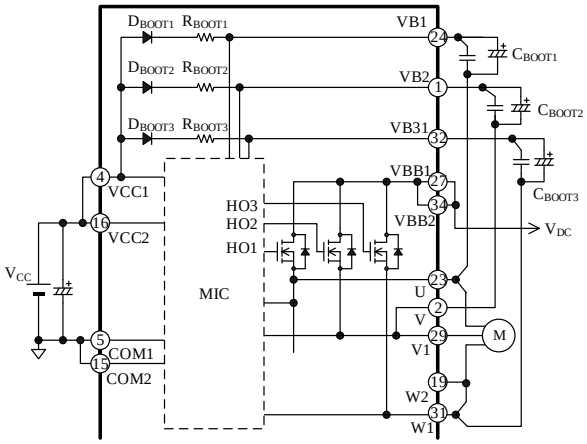


Figure 11-1. Bootstrap Circuit

Figure 11-2 shows an internal level-shifting circuit. A high-side output signal, HOx, is generated according to an input signal on the HINx pin. When an input signal on the HINx pin transits from low to high (rising edge), a "Set" signal is generated. When the HINx input signal transits from high to low (falling edge), a "Reset" signal is generated. These two signals are then transmitted to the high-side by the level-shifting circuit and are input to the SR flip-flop circuit. Finally, the SR flip-flop circuit feeds an output signal, Q (i.e., HOx).

Figure 11-3 is a timing diagram describing how noise or other detrimental effects will improperly influence the level-shifting process. When a noise-induced rapid voltage drop between the VBx and output pins (U, V/V1, or W1; hereafter "VBx–HSx") occurs after the Set signal generation, the next Reset signal cannot be sent to the SR flip-flop circuit. And the state of an HOx signal stays logic high (or "H") because the SR flip-flop does not respond. With the HOx state being held high (i.e., the high-side transistor is in an on-state), the next LINx signal turns on the low-side transistor and causes a simultaneously-on condition, which may result in critical damage to the IC. To protect the VBx pin against such a noise effect, add a bootstrap capacitor, C_{BOOTx}, in each phase. C_{BOOTx} must be placed near the IC and be connected between the VBx and HSx pins with a minimal length of traces. To use an electrolytic capacitor, add a 0.01 µF to 0.1 µF bypass capacitor, C_{Px}, in parallel near these pins used for the same phase.

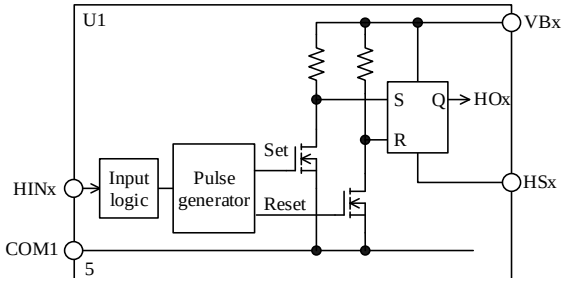


Figure 11-2. Internal Level-shifting Circuit

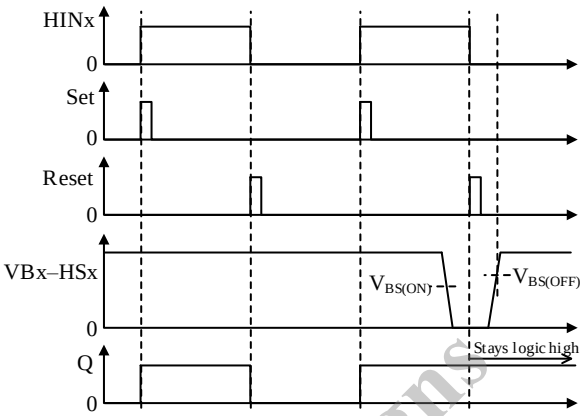


Figure 11-3. Waveforms at VBx-HSx Voltage Drop

11.2.3 VCC1 and VCC2

These are the logic power supply pins for the built-in control MIC. The VCC1 and VCC2 pins must be externally connected on a PCB because they are not internally connected. To prevent malfunction induced by supply ripples or other factors, put a 0.01 µF to 0.1 µF ceramic capacitor, C_{VCC}, near these pins. To prevent damage caused by surge voltages, put an 18 V to 20 V Zener diode, DZ, between the VCCx and COMx pins.

Voltages to be applied between the VCCx and COMx pins should be regulated within the recommended operational range of V_{CC}, given in Section 2.

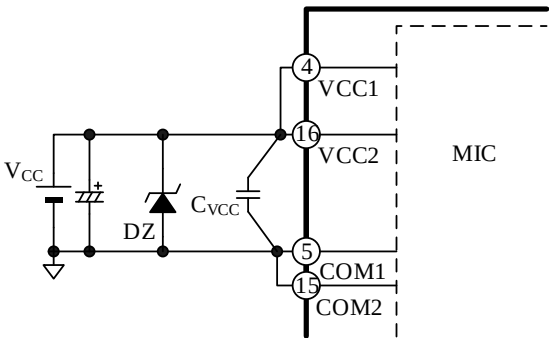


Figure 11-4. VCCx Pin Peripheral Circuit

11.2.4 COM1 and COM2

These are the logic ground pins for the built-in control MIC. The COM1 and COM2 pins should be connected externally on a PCB because they are not internally connected. Varying electric potential of the logic ground can be a cause of improper operations. Therefore, connect the logic ground as close and short as possible to shunt resistors, R_S, at a single-point ground (or star ground) which is separated from the power ground (see Figure 11-5).

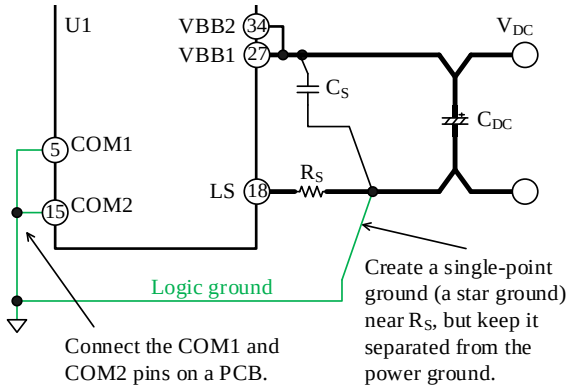


Figure 11-5. Connections to Logic Ground

11.2.5 REG

This is the 7.5 V regulator output pin, which can be used for a power supply of an external logic IC (e.g., Hall IC). A maximum output current of the REG pin is 35 mA. To stabilize the REG pin output, connect the pin to a capacitor of about 0.1 µF.

11.2.6 HIN1, HIN2, and HIN3; LIN1, LIN2, and LIN3

These are the input pins of the internal motor drivers for each phase. The HINx pin acts as a high-side controller; the LINx pin acts as a low-side controller.

Figure 11-6 shows an internal circuit diagram of the HINx or LINx pin. This is a CMOS Schmitt trigger circuit with a built-in 20 kΩ pull-down resistor, and its input logic is active high.

Input signals applied across the HINx–COMx and the LINx–COMx pins in each phase should be set within the ranges provided in Table 11-1, below. Note that dead time setting must be done for HINx and LINx signals because the IC does not have a dead time generator.

The higher PWM carrier frequency rises, the more switching loss increases. Hence, the PWM carrier frequency must be set so that operational case temperatures and junction temperatures have sufficient margins against the absolute maximum ranges, specified in Section 1.

If the signals from the microcontroller become unstable, the IC may result in malfunctions. To avoid this event, the outputs from the microcontroller output line should not be high impedance. Also, if the traces from the microcontroller to the HINx or LINx pin (or both) are too long, the traces may be interfered by noise. Therefore, it is recommended to add an additional filter or a pull-down resistor near the HINx or LINx pin as needed (see Figure 11-7).

Here are filter circuit constants for reference:
R_{IN1x}: 33 Ω to 100 Ω
R_{IN2x}: 1 kΩ to 10 kΩ
C_{INx}: 100 pF to 1000 pF

Care should be taken when adding R_{IN1x} and R_{IN2x} to the traces. When they are connected to each other, the input voltage of the HINx and LINx pins becomes slightly lower than the output voltage of the microcontroller.

Table 11-1. Input Signals for HINx and LINx Pins

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	≥0.5 µs	≥0.5 µs
PWM Carrier Frequency	≤20 kHz	
Dead Time	≥1.5 µs	

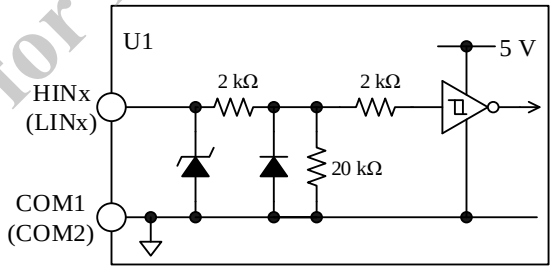


Figure 11-6. Internal Circuit Diagram of HINx or LINx Pin

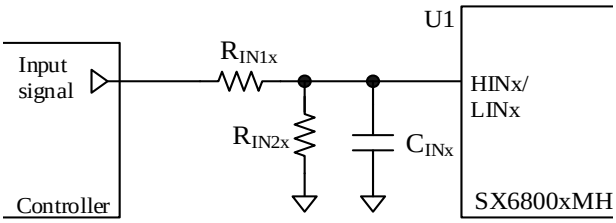


Figure 11-7. Filter Circuit for HINx or LINx Pin

11.2.7 VBB1 and VBB2

These are the input pins for the main supply voltage, i.e., the positive DC bus. All of the power MOSFET drains of the high-side are connected to these pins. Voltages between the VBBx and COM2 pins should be set within the recommended range of the main supply voltage, V_{DC}, given in Section 2.

The VBB1 and VBB2 pins should be connected externally on a PCB. To suppress surge voltages, put a

0.01 µF to 0.1 µF bypass capacitor, C_S, near the VBBx pin and an electrolytic capacitor, C_{DC}, with a minimal length of PCB traces to the VBBx pin.

11.2.8 LS

This pin is internally connected to the power MOSFET source in each phase and the overcurrent protection (OCP) circuit. For current detection, the LS pin should be connected externally on a PCB via a shunt resistor, R_S, to the COMx pin.

For more details on the OCP, see Section 11.3.5.

When connecting the shunt resistor, place it as near as possible to the IC with a minimum length of traces to the LS and COMx pins. Otherwise, malfunction may occur because a longer circuit trace increases its inductance and thus increases its susceptibility to improper operations. In applications where long PCB traces are required, add a fast recovery diode, D_{RS}, between the LS and COMx pins in order to prevent the IC from malfunctioning.

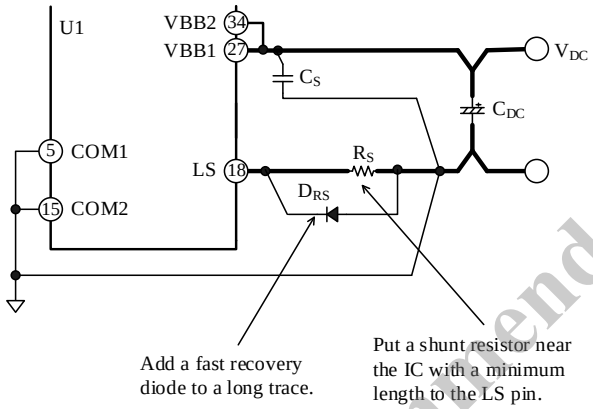


Figure 11-8. Connections to LS Pin

11.2.9 OCL

The OCL pin serves as the output of the overcurrent protections which monitor the currents going through the output transistors. In normal operation, the OCL pin logic level is low. If the OCL pin is connected to the SD pin so that the SD pin will respond to an OCL output signal, the high-side transistors can be turned off when the protections (OCP and OCL) are activated.

11.2.10 SD

When a 5 V or 3.3 V signal is input to the SD pin, the high-side transistors turn off independently of any HINx signals. This is because the SD pin does not respond to a pulse shorter than an internal filter of 3.3 µs (typ.).

The SD–OCL pin connection, as described in Section 11.2.9, allows the IC to turn off the high-side transistors at OCL or OCP activation. Also, inputting the inverted signal of the FO pin to the SD pin permits all the high- and low-side transistors to turn off, when the IC detects an abnormal condition (i.e., some or all of the protections such as TSD, OCP, and UVLO are activated).

11.2.11 FO

This pin operates as the fault signal output and the low-side shutdown signal input. Sections 11.3.1 and 11.3.2 explain the two functions in detail, respectively. Figure 11-9 illustrates an internal circuit diagram of the FO pin and its peripheral circuit.

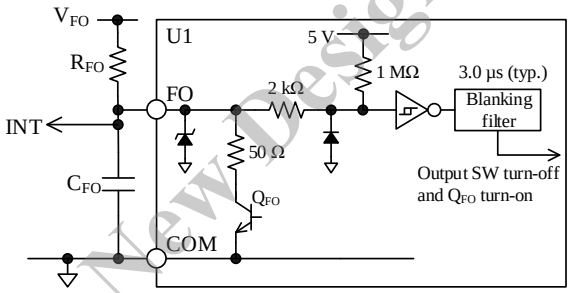


Figure 11-9. Internal Circuit Diagram of FO Pin and Its Peripheral Circuit

Because of its open-collector nature, the FO pin should be tied by a pull-up resistor, R_{FO}, to the external power supply. The external power supply voltage (i.e., the FO Pin Pull-up Voltage, V_{FO}) should range from 3.0 V to 5.5 V.

When the pull-up resistor, R_{FO}, has a too small resistance, the FO pin voltage at fault signal output becomes high due to the saturation voltage drop of a built-in transistor, Q_{FO}. Therefore, it is recommended to use a 3.3 kΩ to 10 kΩ pull-up resistor.

To suppress noise, add a filter capacitor, C_{FO}, near the IC with minimizing a trace length between the FO and COMx pins.

To avoid the repetition of OCP activations, the external microcontroller must shut off any input signals to the IC within an OCP hold time, t_P, which occurs after the internal MOSFET (Q_{FO}) turn-on. t_P is 20 µs where minimum values of thermal characteristics are taken into account. (For more details, see Section 11.3.5.) Our recommendation is to use a 0.001 µF to 0.01 µF filter capacitor.

11.3 Protections

This section describes the various protection circuits provided in the SX68000MH series. The protection circuits include the undervoltage lockout for power supplies (UVLO), the overcurrent protection (OCP), and the thermal shutdown (TSD).

In case one or more of these protection circuits are activated, the FO pin outputs a fault signal; as a result, the external microcontroller can stop the operations of the three phases by receiving the fault signal. The external microcontroller can also shut down IC operations by inputting a fault signal to the FO pin.

In the following functional descriptions, "HOx" denotes a gate input signal on the high-side transistor, whereas "LOx" denotes a gate input signal on the low-side transistor. "VBx–HSx" refers to the voltages between the VBx pin and output pins (U, V/V1, and W1).

11.3.1 Fault Signal Output

In case one or more of the following protections are actuated, an internal transistor, Q_{FO}, turns on, then the FO pin becomes logic low (≤0.5 V).

- Low-side undervoltage lockout (UVLO_VCC)
- Overcurrent protection (OCP)
- Thermal shutdown (TSD)

While the FO pin is in the low state, all the low-side transistors turn off. In normal operation, the FO pin outputs a high signal of 5 V. OCP The fault signal output time of the FO pin at OCP activation is the OCP hold time (t_P) of 25 µs (typ.), fixed by a built-in feature of the IC itself (see Section 11.3.5). The external microcontroller receives the fault signals with its interrupt pin (INT), and must be programmed to put the HINx and LINx pins to logic low within the predetermined OCP hold time, t_P.

11.3.2 Shutdown Signal Input

The FO pin also acts as the input pin of shutdown signals. When the FO pin becomes logic low, all the low-side transistors turn off. The voltages and pulse widths of the shutdown signals to be applied between the FO and COMx pins are listed in Table 11-2.

Table 11-2. Shutdown Signals

Parameter	High Level Signal	Low Level Signal
Input Voltage	3 V < V_{IN} < 5.5 V	0 V < V_{IN} < 0.5 V
Input Pulse Width	—	≥6 µs

11.3.3 Undervoltage Lockout for Power Supply (UVLO)

In case the gate-driving voltages of the output transistors decrease, their steady-state power dissipations increase. This overheating condition may cause permanent damage to the IC in the worst case. To prevent this event, the SX68000MH series has the undervoltage lockout (UVLO) circuits for both of the high- and low-side power supplies.

11.3.3.1. Undervoltage Lockout for High-side Power Supply (UVLO_VB)

Figure 11-10 shows operational waveforms of the undervoltage lockout for high-side power supply (i.e., UVLO_VB).

When the voltage between the VBx and output pins (VBx–HSx) decreases to the Logic Operation Stop Voltage ($V_{BS(OFF)}$ = 10.0 V) or less, the UVLO_VB circuit in the corresponding phase gets activated and sets an HOx signal to logic low.

When the voltage between the VBx and HSx pins increases to the Logic Operation Start Voltage ($V_{BS(ON)}$ = 10.5 V) or more, the IC releases the UVLO_VB operation. Then, the HOx signal becomes logic high at the rising edge of the first input command after the UVLO_VB release.

Any fault signals are not output from the FO pin during the UVLO_VB operation. In addition, the VBx pin has an internal UVLO_VB filter of about 3 µs, in order to prevent noise-induced malfunctions.

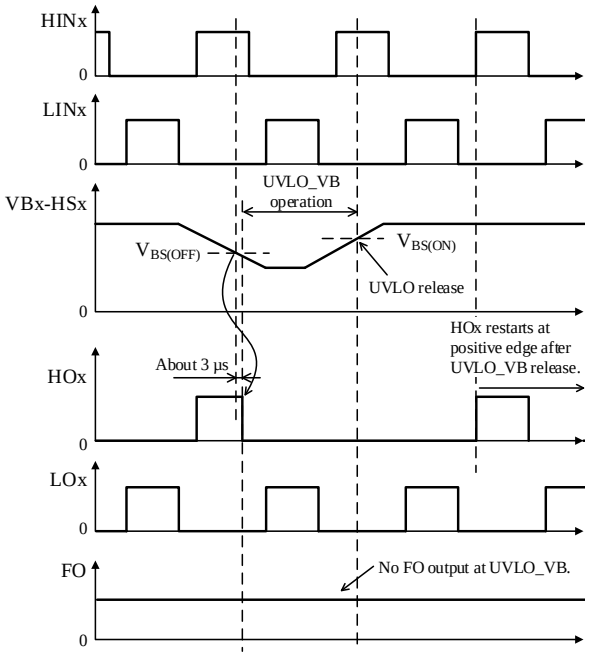


Figure 11-10. UVLO_VB Operational Waveforms

11.3.3.2. Undervoltage Lockout for Low-side Power Supply (UVLO_VCC)

Figure 11-11 shows operational waveforms of the undervoltage lockout for low-side power supply (i.e., UVLO_VCC).

When the VCC2 pin voltage decreases to the Logic Operation Stop Voltage ($V_{CC(OFF)}$ = 11.0 V) or less, the UVLO_VCC circuit in the corresponding phase gets activated and sets both of HOx and LOx signals to logic low. When the VCC2 pin voltage increases to the Logic Operation Start Voltage ($V_{CC(ON)}$ = 11.5 V) or more, the IC releases the UVLO_VCC operation.

Then, the IC resumes the following transmissions: an LOx signal according to an LINx pin input command; an HOx signal according to the rising edge of the first HINx pin input command after the UVLO_VCC release. During the UVLO_VCC operation, the FO pin becomes logic low and sends fault signals.

In addition, the VCC2 pin has an internal UVLO_VCC filter of about 3 µs, in order to prevent noise-induced malfunctions.

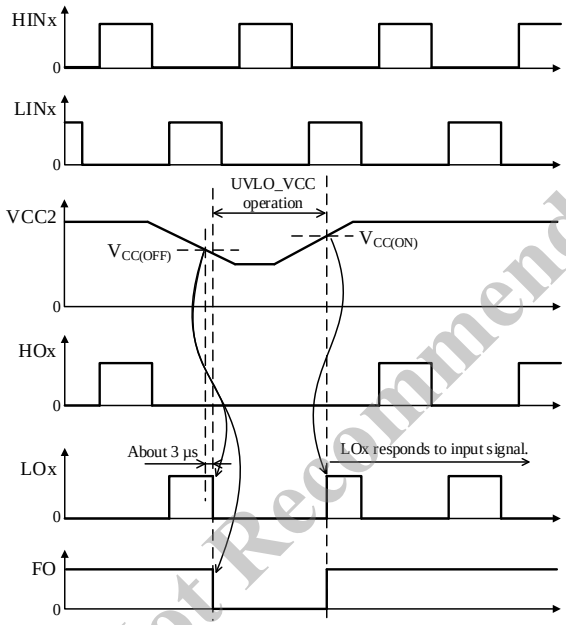


Figure 11-11. UVLO_VCC Operational Waveforms

11.3.4 Overcurrent Limit (OCL)

The overcurrent limit (OCL) is a protection against relatively low overcurrent conditions.

Figure 11-12 shows an internal circuit of the OCL pin; Figure 11-13 shows OCL operational waveforms.

When the LS pin voltage increases to the Current Limit Reference Voltage (V_{LIM} = 0.6500 V) or more, and remains in this condition for a period of the Current Limit Blanking Time ($t_{BK(OCP)}$ = 2 µs) or longer, the OCL circuit is activated. Then, the OCL pin goes logic high.

During the OCL operation, the gate logic levels of the low-side transistors respond to an input command on the LINx pin.

To turn off the high-side transistors during the OCL operation, connect the OCL and SD pins on a PCB. The SD pin has an internal filter of about 3.3 µs (typ.).

When the LS pin voltage falls below V_{LIM} (0.6500 V), the OCL pin logic level becomes low.

After the OCL pin logic has become low, the high-side transistors remain turned off until the first low-to-high transition on an HINx input signal occurs (i.e., edge-triggered).

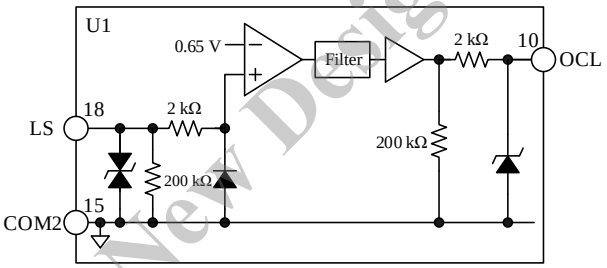


Figure 11-12. Internal Circuit Diagram of OCL Pin

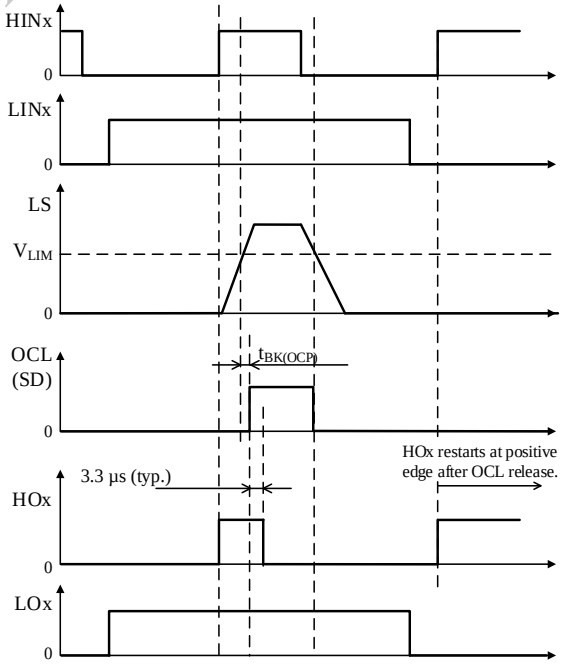


Figure 11-13. OCL Operational Waveforms (OCL = SD)

11.3.5 Overcurrent Protection (OCP)

The overcurrent protection (OCP) is a protection against large inrush currents (i.e., high di/dt). Figure 11-14 is an internal circuit diagram describing the LS pin and its peripheral circuit. The OCP circuit, which is connected to the LS pin, detects overcurrents with voltage across an external shunt resistor, R_S. Because the LS pin is internally pulled down, the LS pin voltage increases proportionally to a rise in the current running through the shunt resistor, R_S.

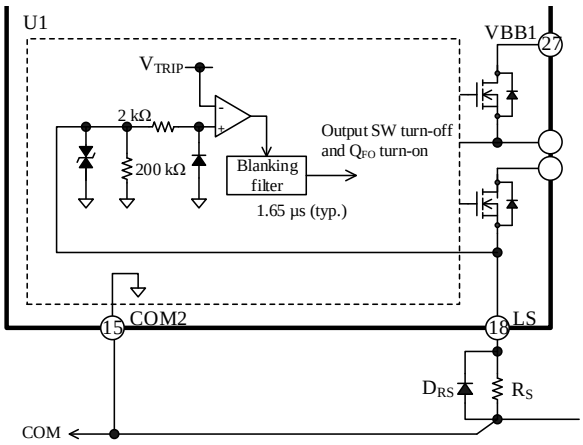


Figure 11-14. Internal Circuit Diagram of LS Pin and Its Peripheral Circuit

Figure 11-15 is a timing chart that represents operation waveforms during OCP operation. When the LS pin voltage increases to the OCP Threshold Voltage (V_{TRIP} = 1.0 V) or more, and remains in this condition for a period of the OCP Blanking Time (t_{BK} = 2 µs) or longer, the OCP circuit is activated.

The enabled OCP circuit shuts off the low-side transistors, and puts the FO pin into a low state.

Then, output current decreases as a result of the output transistors turn-off. Even if the OCP pin voltage falls below V_{TRIP}, the IC holds the FO pin in the low state for a fixed OCP hold time (t_P) of 25 µs (typ.). Then, the output transistors operate according to input signals.

The OCP is used for detecting abnormal conditions, such as an output transistor shorted. In case short-circuit conditions occur repeatedly, the output transistors can be destroyed. To prevent such event, motor operation must be controlled by the external microcontroller so that it can immediately stop the motor when fault signals are detected. To resume IC operations thereafter, set the IC to be resumed after a lapse of ≥2 seconds.

For proper shunt resistor setting, your application must meet the following:

- Use the shunt resistor that has a recommended resistance, R_S (see Section 2).
- Set the LS pin input voltage to vary within the rated LS pin voltages, V_{LS} (see Section 1).
- Keep the current through the output transistors below the rated output current (pulse), I_{OP} (see Section 1).

It is required to use a resistor with low internal inductance because high-frequency switching current will flow through the shunt resistor, R_S. In addition, choose a resistor with allowable power dissipation according to your application.

Note that overcurrents are undetectable when one or more of the U, V/V1/V2, and W1/W2 pins or their traces are shorted to ground (ground fault). In case any of these pins falls into a state of ground fault, the output transistors may be destroyed.

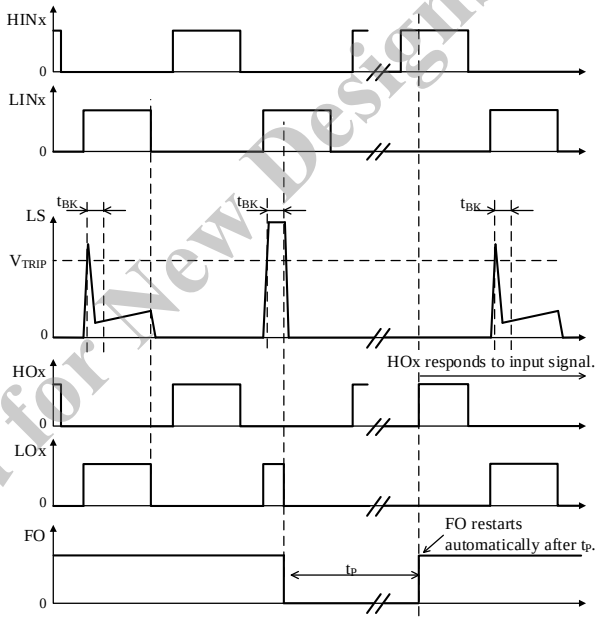


Figure 11-15. OCP Operational Waveforms

11.3.6 Thermal Shutdown (TSD)

The SX68000MH series incorporates the thermal shutdown (TSD) circuit. Figure 11-16 shows TSD operational waveforms. In case of overheating (e.g., increased power dissipation due to overload, or elevated ambient temperature at the device), the IC shuts down the low-side output transistors.

The TSD circuit in the MIC monitors temperatures (see Section 6). When the temperature of the MIC exceeds the TSD Operating Temperature (T_{DH} = 150 °C), the TSD circuit is activated. When the temperature of the MIC decreases to the TSD Releasing Temperature (T_{DL} = 120 °C) or less, the shutdown operation is released. The transistors then resume operating according to input signals. During the TSD operation, the FO pin becomes logic low and transmits fault signals. Note that junction temperatures of the output transistors themselves are not monitored; therefore, do not use the TSD function as an overtemperature prevention for the output transistors.

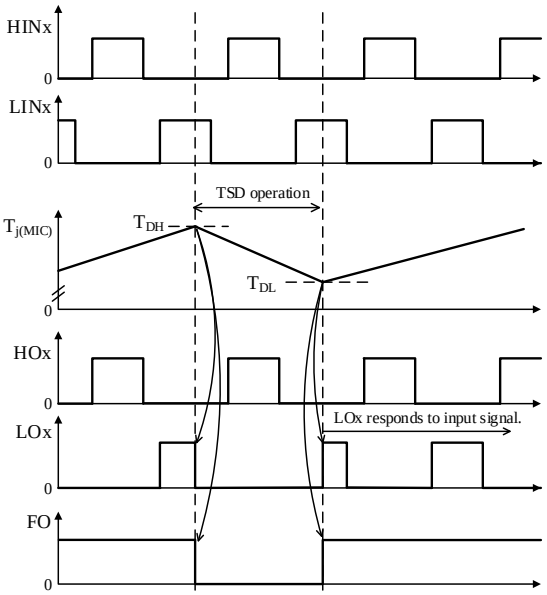


Figure 11-16. TSD Operational Waveforms

12. Design Notes

12.1 PCB Pattern Layout

Figure 12-1 shows a schematic diagram of a motor drive circuit. The circuit consists of current paths having high frequencies and high voltages, which also bring about negative influences on IC operation, noise interference, and power dissipation. Therefore, PCB trace layouts and component placements play an important role in circuit designing.

Current loops, which have high frequencies and high voltages, should be as small and wide as possible, in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that radiated EMI levels can be reduced.

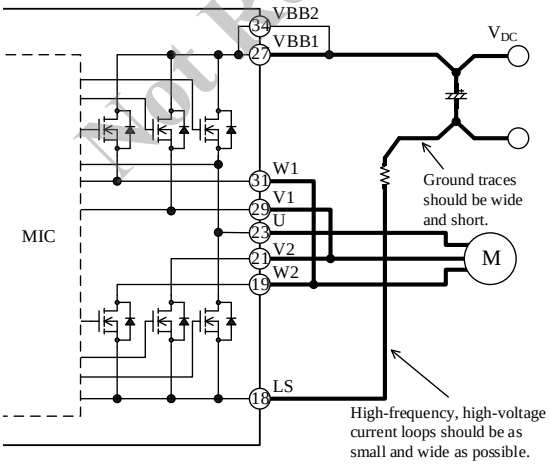


Figure 12-1. High-frequency, High-voltage Current Paths

12.2 Considerations in IC Characteristics Measurement

When measuring the breakdown voltage or leakage current of the transistors incorporated in the IC, note that the gate and emitter (source) of each transistor should have the same potential. Moreover, care should be taken during the measurement because each transistor is connected as follows:

- All the high-side transistors (drains) are internally connected to the VBBx pin.
- In the U-phase, the high-side transistor (source) and the low-side toransistor (drain) are internally connected, and are also connected to the U pin.
  (In the V- and W-phases, the high- and low-side transistors are unconnected inside the IC.)

The gates of the high-side transistors are pulled down to the corresponding output (U, V/V1, and W1) pins; similarly, the gates of the low-side transistors are pulled down to the COM2 pin.

When measuring the breakdown voltage or leakage current of the transistors, note that all of the output (U, V/V1/V2, and W1/W2), LS, and COMx pins must be appropriately connected. Otherwise, the switching transistors may result in permanent damage.

The following are circuit diagrams representing typical measurement circuits for breakdown voltage: Figure 12-2 shows the high-side transistor (Q_{UH}) in the U-phase; Figure 12-3 shows the low-side transistor (Q_{UL}) in the U-phase. And all the pins that are not represented in these figures are open.

When measuring the high-side transistors, leave all the pins not be measured open. When measuring the low-side transistors, connect the LS pin to be measured to the COMx pin, then leave other unused pins open.

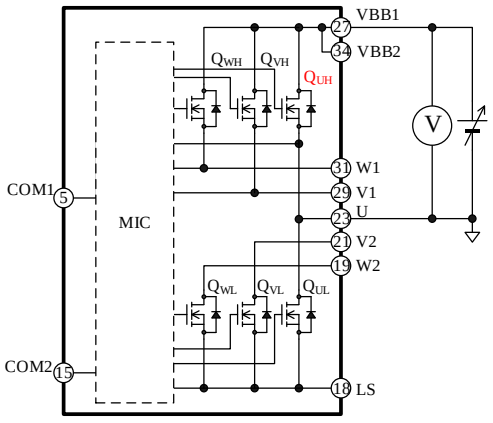


Figure 12-2. Typical Measurement Circuit for High-side Transistor (Q_{UH}) in U-phase

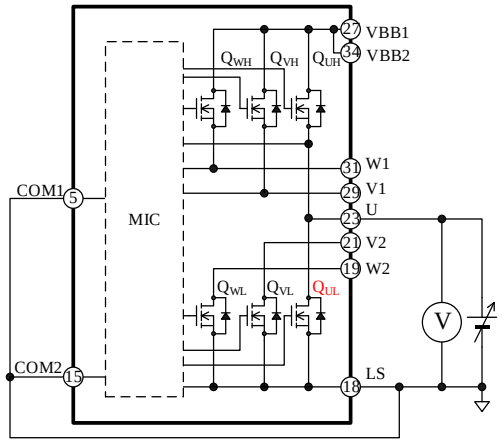


Figure 12-3. Typical Measurement Circuit for Low-side Transistor (Q_{UL}) in U-phase

13. Calculating Power Losses and Estimating Junction Temperature

This section describes the procedures to calculate power losses in switching transistors, and to estimate a junction temperature. Note that the descriptions listed here are applicable to the SX68000MH series, which is controlled by a 3-phase sine-wave PWM driving strategy.

For quick and easy references, we offer calculation support tools online. Please visit our website to find out more.

- DT0050: SX68000MH Calculation Tool
  http://www.semicon.sanken-ele.co.jp/en/calc-tool/mosfet_caltool_en.html

13.1 Power MOSFET

Total power loss in a power MOSFET can be obtained by taking the sum of the following losses: steady-state loss, P_{RON}; switching loss, P_{SW}; the steady-state loss of a body diode, P_{SD}. In the calculation procedure we offer, the recovery loss of a body diode, PRR, is considered negligibly small compared with the ratios of other losses.

The following subsections contain the mathematical procedures to calculate these losses (P_{RON}, P_{SW}, and P_{SD}) and the junction temperature of all power MOSFETs operating.

13.1.1 Power MOSFET Steady-state Loss, P_{RON}

Steady-state loss in a power MOSFET can be computed by using the $R_{DS(ON)}$ vs. I_D curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-1, linear approximations at a range the ID is actually used are obtained by: $R_{DS(ON)} = \alpha \times ID + \beta$. The values gained by the above calculation are then applied as parameters in Equation (4), below. Hence, the equation to obtain the power MOSFET steady-state loss, P_{RON}, is:

$$P_{RON} = \frac{1}{2\pi}\int_0^{\pi} I_D(\varphi)^2 \times R_{DS(ON)}(\varphi) \times DT \times d\varphi$$

$$= 2\sqrt{2}\alpha\left(\frac{1}{3\pi} + \frac{3}{32}M \times \cos\theta\right) {I_M}^3 + 2\beta\left(\frac{1}{8} + \frac{1}{3\pi}M \times \cos\theta\right) {I_M}^2 . \quad (4)$$

Where:

I_D is the drain current of the power MOSFET (A),
$R_{DS(ON)}$ is the drain-to-source on-resistance of the power MOSFET (Ω),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
cosθ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve, and
β is the intercept of the linear approximation in the $R_{DS(ON)}$ vs. I_D curve.

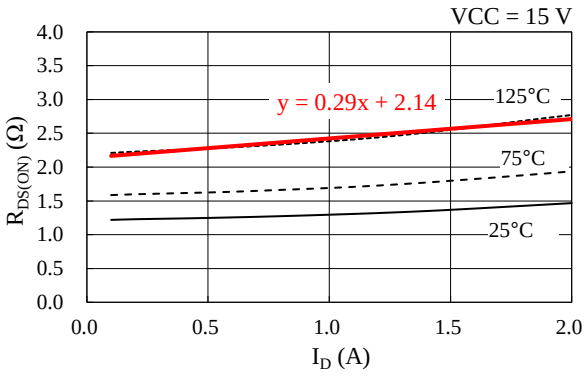


Figure 13-1. Linear Approximate Equation of $R_{DS(ON)}$ vs. I_D Curve

13.1.2 Power MOSFET Switching Loss, P_{SW}

Switching loss in a power MOSFET can be calculated by Equation (5) or (6), letting I_M be the effective current value of the motor.

- **SX68001MH**

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{150}. \quad (5)$$

- **SX68003MH**

$$P_{SW} = \frac{\sqrt{2}}{\pi} \times f_C \times \alpha_E \times I_M \times \frac{V_{DC}}{300}. \quad (6)$$

Where:
f_C is the PWM carrier frequency (Hz),
V_{DC} is the main power supply voltage (V), i.e., the VBBx pin input voltage, and
α_E is the slope on the switching loss curve (see Section 14.3.2).

13.1.3 Body Diode Steady-state Loss, P_{SD}

Steady-state loss in the body diode of a power MOSFET can be computed by using the V_{SD} vs. I_{SD} curves, listed in Section 14.3.1. As expressed by the curves in Figure 13-2, linear approximations at a range the I_{SD} is actually used are obtained by: $V_{SD} = \alpha \times I_{SD} + \beta$.

The values gained by the above calculation are then applied as parameters in Equation (7), below. Hence, the equation to obtain the body diode steady-state loss, P_{SD}, is:

$$P_{SD} = \frac{1}{2\pi}\int_0^{\pi} V_{SD}(\varphi) \times I_{SD}(\varphi) \times (1 - DT) \times d\varphi$$

$$= \frac{1}{2}\alpha\left(\frac{1}{2} - \frac{4}{3\pi}M \times \cos\theta\right) {I_M}^2 + \frac{\sqrt{2}}{\pi}\beta\left(\frac{1}{2} - \frac{\pi}{8}M \times \cos\theta\right) I_M . \quad (7)$$

Where:
V_{SD} is the source-to-drain diode forward voltage of the power MOSFET (V),
I_{SD} is the source-to-drain diode forward current of the power MOSFET (A),
DT is the duty cycle, which is given by

$$DT = \frac{1 + M \times \sin(\varphi + \theta)}{2},$$

M is the modulation index (0 to 1),
$\cos\theta$ is the motor power factor (0 to 1),
I_M is the effective motor current (A),
α is the slope of the linear approximation in the V_{SD} vs. I_{SD} curve, and
β is the intercept of the linear approximation in the V_{SD} vs. I_{SD} curve.

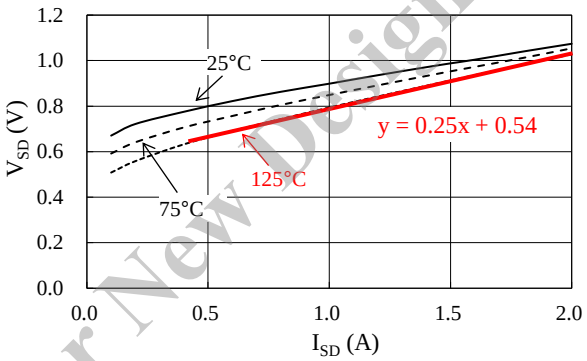


Figure 13-2. Linear Approximate Equation of V_{SD} vs. I_{SD} Curve

13.1.4 Estimating Junction Temperature of Power MOSFET

The junction temperature of all power MOSFETs operating, T_J, can be estimated with Equation (8):

$$T_J = R_{J-C} \times \{(P_{RON} + P_{SW} + P_{SD}) \times 6\} + T_C . \quad (8)$$

Where:
R_{J-C} is the junction-to-case thermal resistance (°C/W) of all the power MOSFETs operating, and
T_C is the case temperature (°C), measured at the point defined in Figure 3-1.

14. Performance Curves

14.1 Transient Thermal Resistance Curves

The following graphs represent transient thermal resistance (the ratios of transient thermal resistance), with steady-state thermal resistance = 1.

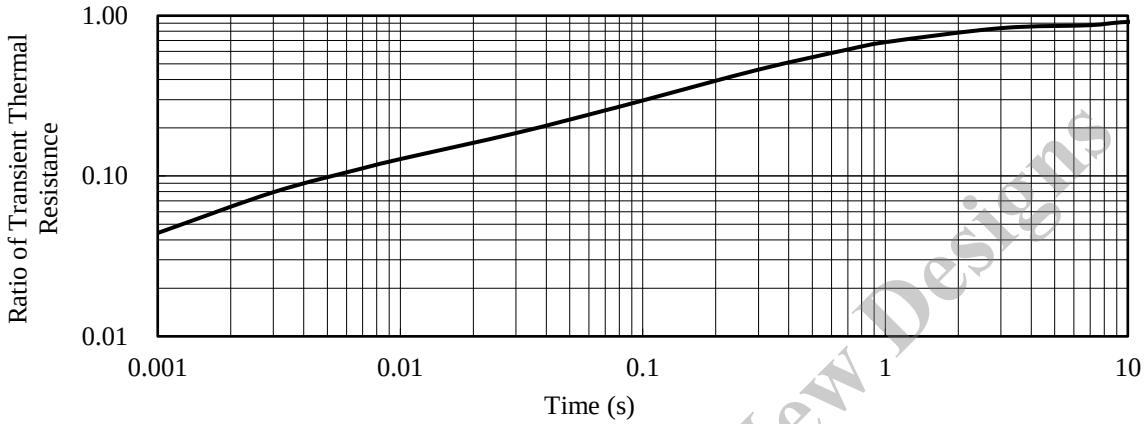


Figure 14-1. Transient Thermal Resistance: SX68001MH

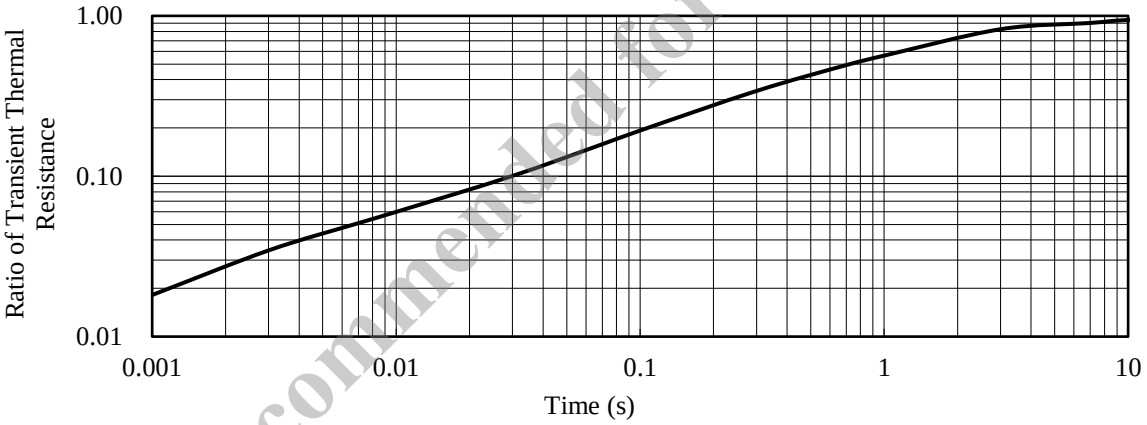


Figure 14-2. Transient Thermal Resistance: SX68003MH

14.2 Performance Curves of Control Parts

Figure 14-3 to Figure 14-27 provide performance curves of the control parts integrated in the SX68000MH series, including variety-dependent characteristics and thermal characteristics. T_J represents the junction temperature of the control parts.

Table 14-1. Typical Characteristics of Control Parts

Figure Number	Figure Caption
Figure 14-3	Logic Supply Current, I_{CC} vs. T_C (INx = 0 V)
Figure 14-4	Logic Supply Current, I_{CC} vs. T_C (INx = 5 V)
Figure 14-5	Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}
Figure 14-6	Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C
Figure 14-7	Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C
Figure 14-8	VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)
Figure 14-9	Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C
Figure 14-10	Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C
Figure 14-11	Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C
Figure 14-12	Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C
Figure 14-13	UVLO_VB Filtering Time vs. T_C
Figure 14-14	UVLO_VCC Filtering Time vs. T_C
Figure 14-15	High Level Input Signal Threshold Voltage, V_{IH} vs. T_C
Figure 14-16	Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C
Figure 14-17	Input Current at High Level (HINx or LINx), I_{IN} vs. T_C
Figure 14-18	High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)
Figure 14-19	Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)
Figure 14-20	Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C
Figure 14-21	Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C
Figure 14-22	SD Pin Filtering Time vs. T_C
Figure 14-23	FO Pin Filtering Time vs. T_C
Figure 14-24	Current Limit Reference Voltage, V_{LIM} vs. T_C
Figure 14-25	OCP Threshold Voltage, V_{TRIP} vs. T_C
Figure 14-26	OCP Hold Time, t_P vs. T_C
Figure 14-27	OCP Blanking Time, $t_{BK(OCP)}$ vs. T_C; Current Limit Blanking Time, $t_{BK(OCL)}$ vs. T_C
Figure 14-28	REG Pin Voltage, V_{REG} vs. T_C

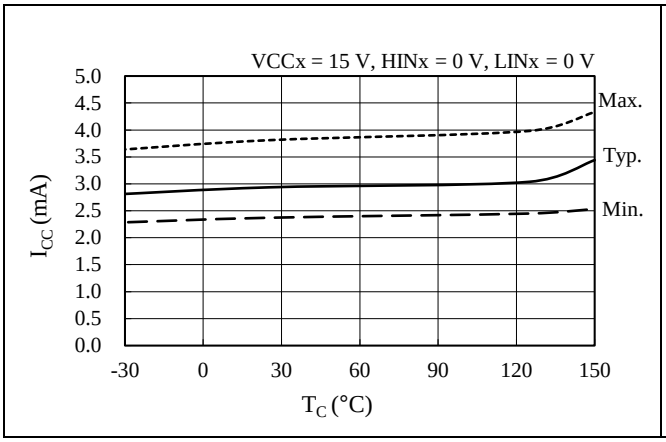


Figure 14-3. Logic Supply Current, I_{CC} vs. T_C (INx = 0 V)

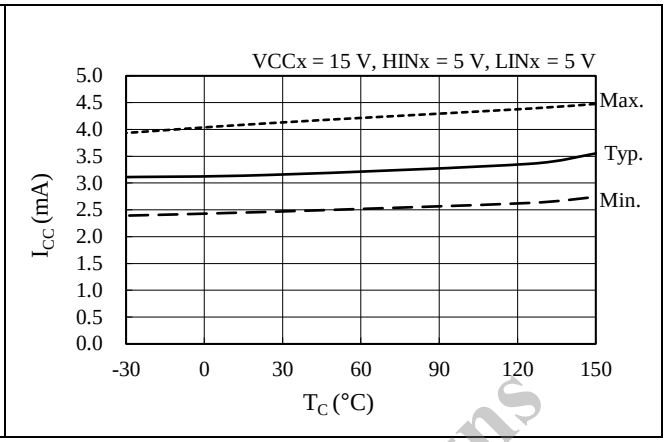


Figure 14-4. Logic Supply Current, I_{CC} vs. T_C (INx = 5 V)

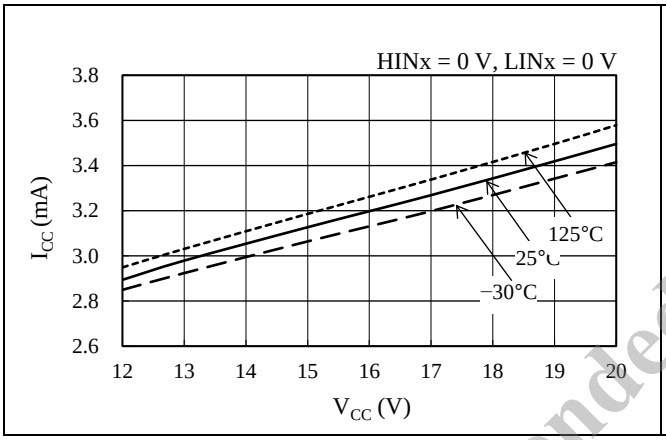


Figure 14-5. Logic Supply Current, I_{CC} vs. VCCx Pin Voltage, V_{CC}

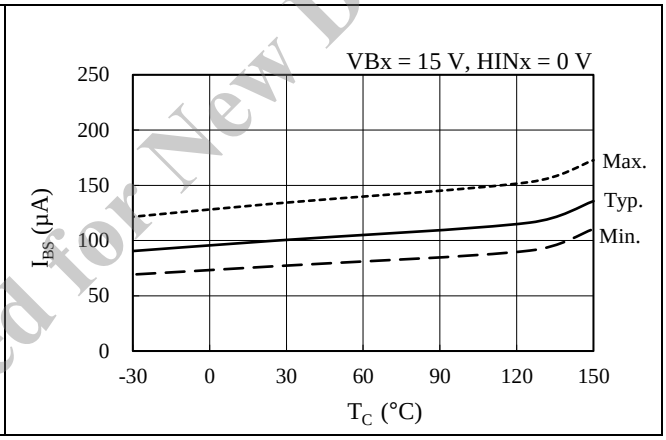


Figure 14-6. Logic Supply Current in 1-phase Operation (HINx = 0 V), I_{BS} vs. T_C

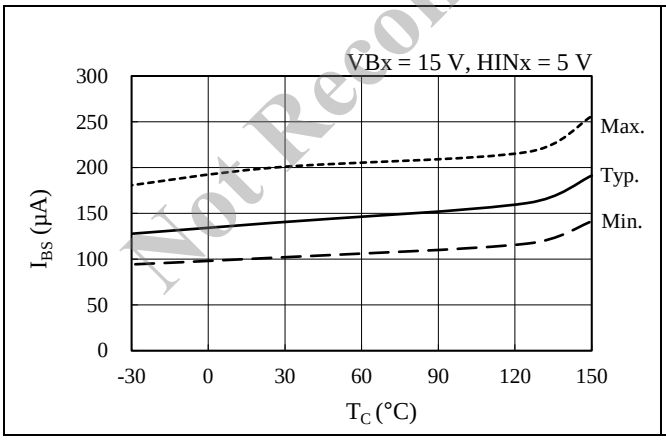


Figure 14-7. Logic Supply Current in 1-phase Operation (HINx = 5 V), I_{BS} vs. T_C

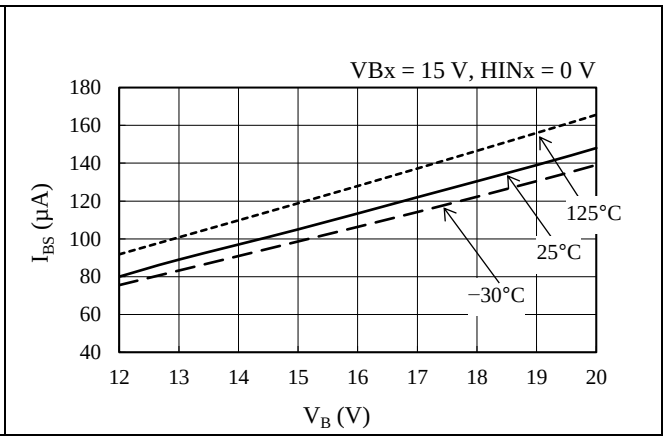


Figure 14-8. VBx Pin Voltage, V_B vs. Logic Supply Current, I_{BS} (HINx = 0 V)

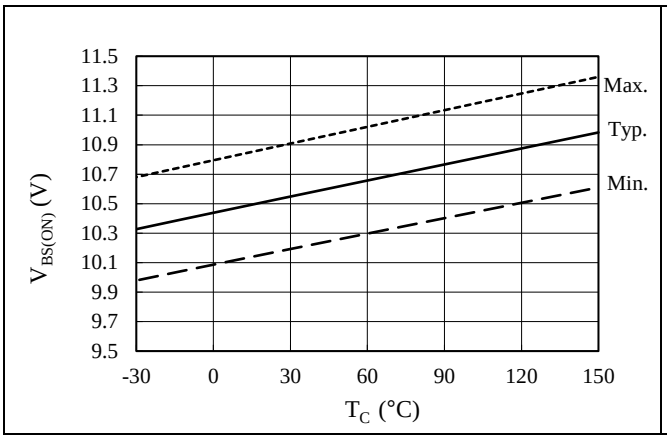


Figure 14-9. Logic Operation Start Voltage, $V_{BS(ON)}$ vs. T_C

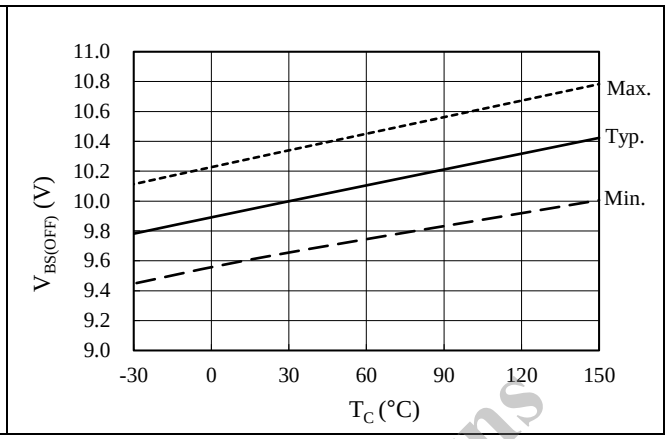


Figure 14-10. Logic Operation Stop Voltage, $V_{BS(OFF)}$ vs. T_C

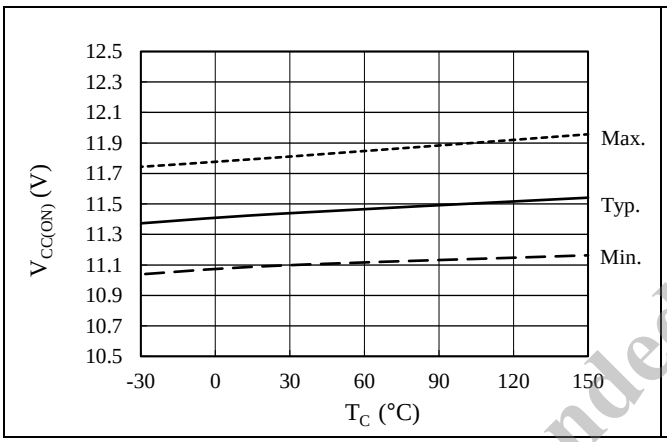


Figure 14-11. Logic Operation Start Voltage, $V_{CC(ON)}$ vs. T_C

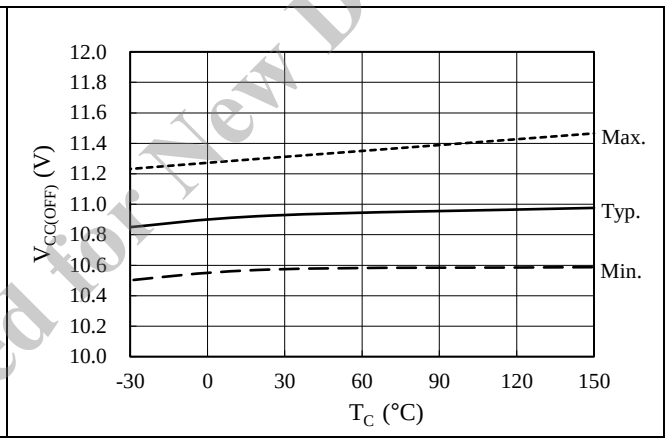


Figure 14-12. Logic Operation Stop Voltage, $V_{CC(OFF)}$ vs. T_C

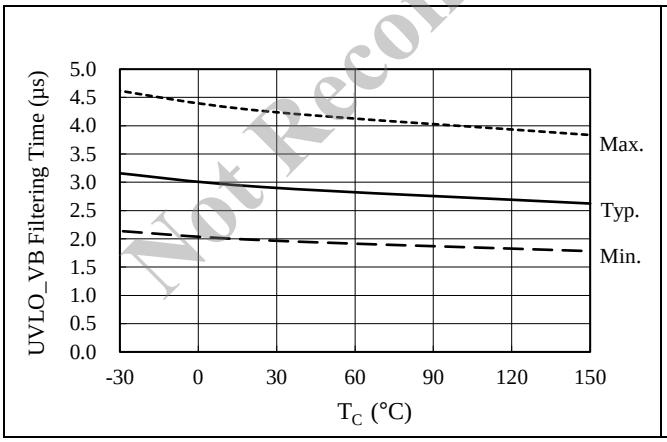


Figure 14-13. UVLO_VB Filtering Time vs. T_C

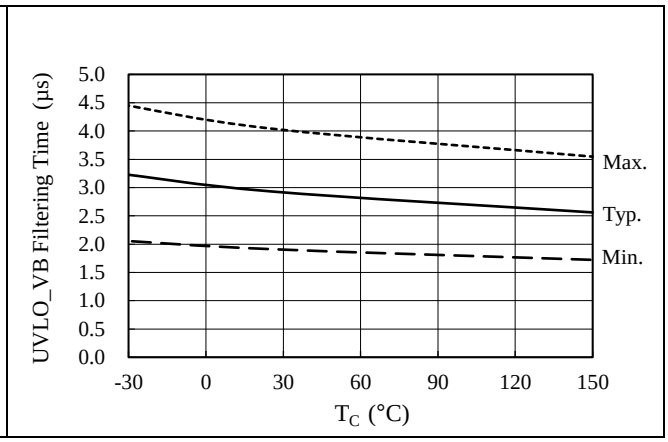


Figure 14-14. UVLO_VCC Filtering Time vs. T_C

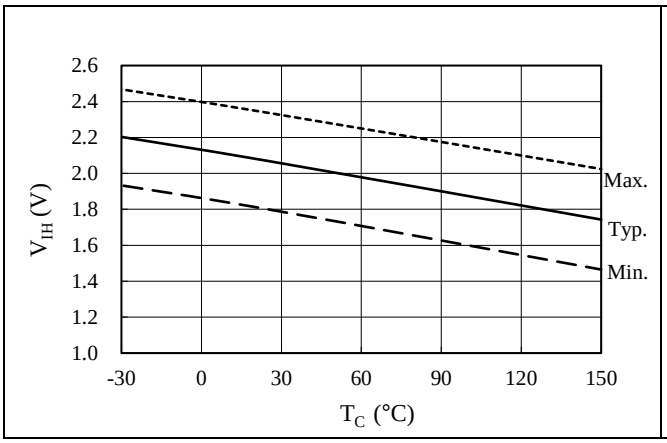


Figure 14-15. High Level Input Signal Threshold Voltage, V_{IH} vs. T_C

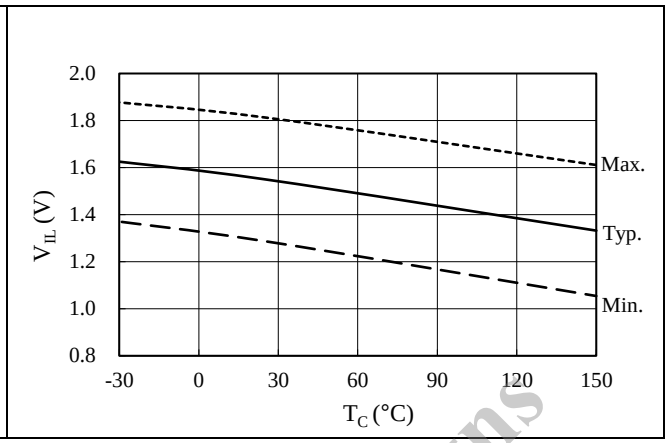


Figure 14-16. Low Level Input Signal Threshold Voltage, V_{IL} vs. T_C

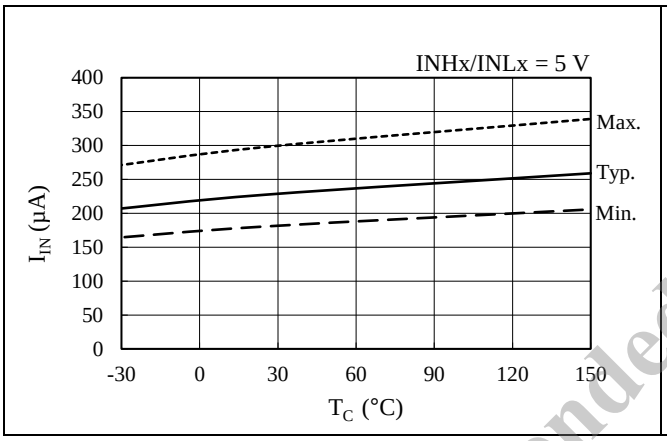


Figure 14-17. Input Current at High Level (HINx or LINx), I_{IN} vs. T_C

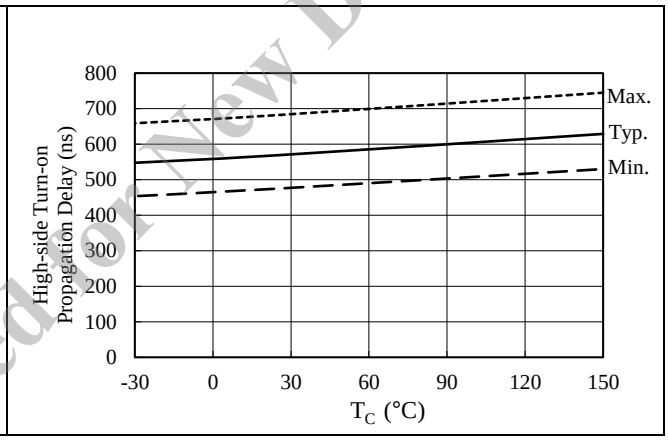


Figure 14-18. High-side Turn-on Propagation Delay vs. T_C (from HINx to HOx)

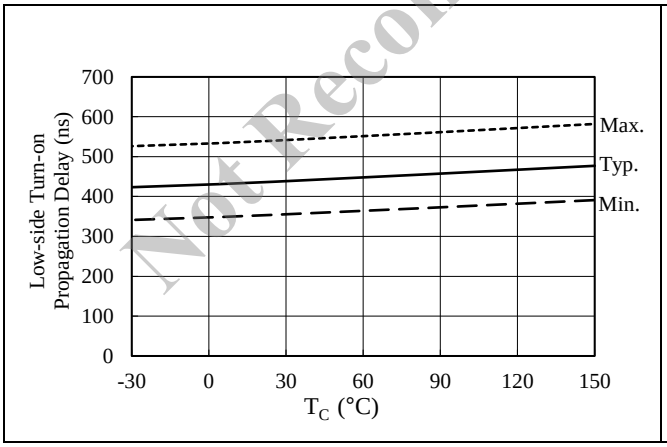


Figure 14-19. Low-side Turn-on Propagation Delay vs. T_C (from LINx to LOx)

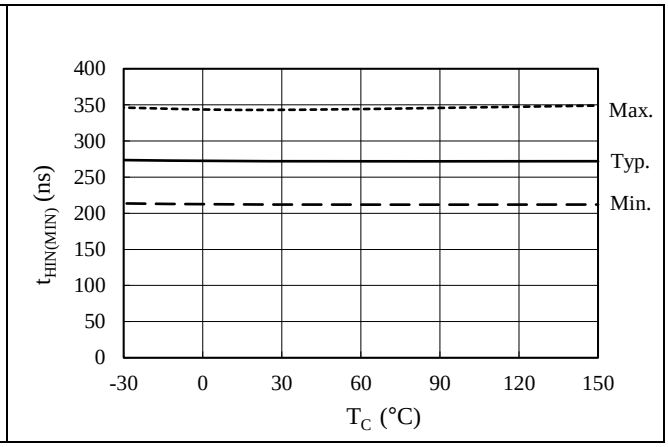


Figure 14-20. Minimum Transmittable Pulse Width for High-side Switching, $t_{HIN(MIN)}$ vs. T_C

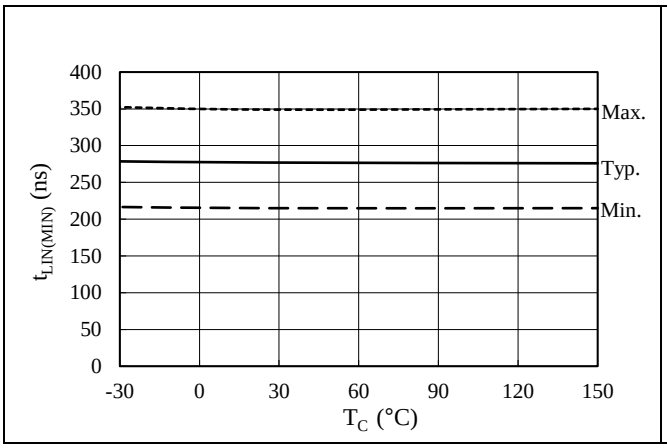


Figure 14-21. Minimum Transmittable Pulse Width for Low-side Switching, $t_{LIN(MIN)}$ vs. T_C

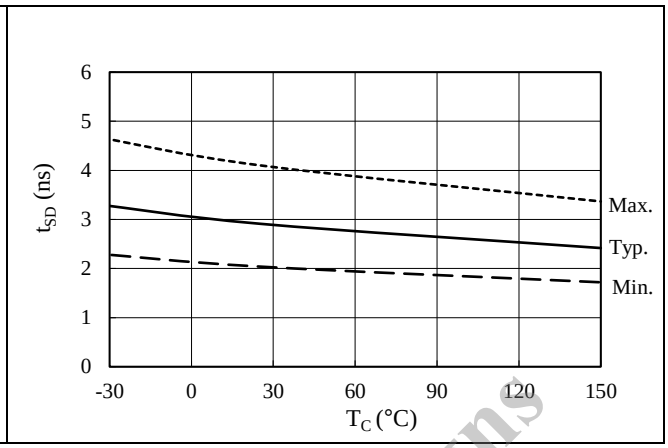


Figure 14-22. SD Pin Filtering Time vs. T_C

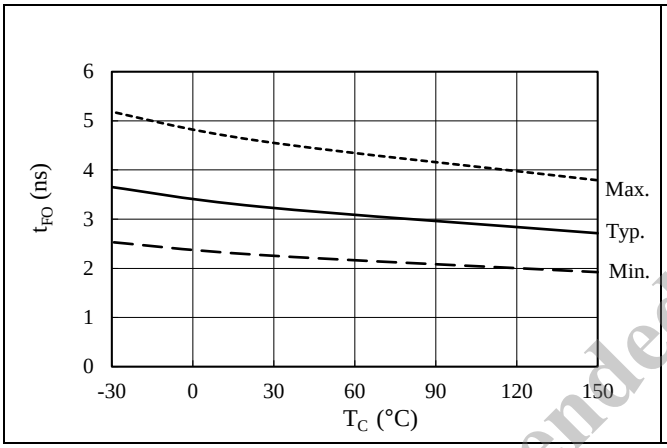


Figure 14-23. FO Pin Filtering Time vs. T_C

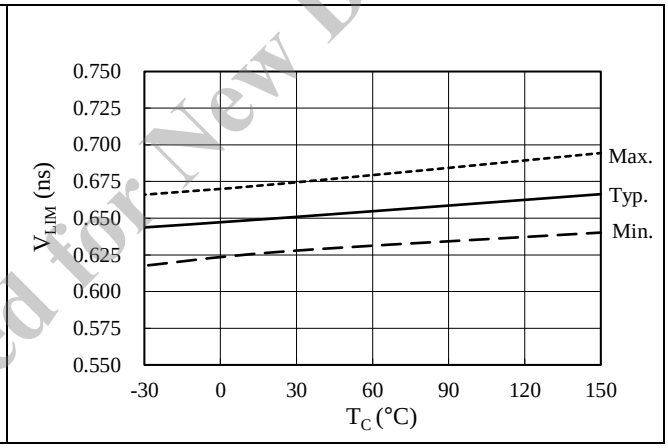


Figure 14-24. Current Limit Reference Voltage, V_{LIM} vs. T_C

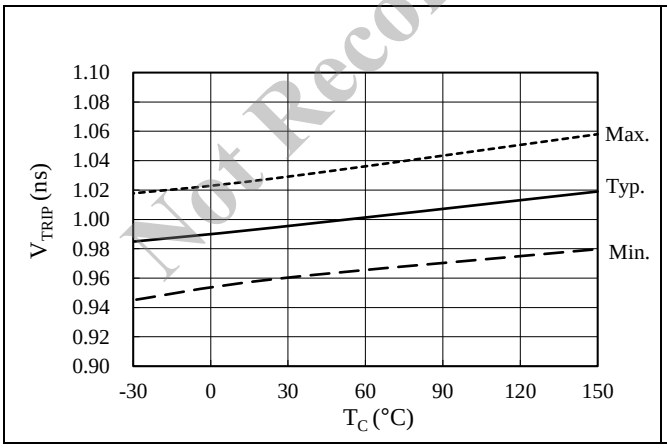


Figure 14-25. OCP Threshold Voltage, V_{TRIP} vs. T_C

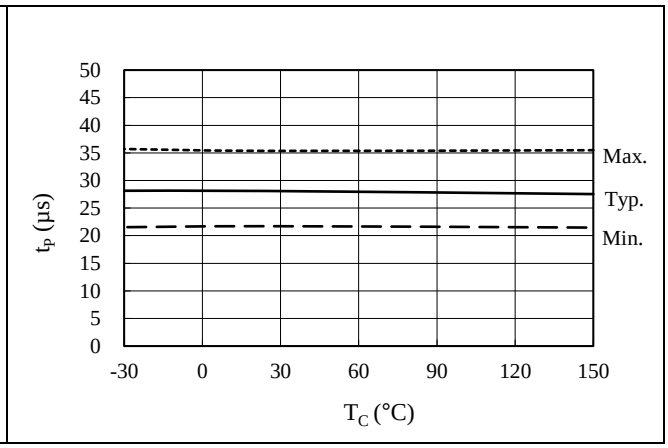


Figure 14-26. OCP Hold Time, t_P vs. T_C

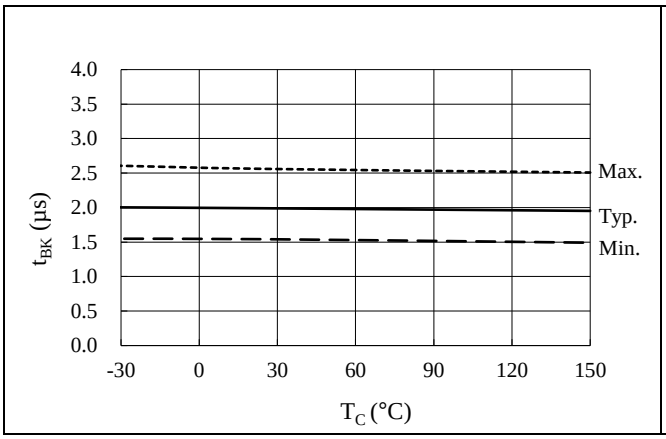


Figure 14-27. OCP Blanking Time, $t_{BK(OCP)}$ vs. T_C; Current Limit Blanking Time, $t_{BK(OCL)}$ vs. T_C

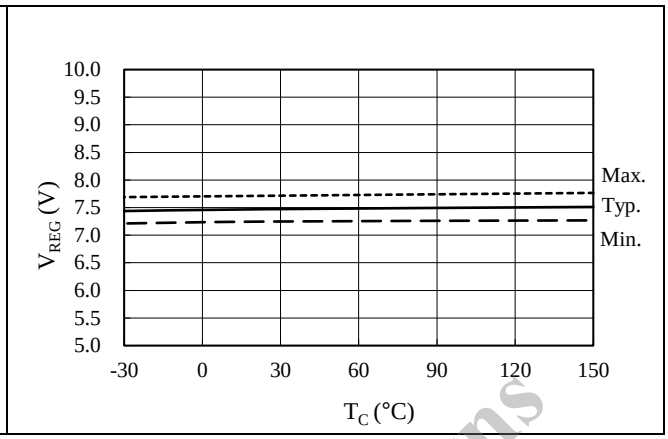


Figure 14-28. REG Pin Voltage, V_{REG} vs. T_C

14.3 Performance Curves of Output Parts

14.3.1 Output Transistor Performance Curves

14.3.1.1. SX68001MH

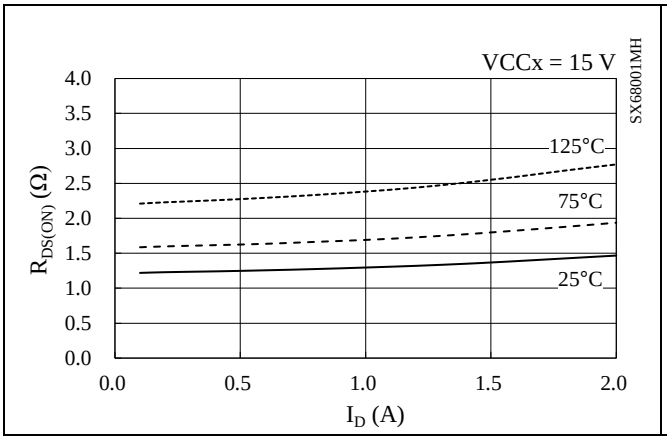


Figure 14-29. Power MOSFET $R_{DS(ON)}$ vs. I_D

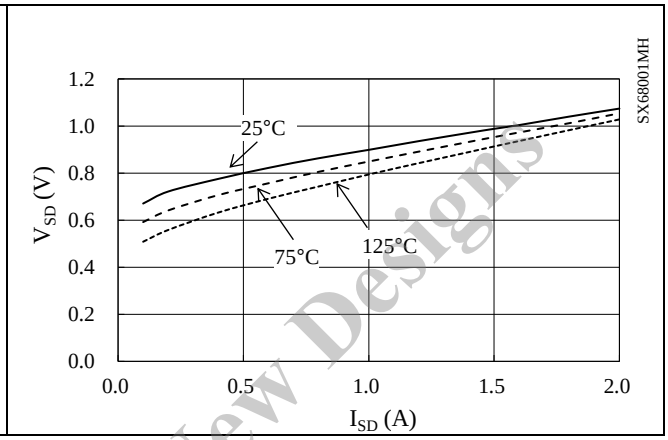


Figure 14-30. Power MOSFET V_{SD} vs. I_{SD}

14.3.1.2. SX68003MH

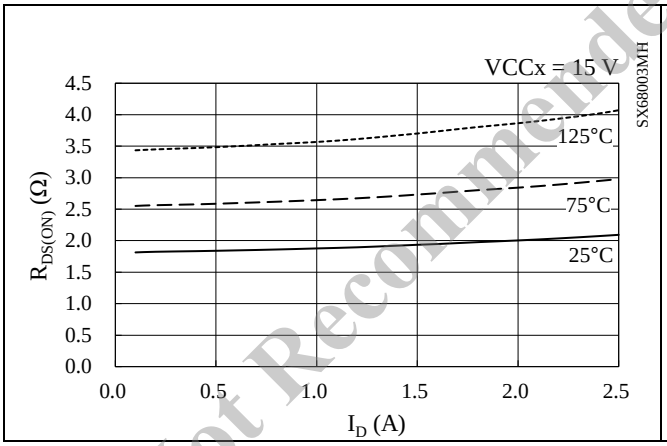


Figure 14-31. Power MOSFET $R_{DS(ON)}$ vs. I_D

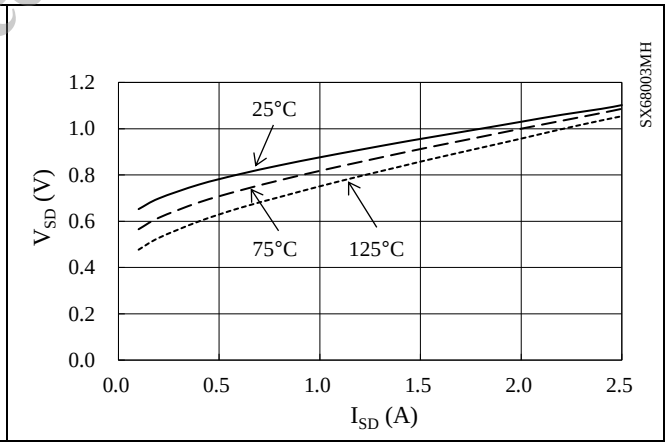


Figure 14-32. Power MOSFET V_{SD} vs. I_{SD}

14.3.2 Switching Loss Curves

Switching Loss, E, is the sum of turn-on loss and turn-off loss.

14.3.2.1. SX68001MH

Conditions: VBBx pin voltage = 150 V, half-bridge circuit with inductive load.

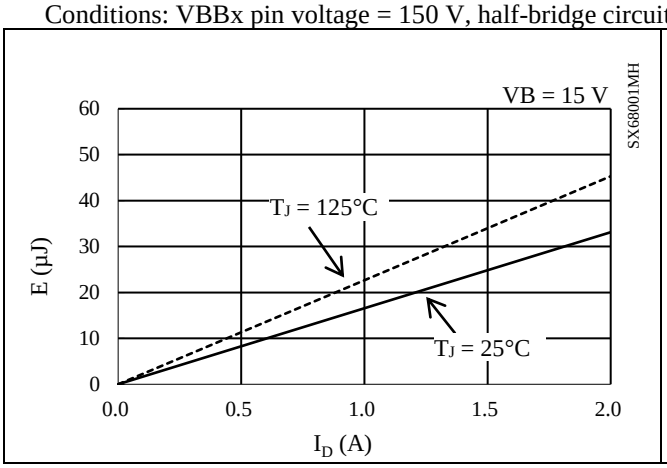


Figure 14-33. High-side Switching Loss

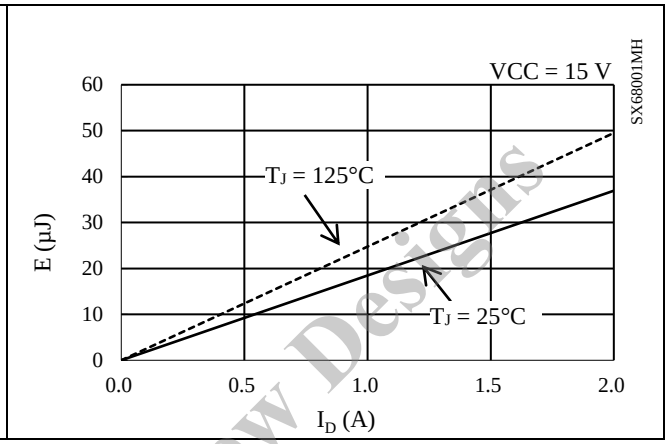


Figure 14-34. Low-side Switching Loss

14.3.2.2. SX68003MH

Conditions: VBBx pin voltage = 300 V, half-bridge circuit with inductive load.

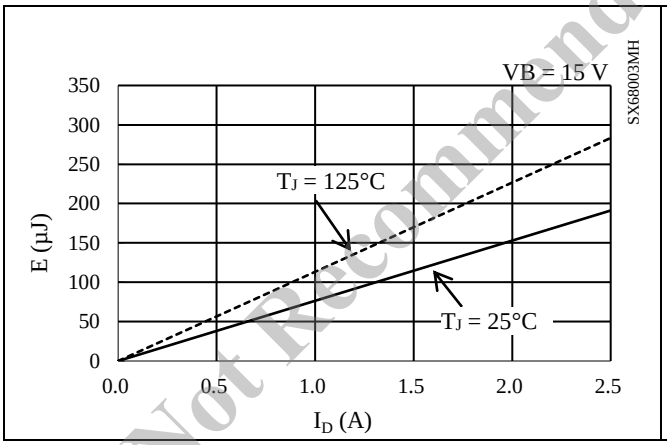


Figure 14-35. High-side Switching Loss

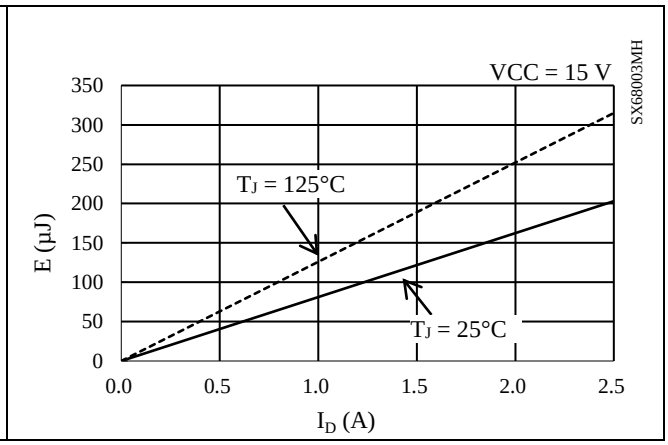


Figure 14-36. Low-side Switching Loss

14.4 Allowable Effective Current Curves

The following curves represent allowable effective currents in 3-phase sine-wave PWM driving with parameters such as typical $R_{DS(ON)}$ or $V_{CE(SAT)}$, and typical switching losses.

14.4.1 SX68001MH

Operating conditions: VBBx pin input voltage, V_{DC} = 150 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

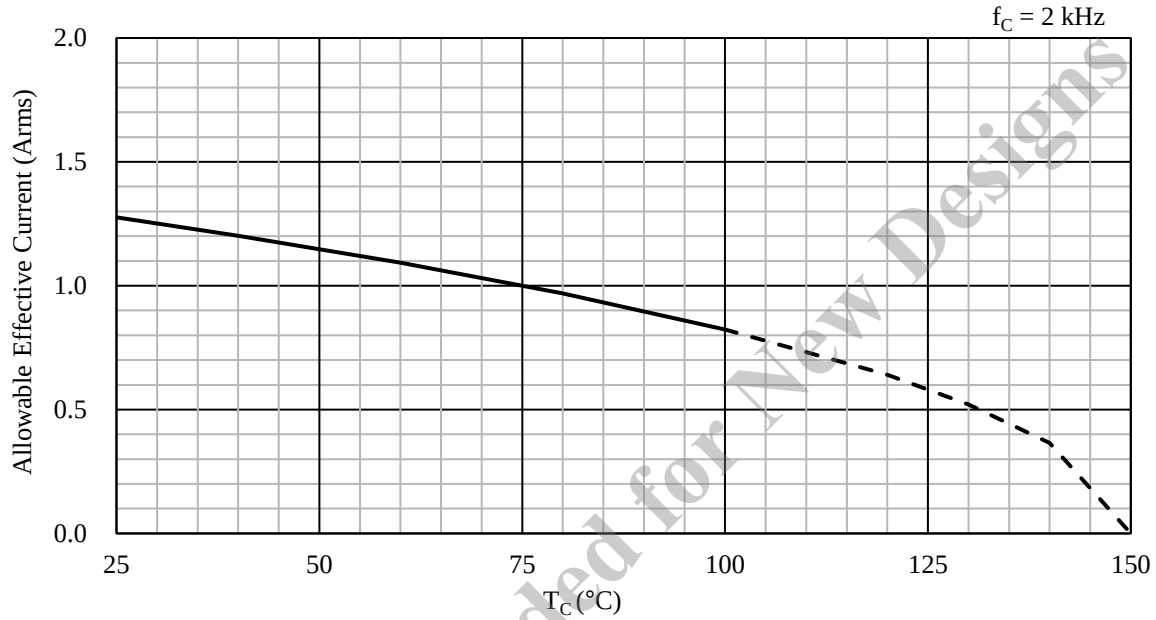


Figure 14-37. Allowable Effective Current (f_C = 2 kHz): SX68001MH

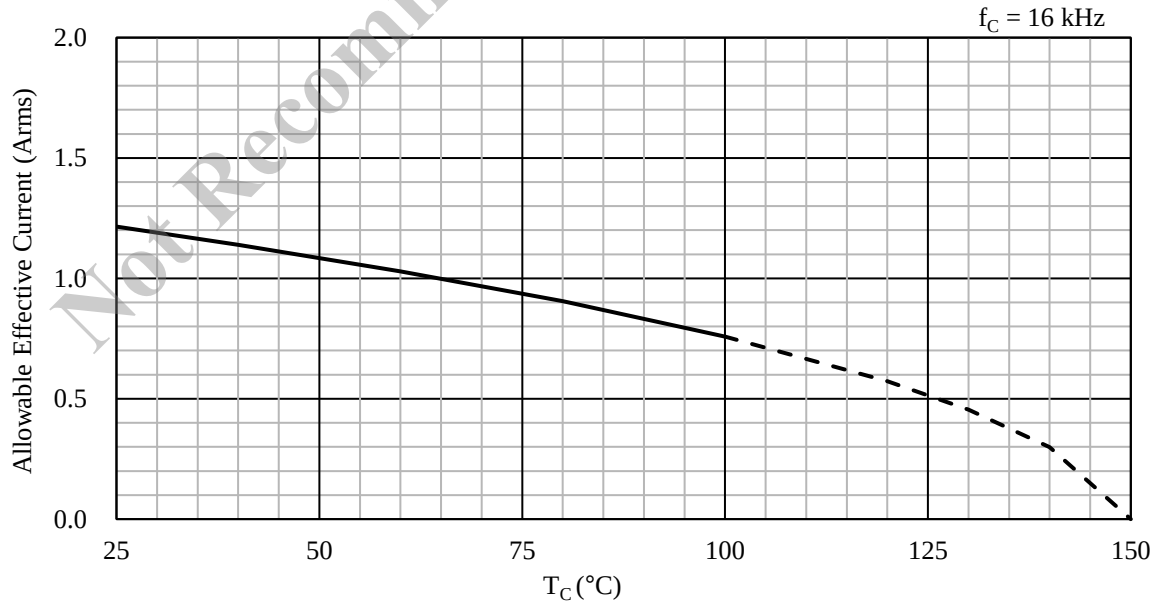


Figure 14-38. Allowable Effective Current (f_C = 16 kHz): SX68001MH

14.4.2 SX68003MH

Operating conditions: VBBx pin input voltage, V_{DC} = 300 V; VCCx pin input voltage, V_{CC} = 15 V; modulation index, M = 0.9; motor power factor, cosθ = 0.8; junction temperature, T_J = 150 °C.

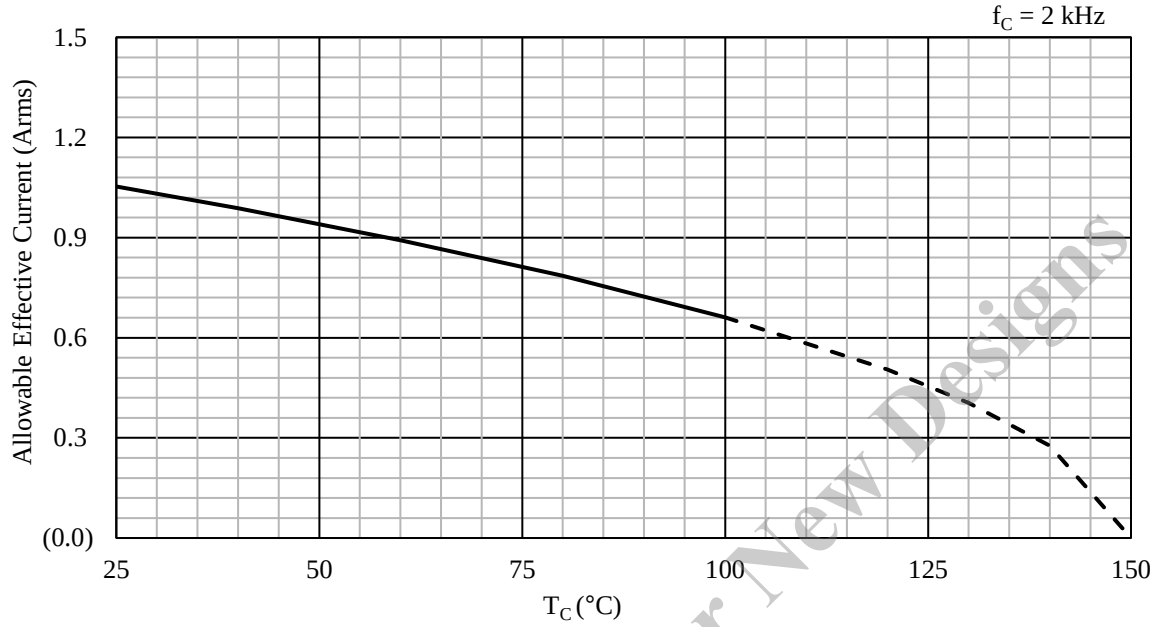


Figure 14-39. Allowable Effective Current (f_C = 2 kHz): SX68003MH

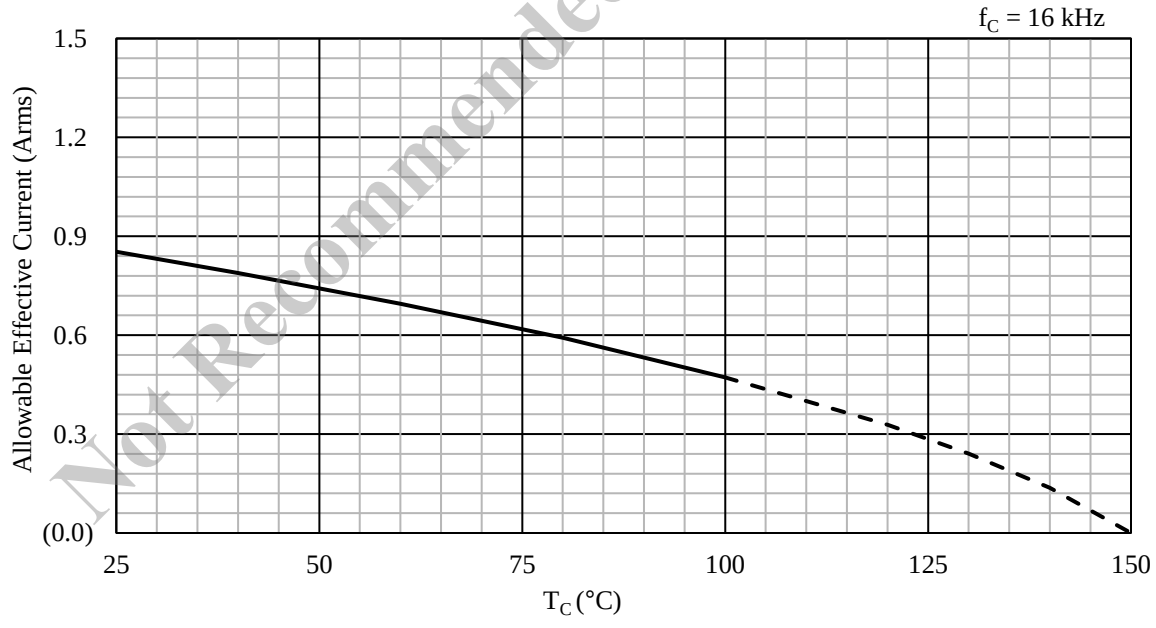


Figure 14-40. Allowable Effective Current (f_C = 16 kHz): SX68003MH

15. Pattern Layout Example

This section contains the schematic diagrams of a PCB pattern layout example using an SX68000MH series device. For details on the land pattern example of the IC, see Section 9.

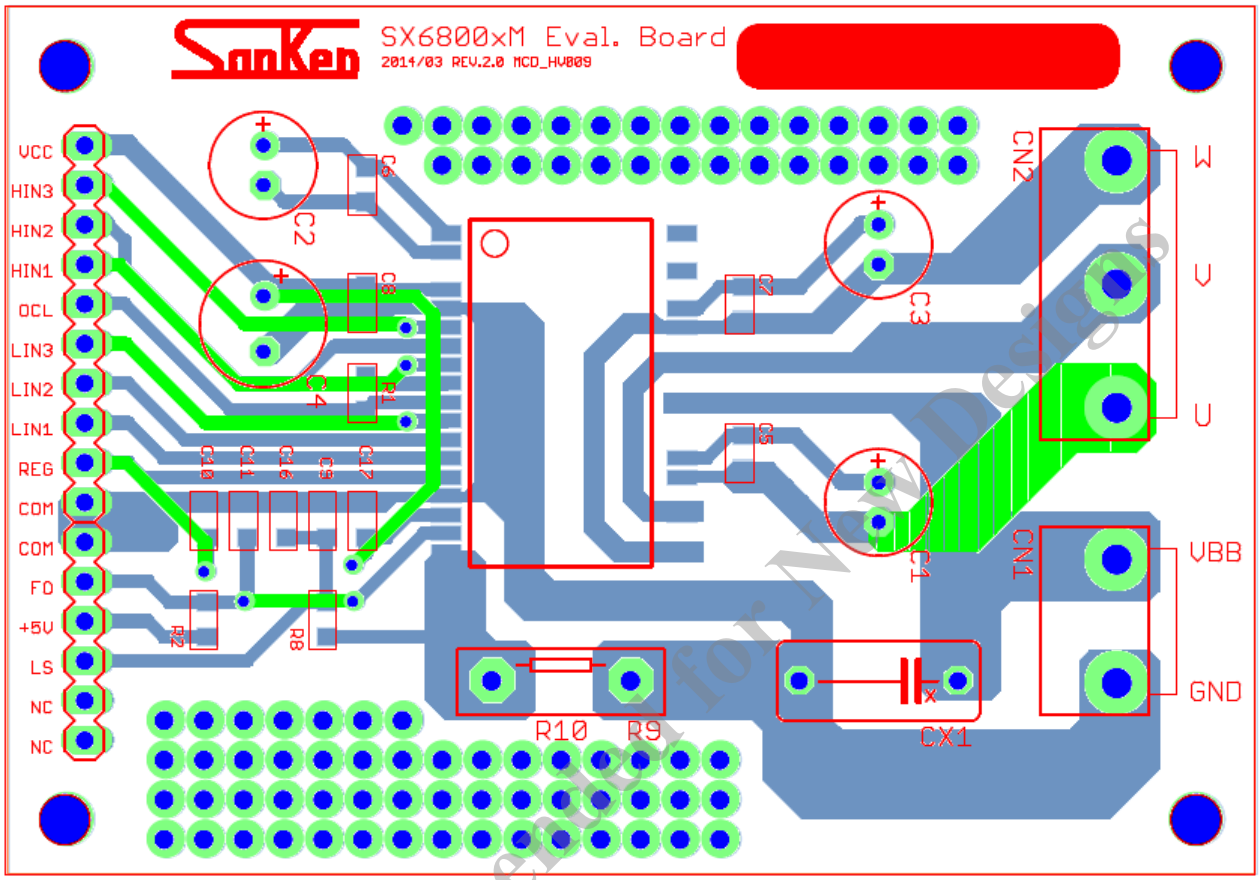


Figure 15-1. Pattern Layout Example (Two-layer Board)

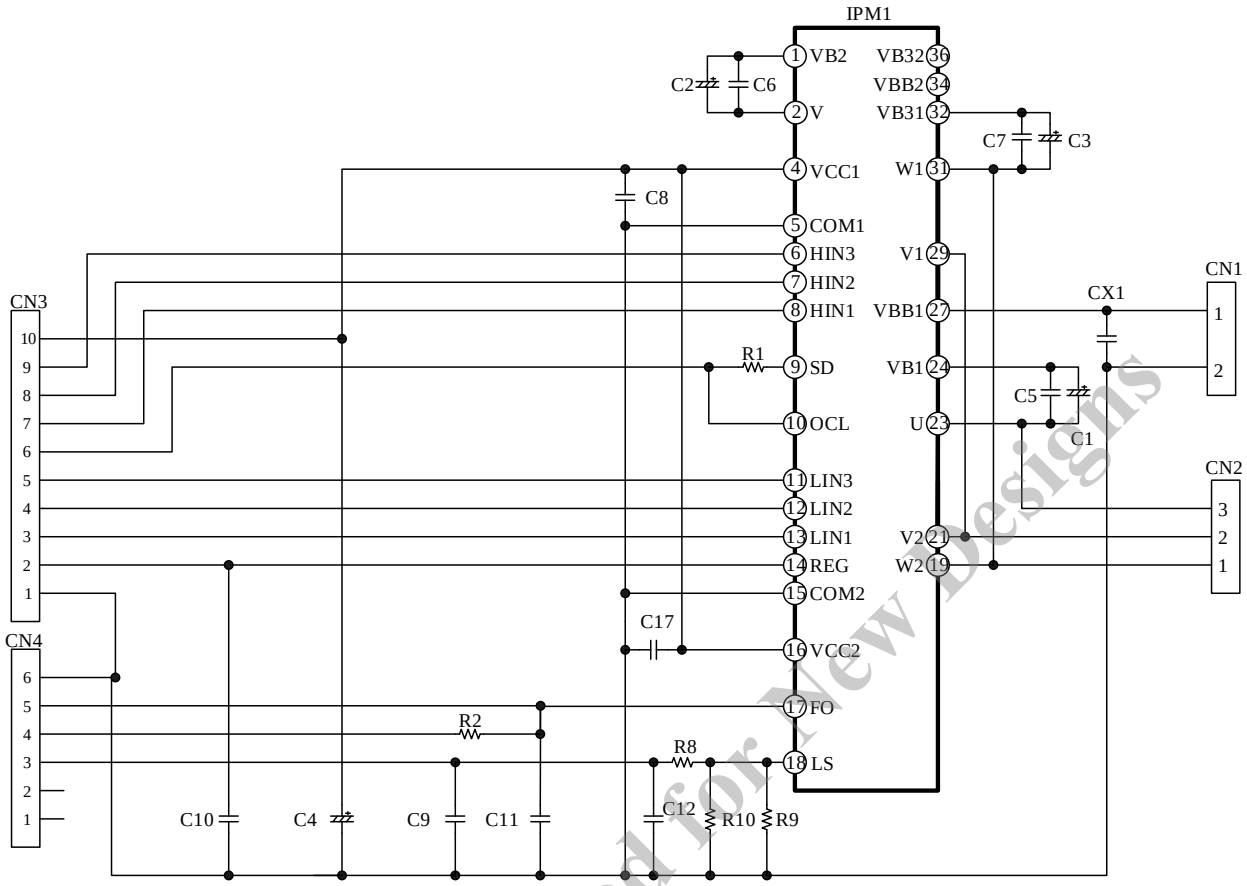


Figure 15-2. Circuit Diagram of PCB Pattern Layout Example

16. Typical Motor Driver Application

This section contains the information on the typical motor driver application listed in the previous section, including a circuit diagram, specifications, and the bill of the materials used.

- **Motor Driver Specifications**

IC	SX68003MH
Main Supply Voltage, V_{DC}	300 VDC (typ.)
Rated Output Power	50 W

- **Circuit Diagram**

See Figure 15-2.

- **Bill of Materials**

Symbol	Part Type	Ratings	Symbol	Part Type	Ratings
C1	Electrolytic	22 µF, 35 V	CX1	Film	0.01 µF, 630 V
C2	Electrolytic	22 µF, 35 V	R1	General	0 Ω, 1/8 W
C3	Electrolytic	22 µF, 35 V	R2	General	4.7 kΩ, 1/8 W
C4	Electrolytic	47 µF, 35 V	R8*	Metal plate	10 kΩ, 1/8 W
C5	Ceramic	0.1 µF, 50 V	R9*	Metal plate	1 Ω, 2 W
C6	Ceramic	0.1 µF, 50 V	R10*	General	Open
C7	Ceramic	0.1 µF, 50 V	IPM1	IC	SX68003MH
C8	Ceramic	0.1 µF, 50 V	CN1	Pin header	Equiv. to B2P3-VH
C9	Ceramic	0.1 µF, 50 V	CN2	Pin header	Equiv. to B2P5-VH
C10	Ceramic	0.1 µF, 50 V	CN3	Connector	Equiv. to MA10-1
C11	Ceramic	0.1 µF, 50 V	CN4	Connector	Equiv. to MA06-1
C16	Ceramic	100 pF, 50 V			
C17	Ceramic	0.1 µF, 50 V			

* Refers to a part that requires adjustment based on operation performance in an actual application.

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