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High Temperature (230 °C) Wirebondable Thin Film Chip Resistors and Resistor Networks



LINKS TO ADDITIONAL RESOURCES



INTRODUCTION

For applications such as down hole applications, the need for parts able to withstand very severe conditions (temperature as high as 215 °C powered or up to 230 °C un-powered) has leaded Vishay Sfernice to push out the limit of the thin film technology.

Designers might read the application note "Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (P, PRA, etc...) (High Temperature Application)" www.vishay.com/doc?53047 in conjunction with this datasheet to help them to properly design their PCBs and get the best performances of the RMKHT.

Vishay Sfernice research and development engineers will be willing to support any customer design considerations.

FEATURES

- Operating temperature range: -55 °C; +215 °C
- Storage temperature: -55 °C; +230 °C
- Wirebondable (aluminum pads)
- Aluminum pads
- Large selection of sizes available
- · Custom networks available on request (CNHT)
- Temperature coefficient down to ± 15 ppm/°C (-55 °C; +215 °C)
- Tolerance down to ± 0.05 %
- Temperature coefficient remains at ± 15 ppm/°C after long term storage at 230 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL PERFORMANCE

	ABS	TRACKING (1)
TCR	± 25 ppm/°C	2 ppm/°C
	ABS	RATIO (1)
TOL.	± 0.05 %	0.02 %

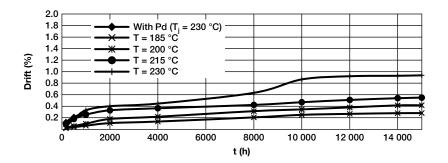
Note

(1) When applicable (networks only)

MECHANICAL SPECIFICATIONS				
Resistive element	Nichrome (NiCr)			
Substrate material	Silicon (size 22, 33, 55, 515) - alumina (other sizes)			
Bonding pads	Aluminum (AI)			
Passivation	Silicon nitride (Si ₃ N ₄)			
Back metallization (1)	Gold (thickness = 0.5 μm typical) on nickel barrier (1 μm typical)			

Note

(1) When applicable (only on alumina substrate)



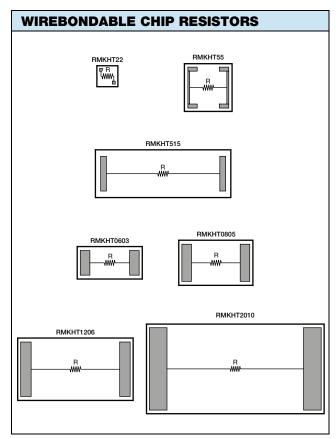
Note

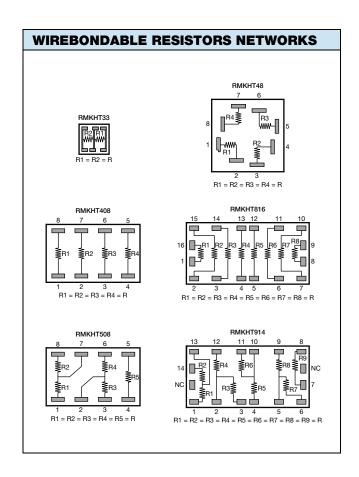
 $\bullet~$ TCR (-55 °C; +215 °C) remains unchanged after 15 000 h storage

Revision: 20-May-2022 **1** Document Number: 60075 For technical questions, contact: sferthinfilm@vishay.com

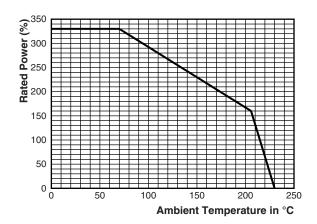


SCHEMATIC



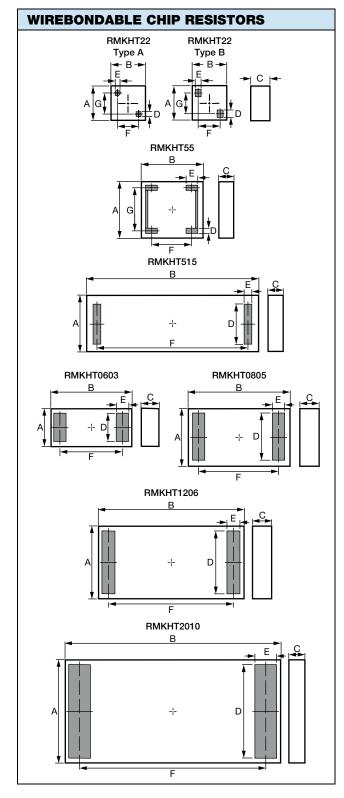


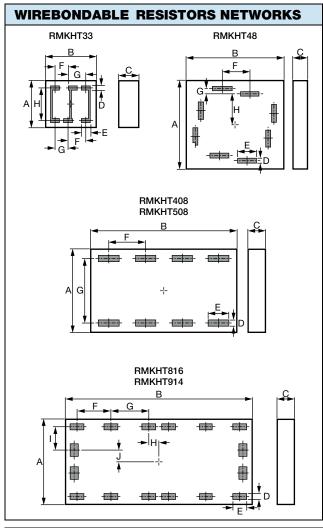
POWER DERATING CURVE





PATTERN





DIMENSIONS in millimeters								
SERIES	A ± 0.05	B ± 0.05	C max.	D	E	F	G	
RMKHT22 Type A	0.58	0.58	0.4	0.08	0.08	0.354	0.354	
RMKHT22 Type B	0.58	0.58	0.4	0.125	0.1	0.374	0.349	
RMKHT55	1.32	1.32	0.4	0.11	0.26	0.87	1.02	
RMKHT515	1.32	3.75	0.4	0.96	0.16	3.3		
RMKHT0603	0.9	1.8	0.45	0.68	0.265	1.365		
RMKHT0805	1.25	2.05	0.45	1.03	0.265	1.615		
RMKHT1206	1.725	3.2	0.45	1.505	0.29	2.74		
RMKHT2010	2.64	5.23	0.45	2.42	0.518	4.54		

DIMENSIONS in millimeters										
SERIES	A ± 0.05	B ± 0.05	C max.	D	E	F	G	Н	ı	L
RMKHT33	0.83	0.83	0.4	0.08	0.16	0.3	0.22	0.6		
RMKHT48	2	2	0.4	0.1	0.39	0.57	0.12	0.69		
RMKHT408 RMKHT508	16	2.6	0.4	0.11	0.36	0.65	1.25			
RMKHT816 RMKHT914	17	3.4	0.4.	0.13	0.25	0.62	0.69	0.175	0.47	0.225



STANDARD ELECTRICAL SPECIFICATIONS - Bare Resistors Chips							
MODEL	SIZE	RESISTANCE RANGE ⁽¹⁾ Ω	TCR ⁽²⁾ -55 °C; +215 °C ± ppm/°C	TOLERANCE ± %	POWER RATING ⁽³⁾ P _{70°C} W	POWER RATING ⁽³⁾ P _{215 °C} W	
RMKHT22	0202	10 to 500K	15, 30	0.05, 0.1, 0.5, 1	0.05	0.005	
RMKHT55	0505	150 to 2M	15, 30	0.05, 0.1, 0.5, 1	0.25	0.025	
RMKHT515	0515	100 to 5M	15, 30	0.05, 0.1, 0.5, 1	0.5	0.05	
RMKHT0603	0603	10 to 320K	15, 30	0.05, 0.1, 0.5, 1	0.125	0.0375	
RMKHT0805	0805	10 to 720K	15, 30	0.05, 0.1, 0.5, 1	0.2	0.06	
RMKHT1206	1206	10 to 2.7M	15, 30	0.05, 0.1, 0.5, 1	0.33	0.1	
RMKHT2010	2010	10 to 7.5M	15, 30	0.05, 0.1, 0.5, 1	1	0.2 (5)	

PERFORMANCES - Bare Resistors Chips						
TEST SPECIFICATIONS CONDITIONS						
Limiting voltage	From 75 V to 300 V (depending on size) (4)					
Operating temperature range	-55 °C; +215 °C					
Max. temperature resistive element	220 °C					
Max. substrate temperature	230 °C					
Load life stability	± 0.35 %	2000 h / 220 °C (ambient) at Pn				
Storage temperature range	-55 °C; +230 °C					
Shelf life stability	± 0.6 % typ. (± 0.8 % max.)	15 000 h / 230 °C				

STANDA	STANDARD ELECTRICAL SPECIFICATIONS - Bare Resistors Networks									
MODEL	SIZE	RESISTANCE RANGE (1) Ω	ABSOLUTE TOLERANCE ± %	RATIO TOLERANCE ± %	ABSOLUTE TCR ⁽²⁾ -55 °C; +215 °C ± ppm/°C	RATIO TCR -55 °C; +215 °C ± ppm/°C	POWER RATING ⁽³⁾ P _{70°C} W PER RESISTOR	POWER RATING ⁽³⁾ P ₂₁₅ °C W PER RESISTOR		
RMKHT33	0303	100 to 500K	0.05, 0.1, 0.5, 1	0.02, 0.05, 0.5, 0.1	15, 30	2, 5	0.10	0.010		
RMKHT48	0808	100 to 800K	0.05, 0.1, 0.5, 1	0.02, 0.05, 0.5, 0.1	15, 30	2, 5	0.10	0.010		
RMKHT408	0610	100 to 400K	0.05, 0.1, 0.5, 1	0.02, 0.05, 0.5, 0.1	15, 30	2, 5	0.10	0.010		
RMKHT508	0610	500 to 400K	0.05, 0.1, 0.5, 1	0.02, 0.05, 0.5, 0.1	15, 30	2, 5	0.10	0.010		
RMKHT816	0714	100 to 400K	0.05, 0.1, 0.5, 1	0.02, 0.05, 0.5, 0.1	15, 30	2, 5	0.10	0.010		
RMKHT914	0714	500 to 200K	0.05, 0.1, 0.5, 1	0.02, 0.05, 0.5, 0.1	15, 30	2, 5	0.10	0.010		

PERFORMANCES - Bare Resistors Networks						
TEST	SPECIFICATIONS	CONDITIONS				
Limiting voltage	100 V on each resistor (except RMKHT33 50 V on each resistor)					
Operating temperature range	-55 °C; +215 °C					
Max. temperature resistive element	220 °C					
Max. substrate temperature	230 °C					
Load life stability	± 0.35 %	2000 h / 220 °C (ambient) at Pn				
Load life stability on ratio	± 0.35 %	2000 h / 220 °C (ambient) at Pn				
Storage temperature range	-55 °C; +230 °C					
Shelf life stability	± 0.6 % typ. (± 0.8 % max.)	15 000 h/230 °C				

Bare Resistors Chips

V	± 10 ppm/°C	-55 °C; +155 °C
T T	± 15 ppm/°C	-55 °C; +215 °C
E	± 25 ppm/°C	-55 °C; +155 °C
	± 30 ppm/°C	-55 °C; +215 °C

Bare Resistors Networks

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V	± 10 ppm/°C abs.	1 ppm/°C tracking	-55 °C; +155 °C
1	± 15 ppm/°C abs.	2 ppm/°C tracking	-55 °C; +215 °C
-	± 25 ppm/°C abs.	2 ppm/°C tracking	-55 °C; +155 °C
-	± 30 ppm/°C abs.	5 ppm/°C tracking	-55 °C; +215 °C

⁽³⁾ Pn is intended with no back side metallized. For power handling improvement, please refer to application note 53047 "Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (High Temperature Applications)" www.vishay.com/doc?53047 and consult Vishay Sfernice.

Notes

(1) For ohmic range vs. tolerance and TCR see detailed table on next page.

⁽²⁾ Temperature Coefficient of Resistance

⁽⁴⁾ See Limiting Voltage table on next page.

⁽⁵⁾ It is possible to dissipate up to 0.3 W, but there will be an additional drift of 0.1 % after load life.



VALUE - Bare Resistors Chips

Baro resistore ompo						
		OHMIC F	RANGE (1)			
SERIES	СТ	T: Y	СТ	:E		
	MIN.	MAX.	MIN.	MAX.		
22	50 Ω	300 kΩ	10 Ω	500 kΩ		
55	1 kΩ	1.5 MΩ	150 Ω	2 ΜΩ		
515	1 kΩ	2 ΜΩ	100 Ω	5 ΜΩ		
0603	39 Ω	210 kΩ	10 Ω	320 kΩ		
0805	39 Ω	480 kΩ	10 Ω	720 kΩ		
1206	39 Ω	1.8 MΩ	10 Ω	2.7 MΩ		
2010	39 Ω	5 ΜΩ	10 Ω	7.5 MΩ		

BEST TOLERANCE AND TCR VS. OHMIC

VALUE - Bare Resistors Networks							
		OHMIC	RANGE				
SERIES	C.	T: Y	C1	[: E			
	MIN.	MAX.	MIN.	MAX.			
33	1 kΩ	250 kΩ	100 Ω	500 kΩ			
48	1 kΩ	200 kΩ	100 Ω	800 kΩ			
408	1 kΩ	200 kΩ	100 Ω	400 kΩ			
508	1 kΩ	200 kΩ	500 Ω	400 kΩ			
816	1 kΩ	200 kΩ	100 Ω	400 kΩ			
914	1 kΩ	100 kΩ	500 Ω	200 kΩ			

REST TOLERANCE AND TOR VS. OHMIC

Note

Best possible tolerance: 0.5 %: 10 Ω to < 20 Ω 0.1 %: 20 Ω to < 39 Ω

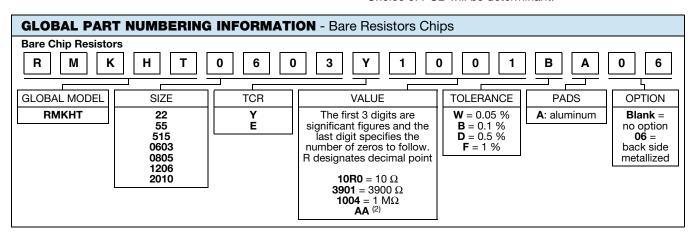
0.05 %: 39 Ω to max. ohmic value

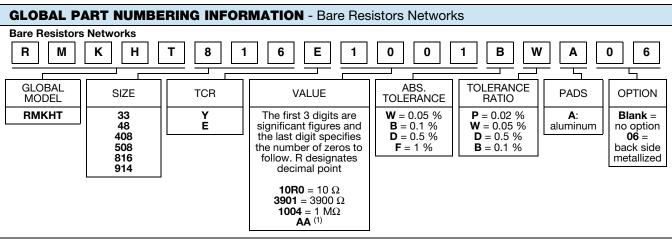
SIZE	LIMITING VOLTAGE in V			
22	100 V			
55	100 V			
515	100 V			
0603	75 V			
0805	150 V			
1206	200 V			
2010	300 V			

POPULAR OPTION

Back side metalized

Option to order: 06 (not available for sizes 22, 33, 55, 515) Please refer to Application Note 53047 "Power Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (High Temperature Applications) www.vishay.com/doc?53047 to evaluate performances improvement depending on process (brazing or gluing). Choice of PCB will be determinant.





Note

(1) For more than three significant digits an alphabetical code will be used (AA to ZZ) and a cross table will be provided





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GLOBAL PART NUMBERING INFORMATION - Bare Custom Networks						
Custom Networks						
C N H T 9 9 9 9						
	GLOBAL MODEL		REFERENCE]		
	CNHT		9999]		
		•		-		

Note

• A specific reference number is assigned by Vishay Sfernice



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