BLC10G15XS-301AVT

Power LDMOS transistor

AMPLEON

Rev. 1 — 26 June 2020 **Product data sheet**

1. Product profile

1.1 General description

350 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1452 MHz to 1492 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo circuit. V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 1.15 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(dBm)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1452 to 1492	30	47.5	18.2	50.5	–27.8 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

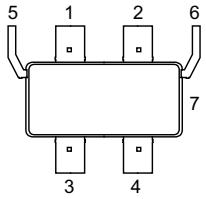
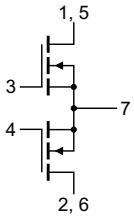
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1452 MHz to 1492 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC10G15XS-301AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+9	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+9	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+150	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 30 V; I_{Dq} = 300 mA (main); $V_{GS(amp)peak}$ = 1.3 V; T_{case} = 80 °C		
		P_L = 56.3 W	0.24	K/W
		P_L = 90 W	0.20	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.04 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 104 mA	1.6	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 400 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	20	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.64 A	-	10	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 3.64 A	-	126	211.9	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.17 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 217 mA	1.6	2.0	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 30 V; I_D = 950 mA	-	2.1	-	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	38	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.595 A	-	20	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 7.595 A	-	64	106.7	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 1454.5 MHz; f_2 = 1489.5 MHz; RF performance at V_{DS} = 30 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 1.15 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1452 MHz to 1492 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 56.3 W	16.2	18	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 56.3 W	-	−14	−9	dB
η_D	drain efficiency	$P_{L(AV)}$ = 56.3 W	44	49	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 56.3 W	-	−28	−23	dBc

Table 8. RF characteristics

Pulsed CW signal at a frequency of 1492 MHz; t_p = 100 µs; δ = 10 %; V_{DS} = 30 V; I_{Dq} = 400 mA (main); $V_{GS(amp)peak}$ = 1.2 V; T_{case} = 25 °C; in a Doherty production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		270	305	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC10G15XS-301AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V; f = 1452 MHz; P_L = 80 W (6 dB OBO); 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 300 mA (main); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1450	3.6 + j7.51	1.8 – j5.03	151	55.1	17.8
1495	5.9 + j8.80	1.5 – j5.46	155	56.4	17.7
Maximum drain efficiency load					
1450	3.6 + j7.51	3.3 – j3.7	107	68.9	20.3
1495	5.9 + j8.80	2.7 – j3.6	112	69.8	20.1

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 700 mA (peak); V_{DS} = 30 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1450	2.5 + j7.07	1.4 – j5.11	295	61.0	16.4
1495	3.7 + j8.37	1.5 – j5.46	288	61.3	16.6
Maximum drain efficiency load					
1450	2.5 + j7.07	2.3 – j4.4	234	65.6	18.2
1495	3.7 + j8.37	1.7 – j4.6	251	66.4	17.6

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

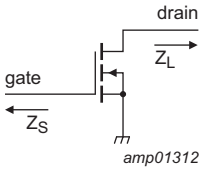
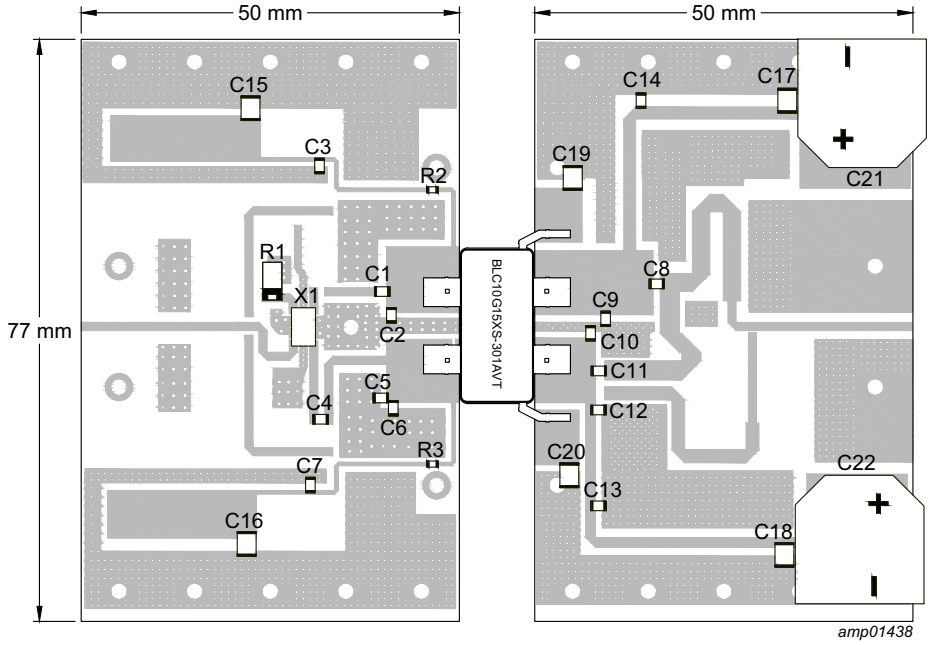


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.508 mm; thickness copper plating on both sides = 35 μm.

See Table 11 for a list of components.

Fig 2. Component layout

Table 11. List of components

See Figure 2 for component layout.

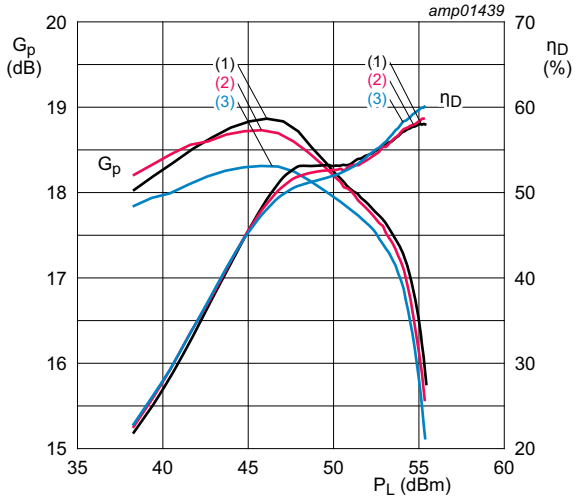
Component	Description	Value	Remarks
C1, C3, C4, C7, C11, C13, C14	multilayer ceramic chip capacitor	20 pF [1]	
C2, C5	multilayer ceramic chip capacitor	2.4 pF [1]	
C6	multilayer ceramic chip capacitor	0.6 pF [1]	
C8	multilayer ceramic chip capacitor	9.1 pF [1]	
C9	multilayer ceramic chip capacitor	1.2 pF [1]	
C10	multilayer ceramic chip capacitor	5.1 pF [1]	
C12	multilayer ceramic chip capacitor	1 pF [1]	
C15, C16, C17, C18	multilayer ceramic chip capacitor	10 μF, 50 V [2]	
C19, C20	multilayer ceramic chip capacitor	1 μF, 50 V [1]	
C21, C22	electrolytic capacitor	1000 μF, 100 V	
R1	resistor	50 Ω	SMD 0805
R2, R3	resistor	5.6 Ω	SMD 0805
X1	hybrid coupler		Anaren: X3C15F1-02S

[1] American Technical Ceramics type 600F or capacitor of same quality.

[2] Murata or capacitor of same quality.

7.4 Graphical data

7.4.1 Pulsed CW



V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V; t_p = 100 µs; δ = 10 %.

(1) f = 1452 MHz

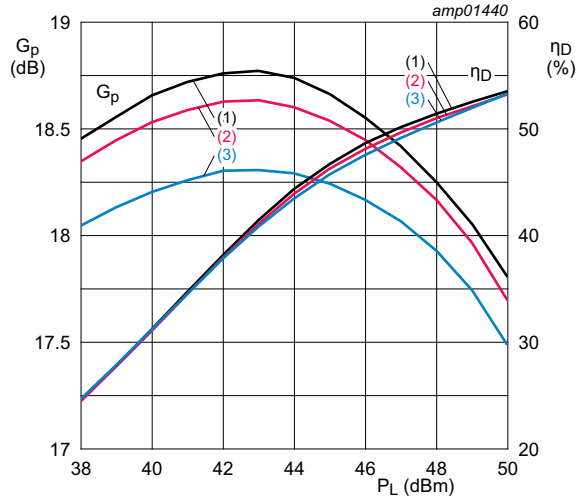
(2) f = 1472 MHz

(3) f = 1492 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values

7.4.2 1-Carrier W-CDMA

Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.



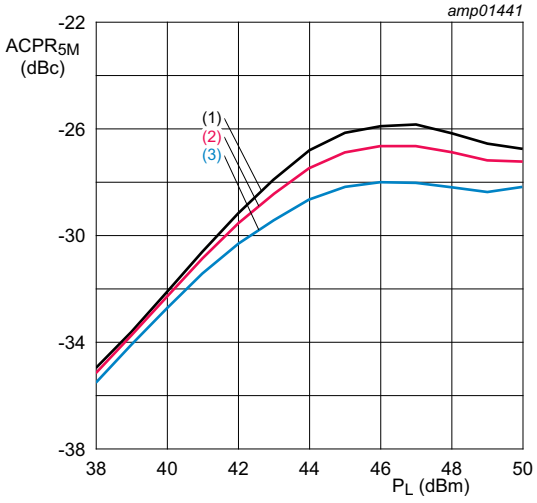
V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V.

(1) f = 1454.5 MHz

(2) f = 1472 MHz

(3) f = 1489.5 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



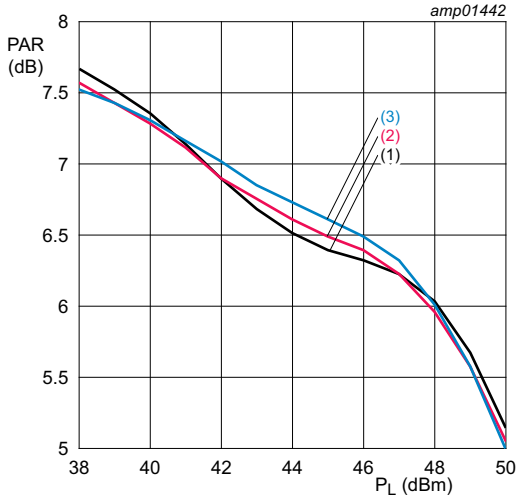
V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V.

(1) f = 1454.5 MHz

(2) f = 1472 MHz

(3) f = 1489.5 MHz

Fig 5. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V.

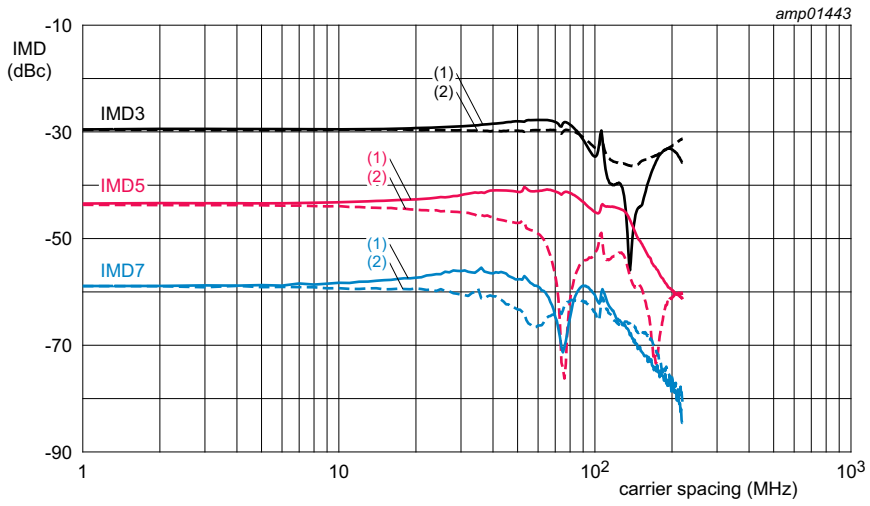
(1) f = 1454.5 MHz

(2) f = 1472 MHz

(3) f = 1489.5 MHz

Fig 6. Peak-to-average power ratio as a function of output power; typical values

7.4.3 2-Tone VBW



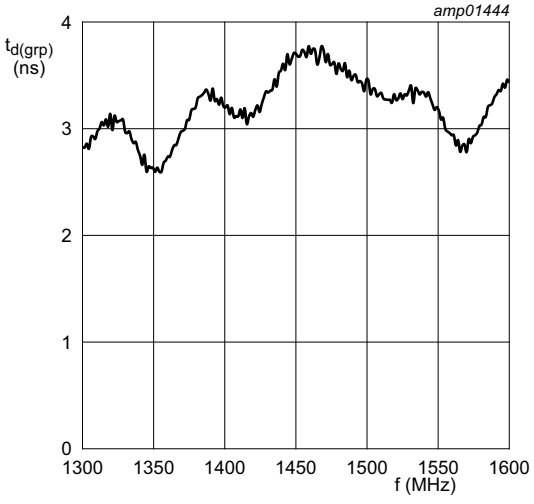
V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V; f = 1472 MHz

(1) IMD low

(2) IMD high

Fig 7. VBW capability

7.4.4 Group delay

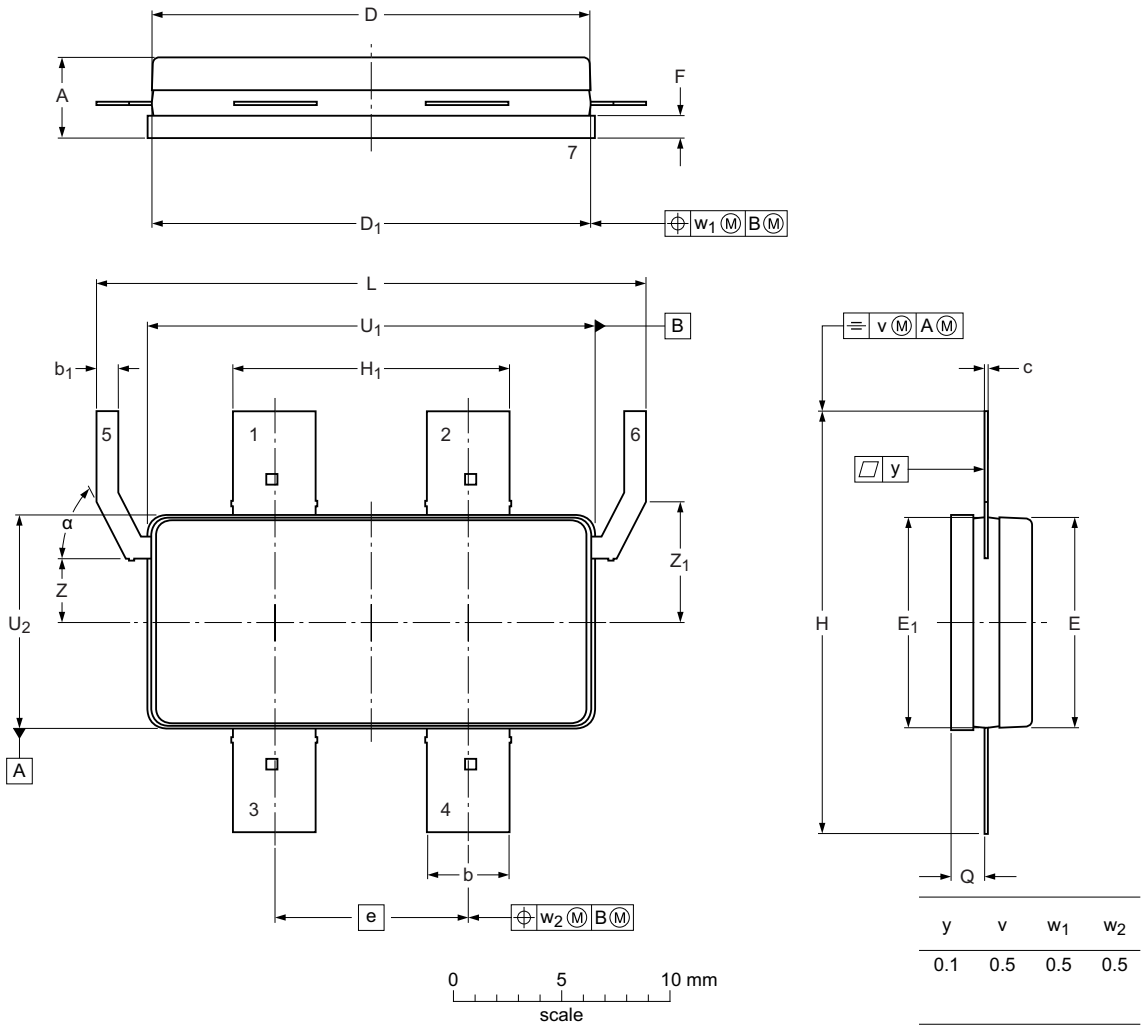


V_{DS} = 30 V; I_{Dq} = 300 mA; $V_{GS(amp)peak}$ = 1.3 V.

Fig 8. Group delay time as a function of frequency; typical values

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1275-1**



y	v	w_1	w_2
0.1	0.5	0.5	0.5

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	L	Q(1)	U_1	U_2	Z	Z_1	α
mm	max	4.01	3.94	1.14	0.178	20.42	20.37	9.80	9.75	8.89	1.14	19.53	12.80	25.40	1.68	20.70	9.91	3.17	5.79	65°
	nom																			
	min	3.40	3.68	0.89	0.127	20.12	20.17	9.50	9.55		0.94	19.33	12.60	25.20	1.45	20.50	9.70	2.67	5.29	61°

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1275-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1275-1						~~16-11-15~~ 17-04-13

Fig 9. Package outline SOT1275-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC10G15XS-301AVT v.1	20200626	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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Date of release: 26 June 2020
Document identifier: BLC10G15XS-301AVT