

# SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

# LC74761 CMOSIC LC74761M CMOSIC On-Screen Display LSI

# Overview

The LC74761 and LC74761M are on-screen display CMOS LSIs that superimpose text and low-level graphics onto a TV screen (video signal) under microcontroller. The display characters have a 12 by 18 dots structure, and 256 characters are provided.

# Features

- Display structure: 12 lines by 24 characters (up to 288 characters)
- Maximum character display: Up to 288 characters
- Character configuration: 12 (W) by 18 (H) dots structure
- Number of characters: 256 characters (254 plus space 1 font and transparent space 1 font)
- Character sizes: Three sizes (normal, double, and triple sizes)
- Display starting positions: 64 horizontal and 64 vertical locations
- Reverse video function: Characters can be inverted on a per character basis.
- Flashing types: Two types with periods of 0.5 and 1.0 second on a per character basis (duty fixed at 50%)
- Background color: One of eight colors (when internal synchronization used)
- External control input: Serial data input in 8-bit units
- Built-in horizontal/vertical sync separation circuit, AFC circuit, and synchronization detector
- Video output: Composite video signal output in NTSC, PAL, PAL-M, PAL-N, PAL60, NTSC4.43, or SECAM format

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Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD1</sub> , V <sub>DD2</sub> pins	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
Maximum input voltage	V <sub>IN</sub> max	All input pins	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Maximum output voltage	V <sub>OUT</sub> max	HSYNC <sub>OUT</sub> , VSYNC <sub>OUT</sub> , SYNC <sub>DET</sub> pins	$V_{SS}$ – 0.3 to $V_{DD}$ + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		-30 to +70	°C
Storage temperature	Tstg		-40 to +125	°C

# **Specifications** Absolute Maximum Ratings at $Ta = 25^{\circ}C$

# Allowable Operating Ranges at Ta = -30 to $+70^{\circ}C$

Deveryorten	Oursels at	O a maliti a ma			Ratings		1.1-24
Parameter	Symbol	Conditions		min	typ	max	Unit
Supply voltage	V <sub>DD1</sub>	V <sub>DD1</sub> pin		4.5	5.0	5.5	V
Supply voltage	V <sub>DD2</sub>	V <sub>DD2</sub> pin		4.5	5.0	1.27 V <sub>DD1</sub>	V
	V <sub>IH1</sub>	RST, CS, SIN, SCLK pins		0.8 V <sub>DD1</sub>		V <sub>DD1</sub> + 0.3	V
Input high level voltage	$V_{\text{IH2}}$	SECAM, <u>525</u> /625, NTSC/PAL, <u>3.58</u> /4.43 pins		0.7 V <sub>DD1</sub>		V <sub>DD1</sub> + 0.3	V
	V <sub>IL1</sub>	RST, CS, SIN, SCLK pins		$V_{SS} - 0.3$		0.2 V <sub>DD1</sub>	V
Input low level voltage	V <sub>IL2</sub>	SECAM, <u>525</u> /625, NTSC/PAL, <u>3.58</u> /4.43 pins	V <sub>SS</sub> – 0.3		0.3 V <sub>DD1</sub>	V	
Input voltage	V <sub>IN</sub>	FC, AMP <sub>IN</sub> pins		$V_{SS} - 0.3$		V <sub>DD1</sub> + 0.3	V
	V <sub>IN1</sub>	CVIN pins			$2 V_{PP}$		V
Composite video signal input voltage	V <sub>IN2</sub>	CV <sub>CR</sub> pins			$2 V_{PP}$		V
	V <sub>IN3</sub>	SYNC <sub>IN</sub> pins			$2 V_{PP}$	2.5 V <sub>PP</sub>	V
			NTSC		14.318		MHz
Oppillator fragmanau		Xtal <sub>IN1</sub> , Xtal <sub>OUT1</sub> , Xtal <sub>IN2</sub> ,	PAL		17.734		MHz
Oscillator frequency	F <sub>OSC1</sub>	Xtal <sub>OUT2</sub> pins; 4fsc			14.302		MHz
			PAL-N		14.328		MHz

# Electrical Characteristics at Ta = -30 to $+70^{\circ}$ C, with $V_{DD1} = V_{DD2} = 5$ V unless otherwise specified

Parameter	Cumhal	Conditions		Ratings		Unit
Parameter	Symbol	Conditions	min	typ	max	Unit
Output off leakage current	I <sub>leak1</sub>	CV <sub>OUT</sub> pin			10	μA
Input off leakage current	I <sub>leak2</sub>	CV <sub>IN</sub> , CV <sub>CR</sub> pins			10	μA
Output high level voltage	V <sub>OH</sub>	$\label{eq:sync_out} \begin{array}{l} HSYNC_{OUT}, VSYNC_{OUT}, \\ \underline{SYNC}_{DET},  \underline{SECAM},  \overline{525}/625, \\ \overline{NTSC}/PAL,  \overline{3.58}/4.43,  AMP_{OUT}, \\ PD_{OUT}  pins;  V_{DD1} = 4.5  V,  I_{OH} = -1.0   mA \end{array}$	3.5			V
Output low level voltage	V <sub>OL</sub>	$\begin{array}{l} \mbox{HSYNC}_{OUT}, \mbox{VSYNC}_{OUT}, \\ \mbox{SYNC}_{DET}, \mbox{SECAM}, \mbox{525}/625, \\ \mbox{NTSC}/PAL, \mbox{3.58}/4.43, \mbox{AMP}_{OUT}, \\ \mbox{PD}_{OUT} \mbox{pins}; \mbox{V}_{DD1} = 4.5 \mbox{ V, } I_{OL} = 1.0 \mbox{ mA} \end{array}$			1.0	V
Input current	I <sub>IH</sub>	$eq:rescaled_$			1	μΑ
input current	I <sub>IL</sub>	$\frac{\text{SECAM, }\overline{525}\text{/}625, }\overline{\text{NTSC}\text{/PAL},} \\ \overline{3.58}\text{/}4.43 \text{ pin; } \text{V}_{\text{IN}} = \text{V}_{\text{SS1}} \\ \end{array}$	-1			μΑ
Oscillator frequency	F <sub>OSC3</sub>	$VCO_{IN}$ , $VCO_{OUT}$ pins; $FC = 1/2 V_{DD1}$		14.12		MHz
Operating current dissipation	I <sub>DD1</sub>	V <sub>DD1</sub> pin; All outputs open, Xtal: 4fsc			15	mA
	I <sub>DD2</sub>	$V_{DD2}$ pin; $V_{DD2}$ = 5.0 V			20	mA

# Timing Characteristics at Ta = –30 to +70°C, $V_{DD}$ = 5 ±0.5 V

Parameter	Cumhal	Conditions		Ratings		Linit	
Parameter	Symbol	Symbol Conditions		typ	max	Unit	
Minimum input pulse width	t <sub>W(SCLK)</sub>	SCLK pin	200			ns	
	t <sub>W(CS)</sub>	$\overline{\text{CS}}$ pin (during periods when CS is high)	1			μs	
Data setup time	t <sub>SU(CS)</sub>	CS pin	200			ns	
	t <sub>SU(SIN)</sub>	SIN pin	200			ns	
Data hold time	t <sub>h(CS)</sub>	CS pin	2			μs	
	t <sub>h(SIN)</sub>	SIN pin	200			ns	
One word write time	t <sub>word</sub>	Write time for 8 bits of data	4.2			μs	
	t <sub>wt</sub>	RAM data write time	1			μs	

# **Serial Data Input Timing**



# **Package Dimensions**

unit : mm (typ) 3196A [LC74761]



# **Package Dimensions**

unit : mm (typ) 3312 [LC74761M]





Top view

## **Pin Functions**

Pin No.	Symbol	Function	Description
1	V <sub>SS</sub>	Ground	Ground connection
2	Xtal <sub>IN1</sub> Xtal <sub>OUT1</sub>	Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal. The oscillator can be selected with a command switch.
4	HSYNC <sub>OUT</sub>	Horizontal synchronization output	Outputs the horizontal synchronization signal (AFC). The output polarity can be selected (metal option). Also functions as general output port (command switch).
5 6	Xtal <sub>IN2</sub> Xtal <sub>OUT2</sub>	- Crystal oscillator connection	Connection for the crystal and capacitor used to form the crystal oscillator that generates the internal synchronization signal.
7	VSYNC <sub>OUT</sub>	Vertical synchronization output	Outputs the vertical synchronization signal. The output polarity can be selected (metal option). Also functions as general output port (command switch).
8	CS	Enable input	Enables/disables serial data input. Serial data is enabled when this pin is low (hysteresis input). Pull-up resistor built in (metal option).
9	SIN	Data input	Serial data input (hysteresis input). Pull-up resistor built in (metal option).
10	SCLK	Clock input	Clock input for serial data input (hysteresis input). Pull-up resistor built in (metal option).
11	SECAM	SECAM mode switch input/ output (command switch)	During input, switches between SECAM and other modes. During output, functions as general output port or internal V output (command switch). Low = other modes, high = SECAM mode
12	525/625	525/625 switch input/output (command switch)	During input, switches between 525 scan lines and 625 scan lines. During output, functions as general output port or character data output (command switch). Low = 525 lines, high = 625 lines
13	NTSC/PAL	NTSC/PAL switch input/output (command switch)	Switches the color mode between NTSC and PAL. During output, functions as general output port or frame data output (command switch). Low = NTSC, high = PAL
14	3.58/4.43	3.58/4.43 switch input/output (command switch)	Switch FSC between 3.58 MHz and 4.43 MHz. During output, functions as general output port or half-tone output (command switch). Low = 3.58, high = 4.43
15	RST	Reset input	System reset input pin, low is active (hysteresis input). Pull-up resistor built in (metal option).
16	CV <sub>OUT</sub>	Video signal output	Composite video output
17	V <sub>DD2</sub>	Power supply connection	Power supply connection for composite video signal level generation
18	CVIN	Video signal input	Composite video input
19	CV <sub>CR</sub>	Video signal input	SECAM chroma signal input
20	SYNCIN	Sync separator circuit input	Built-in sync separator circuit video signal input
21	SEPc	Sync separator circuit	Built-in sync separator circuit
22	V <sub>SS</sub>	Ground	Ground connection
23	PD <sub>OUT</sub>	Control voltage output	AFC control voltage output
24	AMPIN	AFC filter connection	Filter connection
25	AMPOUT		
26	FC	Control voltage input	AFC control voltage input
27	VCOIN	LC oscillator connection	VCO LC oscillator circuit coil and capacitor connection
28	VCO <sub>OUT</sub>		
29	SYNC <sub>DET</sub>	External synchronization signal detection output	Outputs the exclusive NOR of the horizontal synchronization signal (AFC) and CSYNC (sync separator). The output polarity can be selected (metal option). Also functions as general output port (command switch).
30	V <sub>DD1</sub>	Power supply connection	Power supply connection (+5 V: digital system power supply)

## System Block Diagram



# **Display Control Commands**

Display control commands are input in an 8-bit serial format. Commands consist of a command identification code in the first byte and data in the second and following bytes. The following commands are supported.

- 1 COMMAND0: Display memory (VRAM) write address setting command
- 2 COMMAND1: Display character data write command
- 3 COMMAND2: Vertical display start position and character size (lines 1 and 2) setting command
- 4 COMMAND3: Horizontal display start position and character size (lines 9 and 11) setting command
- 5 COMMAND4: Display control setting command 1
- 6 COMMAND5: Display control setting command 2
- 7 COMMAND6: Display control setting command 3
- 8 COMMAND7: Display control setting command 4

## **Display Control Command Table**

				First	byte							Secor	nd byte			
Command	Comm	and ider	ntificatio	n code		Da	ata					Da	ata		_	
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	at2	at1	c7	c6	c5	c4	сЗ	c2	c1	c0
COMMAND2 Vertical display start position	1	0	1	0	SZ 21	SZ 20	SZ 11	SZ 10	0	0	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal display start position	1	0	1	1	SZ B1	SZ B0	SZ 91	SZ 90	0	0	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control 1	1	1	0	0	RST	RAM	OSC	RND	0	I/N	BLK 1	BLK 0	BK 1	ATS	0	DSP
COMMAND5 Display control 2	1	1	0	1	PH 2	PH 1	PH 0	I/E	0	TST	CHAL	BLK	RSL 1	RSL 0	CVM	XTS
COMMAND6 Display control 3	1	1	1	0	MOD 3	MOD 2	MOD 1	MOD 0	0	HFI	M30S	SMS	IOS	BCL 1	BCL 0	СВ
COMMAND70 Display control 4	1	1	1	1	0	0	0	LINS	0	VCOS 1	LIN 5	LIN 4	LIN 3	LIN 2	LIN 1	LIN 0
COMMAND71 Display control 5	1	1	1	1	0	1	0	LINS	0	EG 2	PS 2	PS 1	VMN	SVIS	VNS	VSS
COMMAND72 Display control 6	1	1	1	1	1	0	0	LINS	0	0	0	0	MOD 3	MOD 2	MOD 1	MOD 0
COMMAND73 Display control 7	1	1	1	1	1	1	0	LINS	0	0	0	0	VCOS 2	SOUT	VOUT	HOUT

Once the command identification code in the first bite is written, it is stored internally until the first byte of the following command is written. However, when the display character data write command (COMMAND1) is written, the system becomes locked in display character data write mode, and the first byte cannot be overwritten.

When the  $\overline{\text{CS}}$  pin is set high the command state is set to COMMAND0, i.e., display memory write address setting mode.

## 1 COMMAND0: Display Memory Write Address Setting Command

#### First data byte

	Desister serve		Register content	Nete
DA0 to DA7	Register name	State	Function	Note
7	—	1		
6	—	0	The command 0 identification code:	
5	—	0	sets the display memory write address.	
4	—	0		
2	3 V3 –	0		
3		1		
2	V2	0		
2	V2	1	Display memory line address (from 0 to B (hexadecimal))	
1	1 V1	0	Display memory line address (nom o to b (nexadecimal))	
I VI		1		
0	0 V0	0		
0	v0	1		

## Second byte

	<b>D</b>		Register content	N	
DA0 to DA7	DA0 to DA7 Register name		Function	Note	
7	—	0	Second byte identification code		
6	—	0			
5	—	0			
4	H4	0			
4	114	1			
3	H3	0			
5	115	1			
2	H2	0	Display memory character address (from 0 to 17 (hexadecimal))		
2	112	1	Display memory character address (non 0 to 17 (nexadecimal))		
1	1 H1	0			
1 111	1				
0	0 H0	0			
0					

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

## 2 COMMAND1: Display Character Data Write Setting Command

	Desistant		Register content	Ninte			
DA0 to DA7	Register name	State	Function	Note			
7	—	1					
6	—	0	The command 1 identification code:	When this command is entered, the chip locks in display character write			
5	—	0	sets the display memory write address.	mode until the $\overline{CS}$ pin is set high.			
4	—	1					
3	—	0					
2	—	0					
1	1 at2	at 2	1 010	1 010	0	Turns character attribute 2 off.	Specifies highlight or flashing.
		1	Turns character attribute 2 on.	opeones nightight of hashing.			
0	at1	0	Turns character attribute 1 off.	Specifies reverse video.			
0	at 1	1	Turns character attribute 1 on.				

# LC74761, LC74761M

## Second byte

	<b>D</b>		Register content		
DA0 to DA7	Register name	State	Function	Note	
7	c7	0			
1	67	1			
6	6 c6	0			
0		1			
5	c5	0			
5		1			
4		0			
		1	Character code (from 00 to FF (hexadecimal))		
3	c3	0			
		1			
2	c2	0			
		1			
1		0			
		1			
0	c0	0			
Ĵ	0 00				

Note: When the chip is reset by the  $\overrightarrow{\text{RST}}$  pin, the register states (bits) are all cleared to 0.

## 3 COMMAND2: Vertical Display Position Setting Command

## First byte

				Register content		
DA0 to DA7	Register name	State		Function	Note	
7	—	1				
6	—	0	The command 2 i	dentification code:		
5	—	1	sets the vertical d	isplay position.		
4	—	0				
3	SZ21	0	SZ20	_		
3	5221	1	SZ21	0	1	Character size for the second line
	0700	0	0	Normal size	Double size	Character size for the second line
2	SZ20	1	1	Triple size	Normal size	
4	SZ11	0	SZ10			
I	5211	1	SZ11	0	1	
	07/0	0	0	Normal size	Double size	Character size for the first line
0	SZ10	1	1	Triple size	Normal size	

## Second byte

	Deviator		Register content	Nete	
DA0 to DA7	Register name	State	Function	Note	
7	—	0	Second byte identification code		
6	_	0			
5	VP5	0	The vertical display start position is given by		
Э	(MSB)	1	5		
4	VP4	0	$VS = H \times (\sum_{n=0}^{5} 2^{n} VPn)$		
4 VP4		1	where H is the horizontal synchronization pulse period.		
3	VP3	0	HSYNC	The six bits VD0 to VD5 exectly the	
3	VP3	1		The six bits VP0 to VP5 specify the vertical display start position.	
2	VP2	0		The weight of the lsb is $1 \times H$ .	
2	VP2	1	l (vs		
	0				
I	VP1	1	(haraatar		
0	VP0	0	HS display area		
0	(LSB)	1			

# 4 COMMAND3: Horizontal Display Position Setting Command

#### First byte

	Desistances			Register content	Nete	
DA0 to DA7	Register name	State		Function		Note
7	—	1				
6	—	0	The command 3	identification code:		
5	—	1	sets the horizonta	al display position.		
4	—	1				
3	SZB1	0	SZB0			
3	3201	1	SZB1	0	1	The character size for the eleventh line.
	0750	0	0	Normal size	Double size	The character size for the eleventh line.
2	SZB0	1	1	Triple size	Normal size	
	0701	0	SZ90			
1	SZ91	1	SZ91	0	1	
_		0	0	Normal size	Double size	The character size for the ninth line.
0	SZ90	1	1	Triple size	Normal size	

## Second byte

	Desistances		Register content	N - + -
DA0 to DA7	Register name	State	Function	Note
7	—	0	Second byte identification code	
6	—	0		
5	HP5	0		
5	(MSB)	1		
4	HP4	0		
4	1114	1	The horizontal display start position is given by	
3	HP3	0		The six bits HP0 to HP5 specify the
5	111.5	1	$HS = Tc \times \left(\sum_{n=0}^{5} 2^{n}HPn\right)$	vertical display start position. The weight of the lsb is 1 x Tc.
2	HP2	0		The weight of the isb is 1 x 1c.
2	TTF Z	1	where Tc is the period of the OSCIN and OSCOUT oscillator in operating mode.	
1	HP1	0	operating mode.	
	1161	1		
0	HP0	0		
0	0 (LSB)			

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

# 5 COMMAND4: Display Control Setting Command 1

	<b>D</b>		Register content	N	
DA0 to DA7 Register name		State	Function	Note	
7	—	1			
6	—	1	The command 4 identification code:		
5	—	0	sets display control parameters.		
4	—	0			
3	DOT	0		This reset occurs when the CS pin goes low, and the reset state cleared when	
3	RST <sub>SYS</sub>	1	Resets all registers. (Clears all registers to 0.)	the $\overline{\text{CS}}$ pin goes high.	
0	DAM	0		The RAM erase function requires at least 500 µs.	
2	RAM <sub>ERS</sub>	1	Erases display RAM. (Sets display RAM to FF (hexadecimal).)	It is executed on DSPOFF.	
1	OSC <sub>STP</sub>	0	Continues crystal oscillator operation.	Only valid with character display off if	
			Stops the crystal oscillator.	external synchronization is used.	
0	0 RND <sub>SEL</sub> 0		Turns off rounding.	Only valid for double and triple size	
5			Turns on rounding.	characters.	

# LC74761, LC74761M

## Second byte

				Register content		N
DA0 to DA7	Register name	State		Function		Note
7	—	0	Second byte ide	entification code		
6	INT/NON	0	Interlaced			Switches between interlaced and
0	IN I/NON	1	Non-interlaced			non-interlaced display.
5	BLK1	0	BLK0			
5	DLNI	1	BLK1	0	1	Obernes the blanking size
4	DL KO	0	0	Blanking off	Character size blanking	Changes the blanking size.
4	BLK0	1	1	Frame size blanking	Total area blanking	
0	DK4	0	Flashing period	about 0.5 s		O sta tha flashing a suis d
3	BK1	1	Flashing period	about 1 s		Sets the flashing period.
2	470	0	Highlight function	on		
2	ATS	1	Flashing function	n	Selects at2.	
1	—	0				
0			Character displa	ay off	Turne abaracter output on and off	
0	DSPON	1	Character displa	ay on	Turns character output on and off.	

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

## 6 COMMAND5: Display Control Setting Command 2

				Regist	er content	N							
DA0 to DA7	Register name	State			Function			Note					
7	—	1											
6	—	1	The comma	and 5 identific	cation code:								
5	—	0	sets display	control para	meters.								
4	—	1											
3	PH2	0	PHASE 2	PHASE 1	PHASE 0	Backgro (phase)	und color						
					1		-		NTSC	PAL			
			0	0	0	π/2	±π/2						
		0	0	0	1	In phase	In phase	Sets the phase of the background color					
2	2 PH1		0	1	0	3 π/2	∓π/2	for color burst.sz					
		1	0	1	1	π	±π						
	PH0 -	PH0		1	0	0	3 π/4	±3 π/4					
			PH0	PH0	0	1	0	1	π/4	±π/4			
1					PH0	PH0	PH0	PH0			1	1	0
				1	1	1	5 π/4	∓3 π/4					
0	INT/EXT	0 External synchronization mode					Switches between internal and external						
0		1	Internal syn	chronization	mode			synchronization.					

# Second byte

				Regist	er content		
DA0 to DA7	Register name	State			Function		Note
7	—	0	Second by	e identificatio	on code		
6	тот	0	Normal ope	eration			Test mode should not be used. This bit
6	TST	1	Test mode				should always be zero.
		0	Sets the ch	aracter inten	sity level to about 8	5 IRE (bright white).	
5	CHAL	1	Sets the ch touch of gre		sity level to about 72	Switches the character intensity level.	
		0	Sets the bla as a frame	•	ity level to about 3 I		
4	BKL	1	Sets the bla as a frame	•	ity level to about 13	Switches the blanking intensity level.	
		0	RSL1	RSL0	Intensity level	Amplitude	
3	RSL1	1	0	0	About 15 IRE	About 60 IRE	
			0	1	About 30 IRE	About 60 IRE	Switches the background intensity level
2	RSL0	0	1	0	About 45 IRE	About 60 IRE	,,, _,
L	HOLD	1	1	1	About 55 IRE	About 65 IRE	
	01/	0	Normal CV	output			
1	CV <sub>outmt</sub>	1	CV <sub>out</sub> pede	stal level out	put	7	
0	VTAL	0	Selects XT	AL1			
0	XTALsel	1	Selects XT	AL2		Switches the oscillator circuit	

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

# 7 COMMAND6: Display Control Setting Command 3

			Register content									
DA0 to DA7	Register name	State	Function	Note								
7	_	1										
6	_	1	The command 6 identification code:									
5	_	1	sets display control parameters.									
4	_	0										
					14000	MODA	MODA		0	Sets Fsc to 3.58 MHz.	The logical or of this bit and the Fsc	
3	3 MOD3	1	Sets Fsc to 4.43 MHz.	switching input pin (pin 14) is used.								
		0	Sets the color mode to NTSC.	The logical or of this bit and the color								
2	MOD2	1	Sets the color mode to PAL.	mode switching input pin (pin 13) is used.								
	1 MOD1									0	Sets the number of scan lines to 525 lines.	The logical or of this bit and the scan
1		1	Sets the number of scan lines to 625 lines.	line count switching input pin (pin 12) is used.								
2	MODA	0	Sets the mode to a mode other than SECAM.	The logical or of this bit and the mode								
0 MOD0		1	Sets the mode to SECAM mode.	switching input pin (pin 11) is used.								

## Second byte

	<b>D</b>			Regist	er content	N
DA0 to DA7	Register name	State			Function	Note
7	—	0	Second byt	e identificatio	on code	
6	HALF	0	Normal mo	de		
6	INT	1	Half interna	al synchronou	us mode	
5	P14OUT	0	Half tone of	utput		Colocto D14 (2 59/4 42) output
5	SEL	1	High output	t in internal s	ynchronous mode	Selects P14 (3.58/4.43) output.
4	SECAM	0	In SECAM	mode, only tl	he character frame area is on.	Selects the CVCR "on" period.
4	SEL	1	In SECAM	mode, the er	ntire character display area is on.	Selects the CVCR on period.
3	IOS	0	Sets the mo	ode setting p	in to be an input pin.	Switches the input/output direction of
5	103	1	Sets the mo	ode setting p	in to be an output pin.	the mode setting pins.
		0	BCOL1	BCOL0	Background color	
2	BCOL1	1	0	0	Background color displayed	Determines whether a background color
		-	0	1	No background color (about 13 IRE)	is displayed. (Only valid in internal
1	BCOL0	0	1	0	No background color (about 23 IRE)	synchronization mode.)
	20020	1	1	1	CV <sub>outmt2</sub> (CSYNC)	
0	CBOFF	0	Outputs a c	color burst sig	gnal.	Only valid when either BCOL0 is 1 or
0	CBOFF	1	Stops the o	output of colo	r burst signals.	BCOL1 is 1.

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

# 8 COMMAND70: Display Control Setting Command 4

# First byte

	<b>D</b>		Register content	N
DA0 to DA7	Register name	State	Function	Note
7	—	1		
6	—	1	The command 7 identification code:	
5	—	1	sets display control parameters.	
4	—	1		
3	—	0		
2	—	0	Expansion command 0 identification code	
1	—	0		
0	0 LINS 0 1		Selects the lower 6 bits (bits 0 to 5)	Selects the upper or lower six bits when halftone output line mode is specified.
0			Selects the upper 6 bits (bits 6 to B)	

## Second byte

	<b>D</b>		Register content	N						
DA0 to DA7	Register name	State	Function	Note						
7	—	0	Second byte identification code							
0	VCO	0	VCO frequency is 14.12 MHz							
6	SELECT1	1	VCO frequency is 7.07 MHz	Selects VCO oscillation frequency.						
-		0	Turns off (low) sixth line halftone output.	Used for the line 12 setting when LINS						
5	LIN5	1	Turns on (high) sixth line halftone output.	is high.						
4			1.1514			1.1514		0	Turns off (low) fifth line halftone output.	Used for the line 11 setting when LINS
4	LIN4	1	Turns on (high) fifth line halftone output.	is high.						
0	1.1010	0	Turns off (low) fourth line halftone output.	Used for the line 10 setting when LINS						
3	LIN3	1	Turns on (high) fourth line halftone output.	is high.						
2	1.1110	1.1110	1.11.10	1.1110	1.11.10	0	Turns off (low) third line halftone output.	Used for the line 9 setting when LINS is		
2	LIN2	1	Turns on (high) third line halftone output.	high.						
4				1.1514	0	Turns off (low) second line halftone output.	Used for the line 8 setting when LINS is			
I	1 LIN1 -		Turns on (high) second line halftone output.	high.						
0		0 Turns off (low) first line halftone output.		Used for the line 7 setting when LINS is						
U	0 LINO	1	Turns on (high) first line halftone output.	high.						

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

# 9 COMMAND71: Display Control Setting Command 5

#### First byte

DA0 to DA7			Register content	Note
DAU to DA7	Register name	State	Function	Note
7	—	1		
6	—	1	The command 7 identification code: sets display	
5	—	1	control parameters	
4	—	1		
3	—	0	Expansion command 1 identification code	
2	—	1		
1	—	0		
0	0 LINS		Selects lower 6 bits (0 to 5).	Selects lower or upper 6 bits for half tone output line setting.
5			Selects upper 6 bits (6 to B).	

# Second byte

	<b>D</b>		Register content	N
DA0 to DA7	Register name	State	Function	Note
7	—	0	Second byte identification bit	
6	EGMODE	0	Normal display	
0	2SELECT	1	Apply frame to inverted characters also.	
5	PORTSET	0	Set port output data	
5	SELECT2	1	Set port (output switching)	
4	PORTSET	0	Set port output data	
4	SELECT1	1	Set port (output switching)	
3	VMN	0	Normal V signal	
5	SEL	1	VMASK signal	
2	VINPsel	0	Normal I/O	
2	VINF Sei	1	V is input from P11.	
1	VNPsel	0	V rise detection	Selects V detection polarity.
í	i vinesei		V fall detection	Selects V detection polarity.
0	VSEPsel	VCEPsel 0 VSEP is about 9.3 µs.		
0	VGEFSei	1	VSEP is about 18.6 µs.	Selects V separation time.

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

## 10 COMMAND72: Display Control Setting Command 6

	Pagiatar nama		Register content	Noto		
DA0 to DA7 Register name		State	Function	Note		
7	—	1				
6	—	1	The command 7 identification code: sets display			
5	—	1	control parameters			
4	—	1				
3	—	1	Expansion command 2 identification code			
2	—	0	Expansion command 2 identification code			
1	—	0				
0	LINS	0	Selects lower 6 bits (0 to 5).	Selects lower or upper 6 bits for half		
0		1	Selects upper 6 bits (6 to B).	tone output line setting.		

## LC74761, LC74761M

## Second byte

B461 B45	Register name		Register content	
DA0 to DA7		State	Function	Note
7	—	0	Second byte identification bit	
6	—	0		
5	—	0		
4	—	0		
3 MOD3	MOD3	0	Normal MOD3 (P14) output (PS1 = 1)	Specifies port output data
3	SEL	1	Specifies MOD3 general port output	when PS1 = 0.
2 MOD2		0	Normal MOD2 (P13) output (PS1 = 1)	Specifies port output data
2	SEL	1	Specifies MOD2 general port output	when PS1 = 0.
4	MOD1	0	Normal MOD1 (P12) output (PS1 =1)	Specifies port output data
I	SEL 1		Specifies MOD1 general port output	when PS1 = 0.
0	MOD0	0	Normal MOD0 (P11) output (PS1 = 1)	Specifies port output data
0	SEL	1	Specifies MOD0 general port output	when PS1 = 0.

Note: When the chip is reset by the RST pin, the register states (bits) are all cleared to 0.

## 11 COMMAND73: Display Control Setting Command 7

## First byte

DA0 to DA7 Register name			Register content	Noto	
		State	Function	Note	
7	—	1			
6	—	1	The command 7 identification code: sets display		
5	—	1	control parameters		
4	—	1			
3	—	1	Expansion command 3 identification code		
2	—	1	Expansion command 3 identification code		
1	—	0			
0	LINS	0	Selects lower 6 bits (0 to 5).	Selects lower or upper 6 bits for half	
0		1	Selects upper 6 bits (6 to B).	tone output line setting.	

#### Second byte

	<b>D</b>		Register content		
DA0 to DA7	Register name	State	Function	Note	
7	—	0	Second byte identification bit		
6	—	0			
5	—	0			
4	—	0			
3 VCP SELECT2		0	No feedback resistance	Specifies VCO oscillator feedback	
		1	Feedback resistance	resistance connection	
2 SDETOUT SEL		0	Normal SOUT (P29) output (PS2 = 1)	Specifies port output data	
		1	Specifies SOUT general port output	when PS2 = 0.	
4	VOUT	0	Normal VOUT (P7) output (PS2 =1)	Specifies port output data	
1 SEL		1	Specifies VOUT general port output	when PS2 = 0.	
0	HOUT	0	Normal HOUT (P4) output (PS2 = 1)	Specifies port output data	
0	SEL			Specifies HOUT general port output	when PS2 = 0.

Note: When the chip is reset by the  $\overline{\text{RST}}$  pin, the register states (bits) are all cleared to 0.

# **Display Configuration**

The display consists of 12 rows of 24 characters each. Up to 288 characters can be displayed unless enlarged characters are displayed. Display memory addresses are expressed as a row address in the range 0 to B (hexadecimal) and a column address in the range 0 to 17 (hexadecimal).

## **Display Configuration and Display Memory Addresses**

24 characters by 12 rows







Output voltage (VDC)	1.465	1.429	1.212	1.080	0.800	
Output level	Frame level 1	Pedestal level	Background low level 1	Burst low level	Sync level	

Output level	Output voltage (VDC)
Character level 1	2.638
Character level 2	2.449
Background high level 2	2.262
Background high level 1	2.047
Burst high level	1.747
Frame level 2	1.610





Output level	Output voltage (VDC)
Character level 1	2.841
Character level 2	2.652
Background high level 2	2.456
Background high level 1	2.242
Burst high level	1.943
Frame level 2	1.811





Output level	Frame level 1	Pedestal level	Background low level 1	Burst low level	Sync level		
Output voltage (VDC)	3.342	3.153	2.950	2.735	2.436	2.312	
Output level	Character level 1	Character level 2	Background high level 2	Background high level 1	Burst high level	Frame level 2	

Output voltage (VDC)

2.166 2.118 1.902 1.770

# **Application Circuit Diagram**



A02566

Signal format	4 Fsc (MHz)	Signal format	SW1	SW2	SW3	SW4
NTSC	3.579545 × 4	NTSC	0	0	0	0
PAL	4.433618 × 4	PAL	0	1	1	1
SECAM	4.433618 × 4	SECAM	1	(1)	(1)	(1)
PAL-M	3.575611 × 4	PAL-M	0	0	1	0
PAL-N	3.582056 × 4	PAL-N	0	1	1	0
NTSC4.43	4.433618 × 4	NTSC4.43	0	0	0	1
PAL60	4.433618 × 4	PAL60	0	0	1	1

Note: Fix SW1 to SW4 to 0 when setting a mode by command.

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