

AKM**AP1152****300mA Output, High PSRR, Low Noise LDO Regulator****1. General Description**

The AP1152 is a low dropout linear regulator with On/Off control, which can supply 200mA load current. The output voltage, trimmed with high accuracy, is available from 1.3 to 9.5V in 0.1V steps, and the output capacitor is available to use a small 0.1 μ F ceramic capacitor ($2.5V \leq V_{OUT}$).

The AP1152 has a built-in over-current protection and thermal shutdown protection circuit, and is possible to provide two types of package, the AP1152ADUXX is the SOT89-5 package and the AP1152AEUXX is the PLP1822-6 package with Exposed Pad.

2. Features

- Operating Temperature Range -40 to 85°C
- Operating Voltage Range 2.1 to 14.5V
- Output Current 300mA
- Settable range of output voltage 1.3 to 9.5V
- Output Voltage Precision $\pm 1.5\%$ or $\pm 50mV$
- Dropout Voltage 105mV at $I_{OUT}=100mA$
- Ripple Rejection 80dB at 1kHz
- Available very low noise application
- Available to use a small ceramic capacitor
- On/Off control (High active)
- Built-in Short circuit protection, thermal shutdown
- Package AP1152ADUXX : SOT89-5
 AP1152AEUXX : PLP1822-6 (with Exposed Pad)

3. Applications

- RF Power Supplies PLL, VCO, Mixer, LNA
- Low Noise Image Sensor Unit Digital Still Camera
- High Speed/High Precision A-D, D-A, Amplifier Audio Equipment
 Medical Equipment
 Instrumentation
- Precision Power Supplies
- Post Regulator for Switching Supplies Car Infotainment

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5. Block Diagram

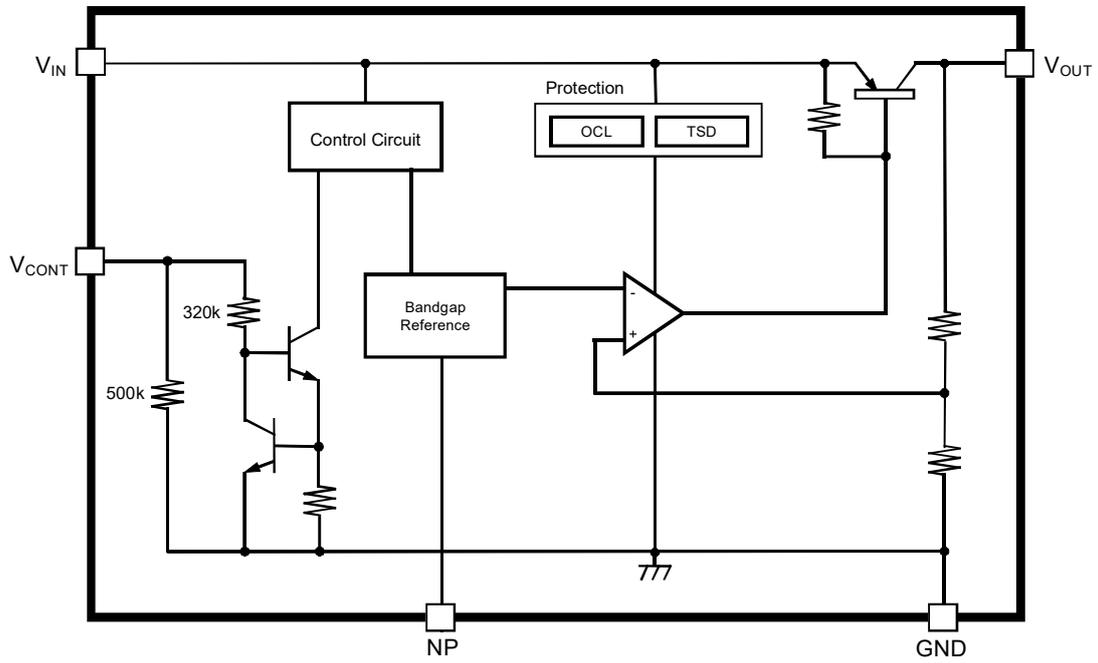


Figure 1. Block Diagram

| |
|--------------------------------|
| 6. Ordering Information |
|--------------------------------|

| | | |
|-------------|------------------|-----------|
| AP1152ADUXX | Ta = -40 to 85°C | SOT89-5 |
| AP1152AEUXX | Ta = -40 to 85°C | PLP1822-6 |

• **Output Voltage Code**

Please check [Table 1](#) for output voltage code. Please consult our distributor for consideration other than the output voltage lineup of [Table 1](#).

AP1152ADUXX

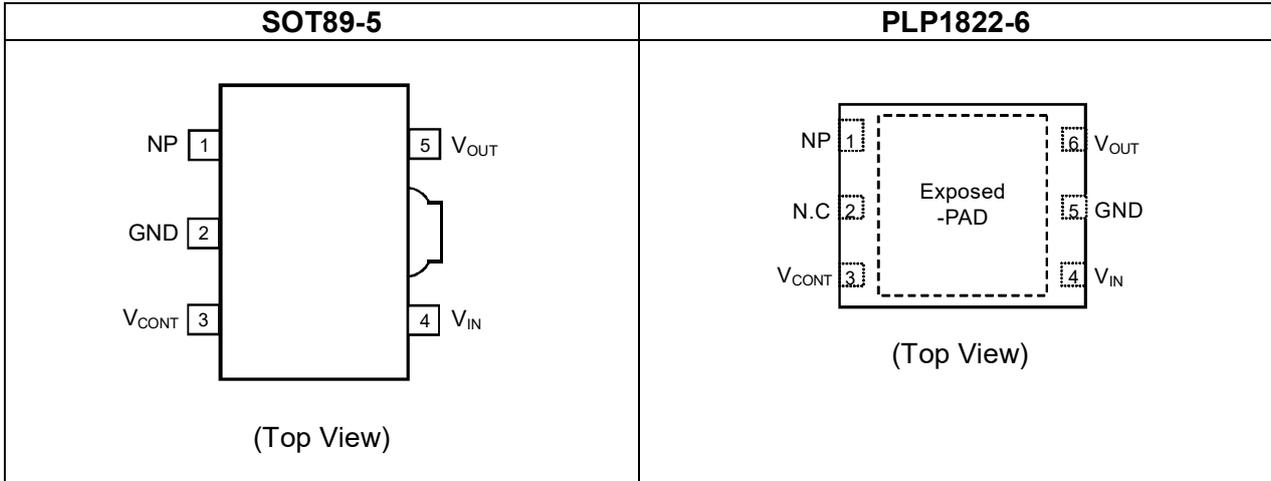

AP1152AEUXX


Table 1. Output Voltage Code

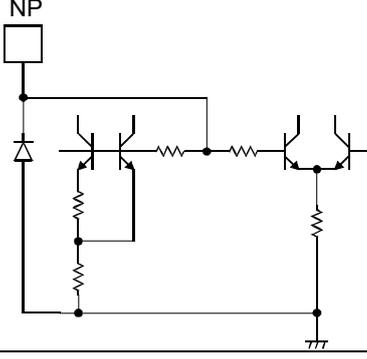
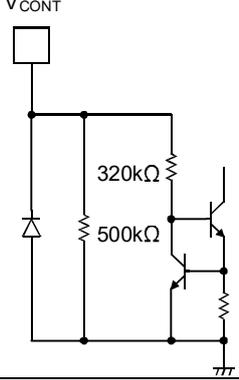
| XX | V _{OUT} |
|----|------------------|----|------------------|----|------------------|----|------------------|----|------------------|
| 18 | 1.8 | 25 | 2.5 | 30 | 3.3 | 40 | 4.0 | 50 | 5.0 |
| | | 28 | 2.8 | 33 | 3.3 | 45 | 4.5 | | |
| | | | | | | | | | |

7. Pin Configuration and Functions

■ Pin Configurations



■ Functions

| Pin No. | | Pin Description | Internal Equivalent Circuit | Description |
|---------|-----------|-----------------|---|--|
| SOT89-5 | PLP1822-6 | | | |
| 1 | 1 | NP |  | Noise Bypass Terminal Connect a bypass capacitor between GND. |
| 2 | 5 | GND | | GND Terminal |
| 3 | 3 | V_{CONT} |  | On/Off Control Terminal The pull-down resistor (500kΩ) is built-in. |
| 4 | 4 | V_{IN} | | Input Terminal |

| Pin No. | | Pin Description | Internal Equivalent Circuit | Description |
|----------|-------------|------------------|-----------------------------|--|
| SOT89 -5 | PLP1822 -6 | | | |
| 5 | 6 | V _{OUT} | | Output Terminal |
| - | 2 | N.C | | No Connection Terminal |
| - | Exposed Pad | - | | Ground Terminal Heat dissipation pad Exposed Pad must be connected to GND. |

8. Absolute Maximum Ratings

| Parameter | Symbol | min | max | Unit | Condition | |
|-----------------------------|-----------------|-------|-----|------|--------------------------|----------|
| Supply Voltage | $V_{CC(MAX)}$ | -0.4 | 16 | V | | |
| Reverse Bias Voltage | $V_{REV(MAX)}$ | -0.4 | 6 | V | $V_{OUT(TYP)} \leq 2.0V$ | |
| | | -0.4 | 12 | V | $2.1V \leq V_{OUT(TYP)}$ | |
| NP Terminal Voltage | $V_{NP(MAX)}$ | -0.4 | 5 | V | | |
| V_{CONT} Terminal Voltage | $V_{CONT(MAX)}$ | -0.4 | 16 | V | | |
| Junction Temperature | T_j | - | 150 | °C | | |
| Storage Temperature Range | T_{STG} | -55 | 150 | °C | | |
| Power Dissipation | SOT89-5 | P_D | - | 900 | mW | (Note 1) |
| | PLP1822-6 | | - | 1500 | mW | (Note 1) |

Note 1. A 4-layer JEDEC51-3 compliant board is used.
 If the temperature exceeds 25°C, be sure to derate at [Figure 2](#).
 SOT23-5 : $\theta_{JA} = 138^\circ\text{C/W}$
 PLP1822-6 : $\theta_{JA} = 83^\circ\text{C/W}$

WARNING: The maximum ratings are the absolute limitation values with the possibility of the IC breakage. When the operation exceeds this standard quality cannot be guaranteed.

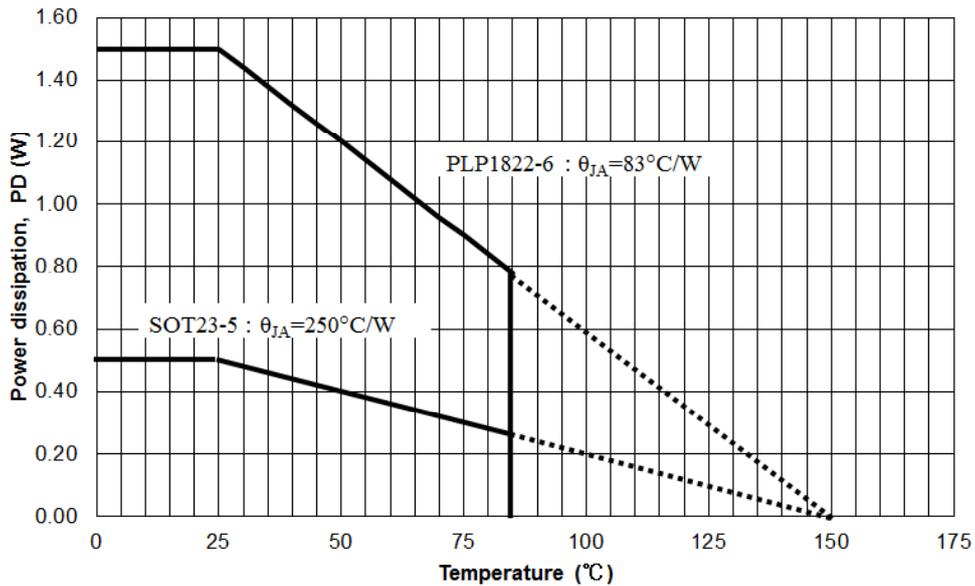


Figure 2. Maximum Power Dissipation

9. Recommended Operating Conditions

| Parameter | Symbol | min | typ | max | Unit | Condition |
|-----------------------------|-----------|-----|-----|------|------|-----------|
| Operating Temperature Range | T_a | -40 | - | 85 | °C | |
| Operating Voltage Range | V_{OP} | 2.1 | - | 14.5 | V | |
| Output Voltage Range | V_{OUT} | 1.3 | - | 9.5 | V | |

| |
|---------------------------------------|
| 10. Electrical Characteristics |
|---------------------------------------|

■ **Electrical Characteristics of Ta=Tj=25°C**

The parameters with min or max values will be guaranteed at Ta=Tj=25°C.

($V_{IN}=V_{OUT}(typ)+1V, V_{CONT}=1.8V, Ta=Tj=25°C$, unless otherwise specified.)

| Parameter | Symbol | Condition | min | typ | max | Unit |
|---|---------------|--|-----------|-----|------|---------|
| Output Voltage | V_{OUT} | $I_{OUT}=5mA$ | (Table 2) | | | V |
| Line Regulation | LinReg | $\Delta V_{IN} = 5V$ | - | 0.0 | 6.0 | mV |
| Load Regulation | LoaReg | $I_{OUT}=5mA\sim 100mA$ | (Table 2) | | | mV |
| | | $I_{OUT}=5mA\sim 200mA$ | | | | |
| | | $I_{OUT}=5mA\sim 300mA$ | | | | |
| Dropout Voltage (Note 2) | V_{DROP} | $I_{OUT}=100mA$ | - | 105 | 170 | mV |
| | | $I_{OUT}=200mA$ | - | 170 | 270 | |
| | | $I_{OUT}=270mA$ ($2.1V \leq V_{OUT} \leq 2.3V$) | - | 235 | 370 | |
| | | $I_{OUT}=300mA$ ($2.4V \leq V_{OUT}$) | - | 235 | 370 | |
| Maximum Output Current (Note 3) | I_{OUTMAX} | $V_{OUT}=V_{OUT(TYP)} \times 0.9$ | 380 | 480 | - | mA |
| Output Short-Circuit Current (Note 3) | I_{SHORT} | | - | 500 | - | mA |
| Quiescent Current | I_Q | $I_{OUT}=0mA$ | - | 65 | 90 | μA |
| Standby Current | $I_{STANDBY}$ | $V_{CONT}=0V$ | - | 0.0 | 0.1 | μA |
| Ground Terminal Current | I_{GND} | $I_{OUT}=100mA$ | - | 1.8 | 3.0 | mA |
| Control Terminal (V_{CONT}) | | | | | | |
| V_{CONT} Terminal Current | I_{CONT} | $V_{CONT}=1.8V$ | - | 5.0 | 10.0 | μA |
| V_{CONT} Terminal Voltage | V_{CONT} | V_{OUT} ON state | 1.8 | - | - | V |
| | | V_{OUT} OFF state | - | - | 0.35 | V |

Note 2. For $V_{OUT} \leq 2.0V$, no regulations.

Note 3. The maximum output current is limited by power dissipation.

Table 2. Output Voltage & Load Regulation

| Part Number | Output Voltage | | | Load Regulation | | | |
|----------------------------|----------------|-------|-------|--------------------------|-----|--------------------------|-----|
| | | | | $I_{OUT} = 100\text{mA}$ | | $I_{OUT} = 200\text{mA}$ | |
| | min | typ | max | typ | max | typ | max |
| | V | V | V | V | V | mV | V |
| AP1150ADS15 AP1150AEU15 | 1.450 | 1.500 | 1.550 | 10 | 23 | 21 | 49 |
| AP1150ADS18 AP1150AEU18 | 1.750 | 1.800 | 1.850 | 10 | 24 | 22 | 51 |
| AP1150ADS30 AP1150AEU30 | 2.950 | 3.000 | 3.050 | 11 | 27 | 26 | 61 |
| AP1150ADS31 AP1150AEU31 | 3.050 | 3.100 | 3.150 | 12 | 27 | 26 | 62 |
| AP1150ADS33 AP1150AEU33 | 3.250 | 3.300 | 3.350 | 12 | 28 | 27 | 64 |
| AP1150ADS45 AP1150AEU45 | 4.432 | 4.500 | 4.568 | 13 | 31 | 31 | 73 |
| AP1150ADS50 AP1150AEU50 | 4.925 | 5.000 | 5.075 | 14 | 32 | 33 | 78 |
| AP1150ADS54 AP1150AEU54 | 5.319 | 5.400 | 5.481 | 14 | 33 | 34 | 81 |

■ Electrical Characteristics of Ta=-40°C to 85°C

The parameters with min or max values will be guaranteed at Ta=-40°C to 85°C.

($V_{IN}=V_{OUT}(typ)+1V, V_{CONT}=1.8V, Ta=-40 \sim 85^{\circ}C$, unless otherwise specified.)

| Parameter | Symbol | Condition | min | typ | max | Unit |
|---|---------------|-------------------------------------|-----------|-----|------|---------|
| Output Voltage | V_{OUT} | $I_{OUT}=5mA$ | (Table 3) | | | V |
| Line Regulation | LinReg | $\Delta V_{IN}=5V$ | - | 0.0 | 8.0 | mV |
| Load Regulation | LoaReg | $I_{OUT}=5mA \sim 100mA$ | (Table 3) | | | mV |
| | | $I_{OUT}=5mA \sim 200mA$ | | | | |
| | | $I_{OUT}=5mA \sim 300mA$ | | | | |
| Dropout Voltage (Note 4) | V_{DROP} | $I_{OUT}=100mA (2.2V \leq V_{OUT})$ | - | 105 | 200 | mV |
| | | $I_{OUT}=200mA (2.2V \leq V_{OUT})$ | - | 170 | 320 | |
| | | $I_{OUT}=300mA (2.4V \leq V_{OUT})$ | - | 235 | 440 | |
| Maximum Output Current (Note 5) | $I_{OUT MAX}$ | $V_{OUT}=V_{OUT(TYP)} \times 0.9$ | 340 | 480 | - | mA |
| Output Short-Circuit Current (Note 5) | I_{SHORT} | | - | 500 | - | mA |
| Quiescent Current | I_Q | $I_{OUT}=0mA$ | - | 65 | 100 | μA |
| Standby Current | $I_{STANDBY}$ | $V_{CONT}=0V$ | - | 0.0 | 0.5 | μA |
| Ground Terminal Current | I_{GND} | $I_{OUT}=100mA$ | - | 1.8 | 3.6 | mA |
| Control Terminal (V_{CONT}) | | | | | | |
| V_{CONT} Terminal Current | I_{CONT} | $V_{CONT}=1.8V$ | - | 5.0 | 12.0 | μA |
| V_{CONT} Terminal Voltage | V_{CONT} | V_{OUT} ON state | 1.8 | - | - | V |
| | | V_{OUT} OFF state | - | - | 0.35 | V |

Note 4. For $V_{OUT} \leq 2.1V$, no regulations.

Note 5. The maximum output current is limited by power dissipation.

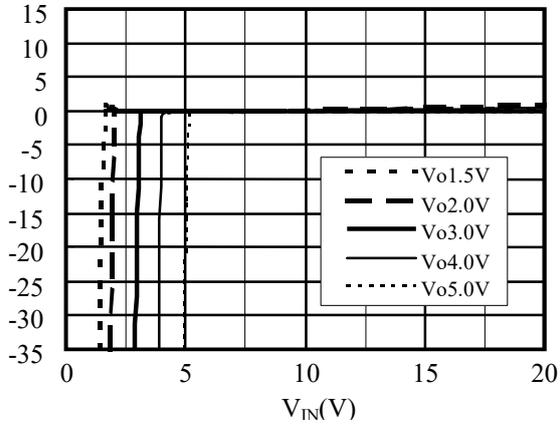
Table 3. Output Voltage & Load Regulation

| Part Number | Output Voltage | | | Load Regulation | | | |
|----------------------------|----------------|-------|-------|--------------------------|-----|--------------------------|-----|
| | | | | $I_{OUT} = 100\text{mA}$ | | $I_{OUT} = 200\text{mA}$ | |
| | min | typ | max | typ | max | typ | max |
| | V | V | V | V | V | mV | V |
| AP1150ADS15 AP1150AEU15 | 1.420 | 1.500 | 1.580 | 10 | 27 | 21 | 63 |
| AP1150ADS18 AP1150AEU18 | 1.720 | 1.800 | 1.880 | 10 | 28 | 22 | 63 |
| AP1150ADS30 AP1150AEU30 | 2.920 | 3.000 | 3.080 | 11 | 32 | 26 | 83 |
| AP1150ADS33 AP1150AEU33 | 3.217 | 3.300 | 3.383 | 12 | 33 | 27 | 88 |
| AP1150ADS40 AP1150AEU40 | 3.900 | 4.000 | 4.100 | 13 | 36 | 29 | 100 |
| AP1150ADS45 AP1150AEU45 | 4.387 | 4.500 | 4.613 | 13 | 38 | 31 | 109 |
| AP1150ADS50 AP1150AEU50 | 4.875 | 5.000 | 5.125 | 14 | 40 | 33 | 117 |

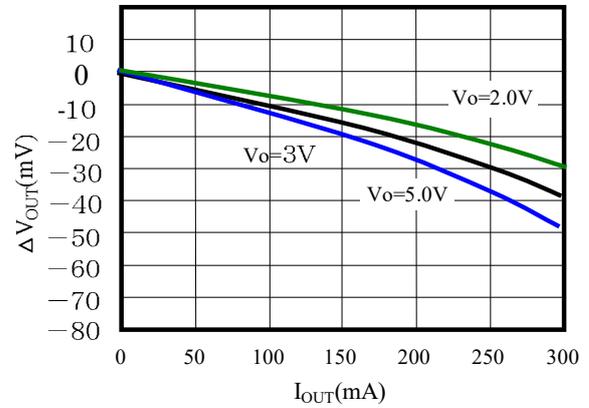
11. Description

11.1 DC Characteristics

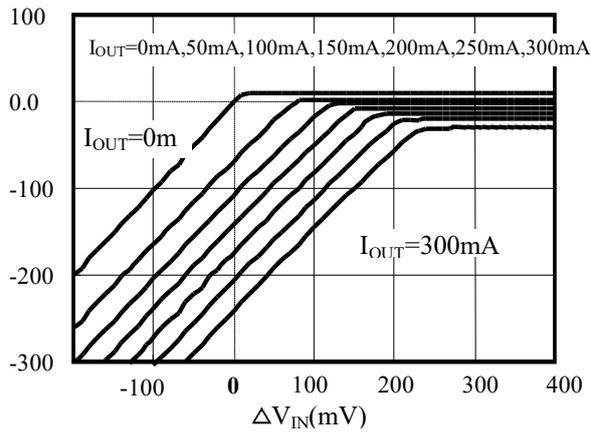
■ Line Regulation



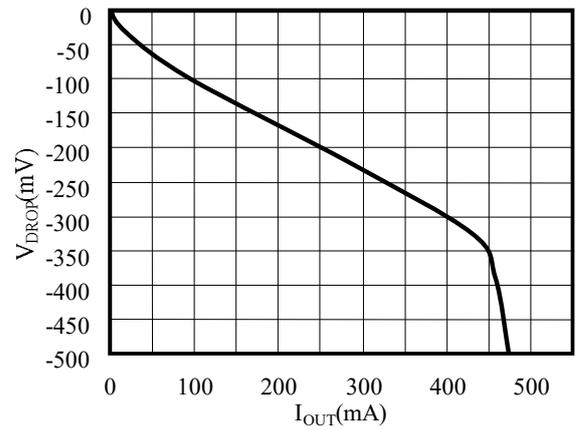
■ Load Regulation



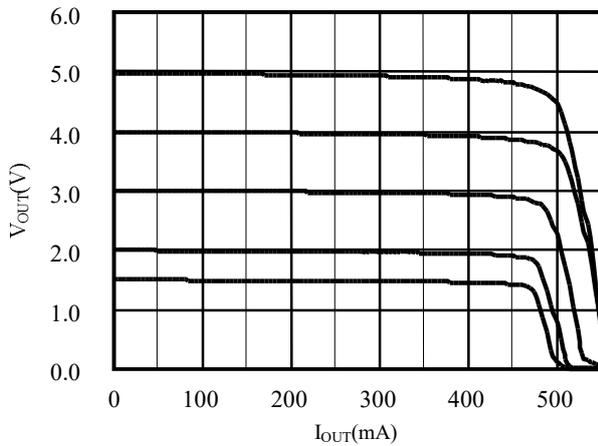
■ V_{IN} vs. V_{OUT} Regulation Point



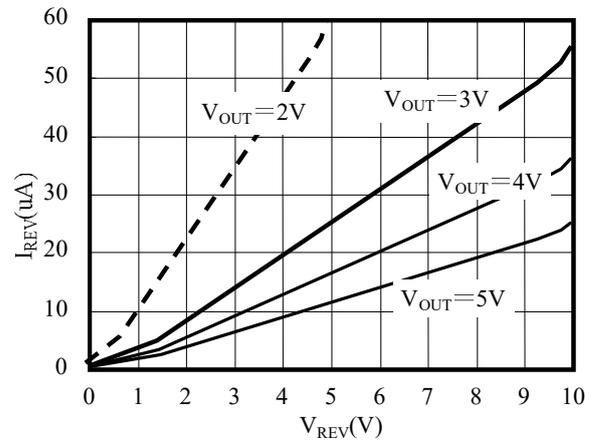
■ Dropout Voltage



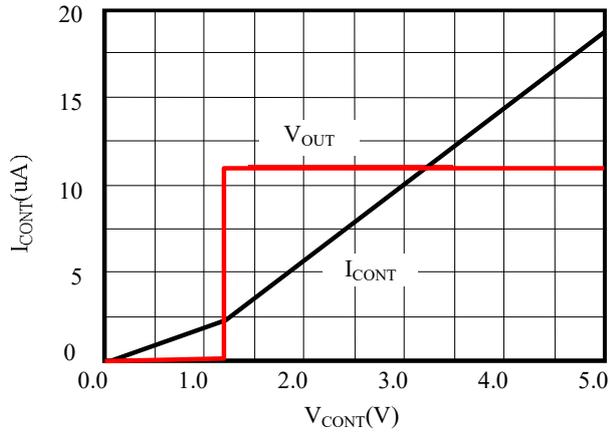
■ Output Short-Circuit Current



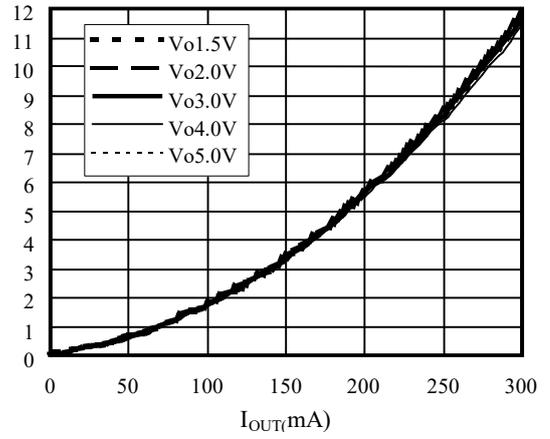
■ Reverse Bias Current



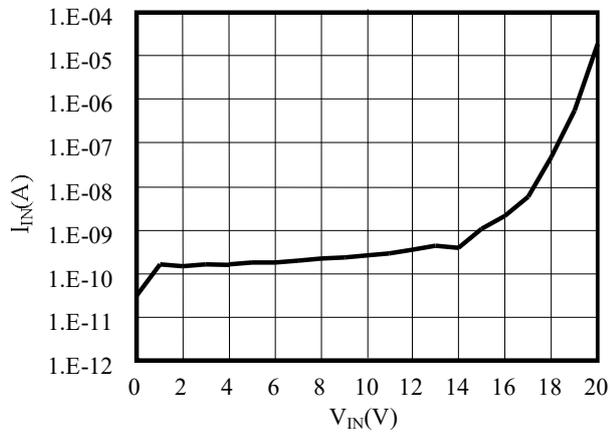
■ CONT Terminal Current and On/Off Point



■ Quiescent Current vs Output Current

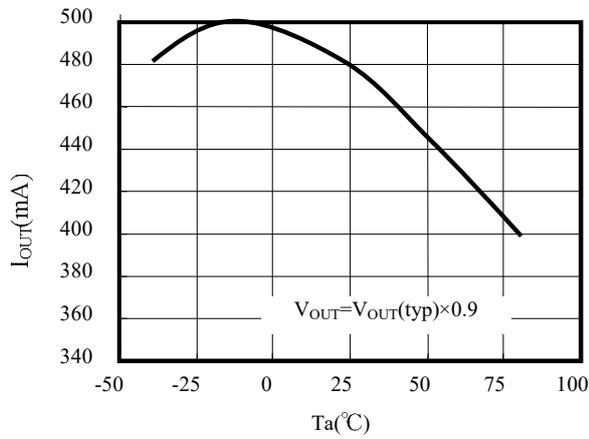


■ Standby Current ($V_{CONT}=0V$)

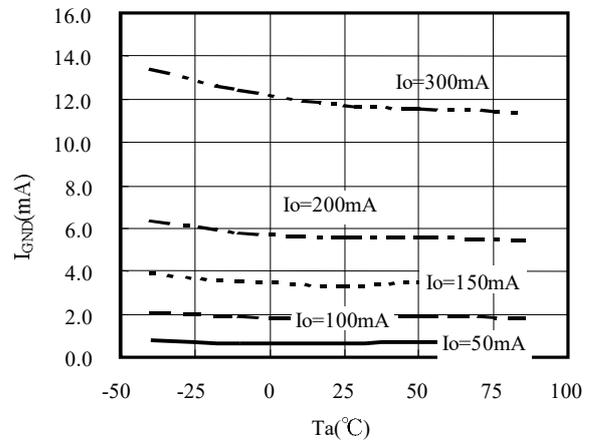


11.2 DC Temperature Characteristics

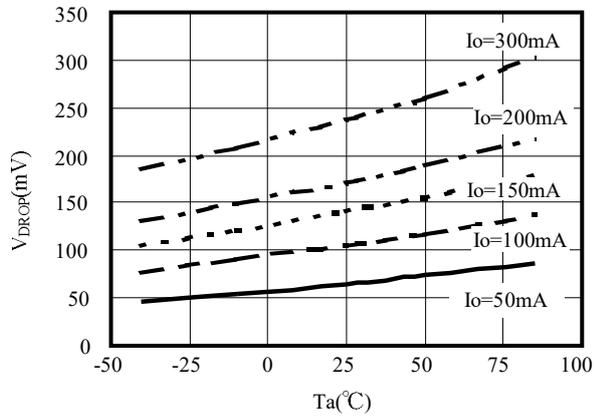
■ Maximum Output Current



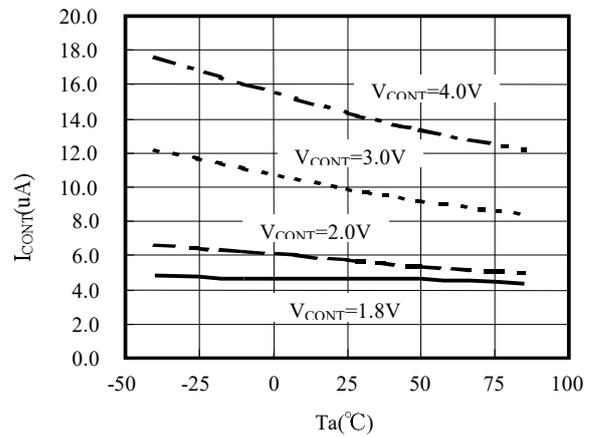
■ Quiescent Current



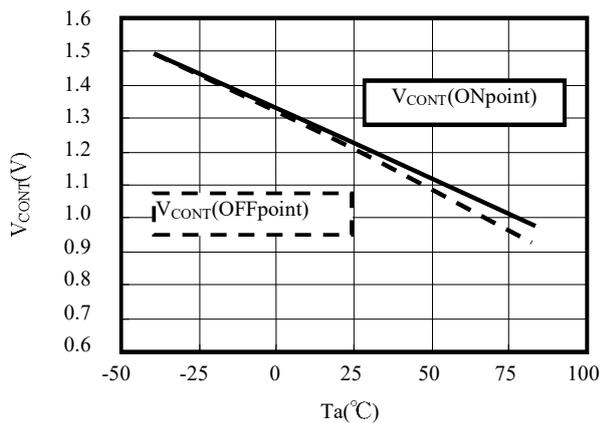
■ Dropout Voltage



■ CONT Terminal Current



■ CONT Terminal On/Off point

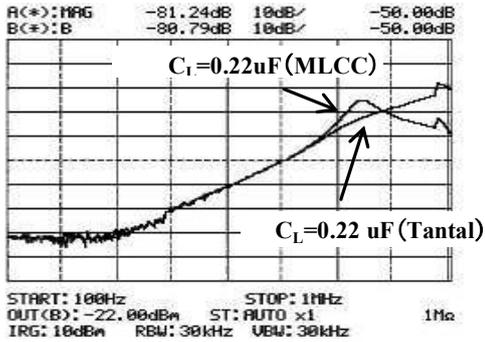


11.3 AC Characteristics

•Ripple Rejection

The ripple rejection characteristic depends on the characteristic and the capacity value of the capacitor connected with the output side. The ripple rejection characteristic of 50kHz or more changes greatly in the capacitor on the output side and PCB pattern. Please confirm stability if necessary while operated.

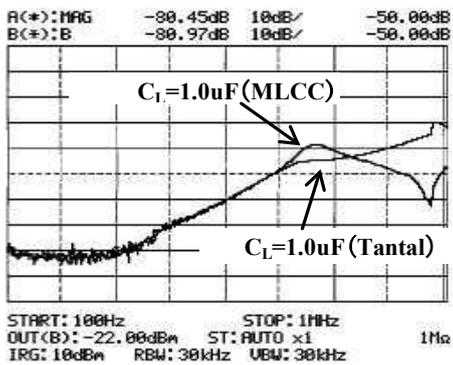
■ MLCC vs. Tantal : $C_L=0.22\mu\text{F}$



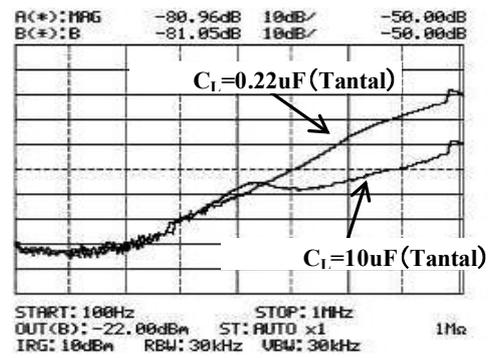
Common conditions are shown as follows:

- $V_{IN}=5.0\text{V}$ ($V_{IN}=V_{OUT.TYP}+2\text{V}$)
- $V_{OUT}=3.0\text{V}$
- $I_{OUT}=30\text{mA}$
- $V_R=500\text{mV}_{P-P}$
- $f=100\text{Hz}$ to 1MHz
- $C_{NP}=0.1\mu\text{F}$

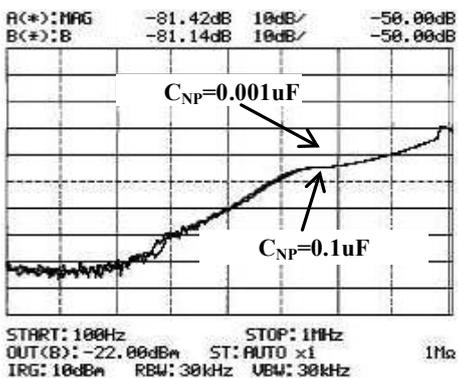
■ MLCC vs. Tantal : $C_L=1.0\mu\text{F}$



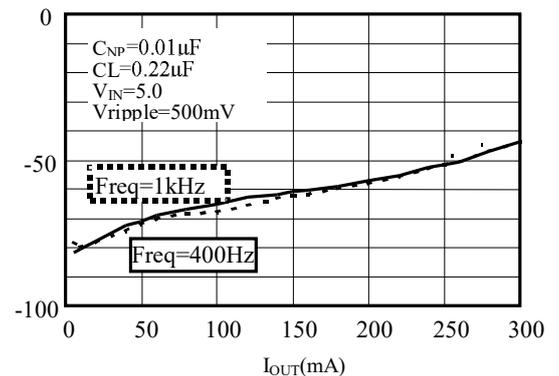
■ Tantal : $C_L=0.22\mu\text{F}$, $10\mu\text{F}$



■ Ripple Rejection vs. C_{NP}



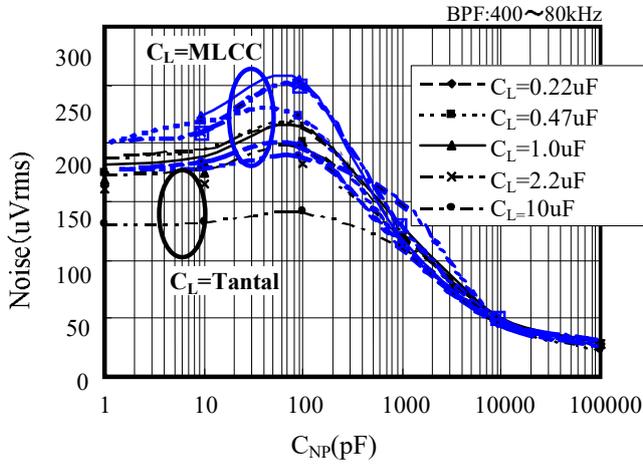
■ Ripple Rejection vs. I_{OUT}



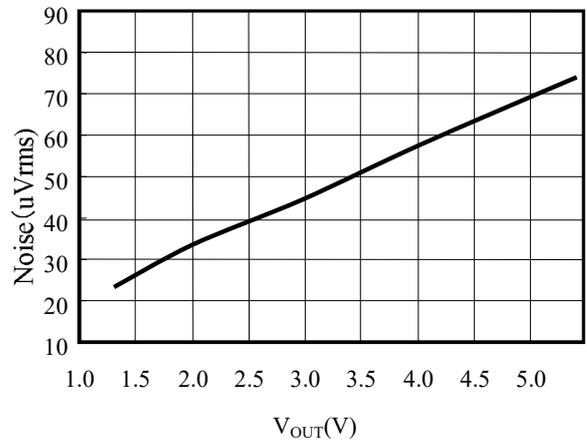
• Output Noise

It is more effective if it increases the C_{NP} than to increase the C_L is the case that require low noise. C_{NP} capacity is recommended 0.01 μ F to 0.1 μ F. Amount of noise will be a lot higher output voltage products.

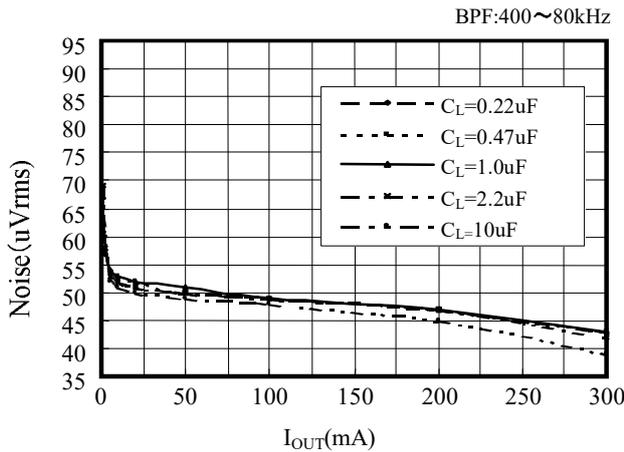
■ Output Noise vs. Noise Pass Capacitance
 $I_{OUT}=30mA$



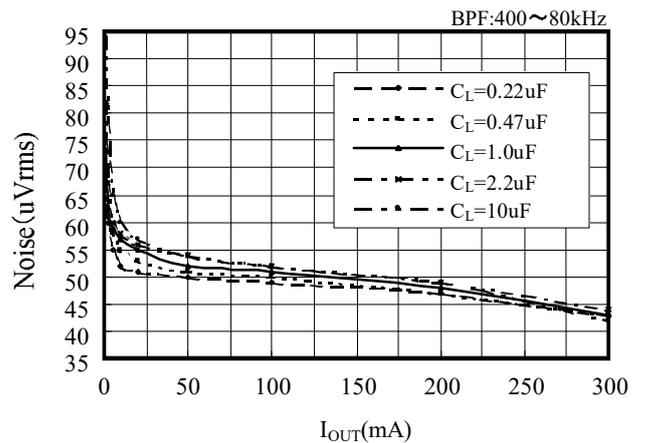
■ Output Noise vs. Output Voltage
 $I_{OUT}=30mA, C_{NP}=10000pF, C_L=0.22\mu F(MLCC)$



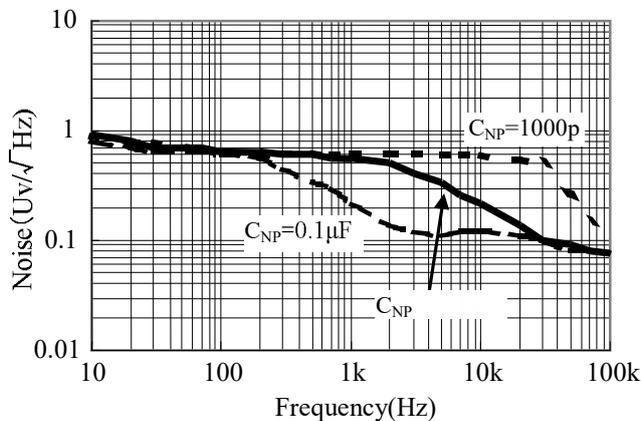
■ Noise vs. Output Current
 $C_L=Tantal, C_{NP}=10000pF$



■ Noise vs. Output Current
 $C_L=MLCC, C_{NP}=10000pF$



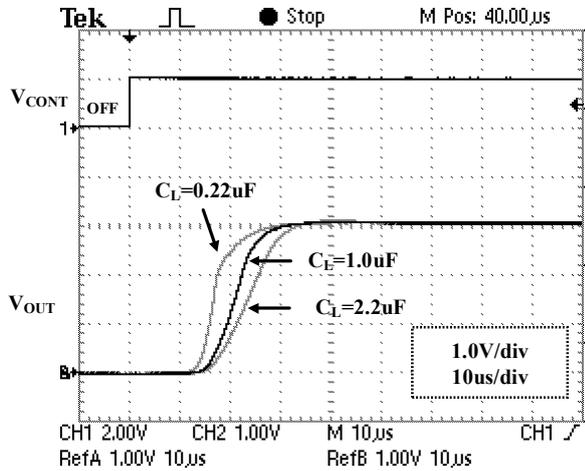
■ Output Noise Level(1/f) vs. Frequency
 $I_{OUT}=10mA, C_{IN}=10\mu F, C_L=0.22\mu F(MLCC)$



•On/Off Transient

The rise time of the IC will be slow and C_L , C_{NP} is large. Rise time is dependent C_L , on the C_{NP} , fall time is dependent on the C_L .

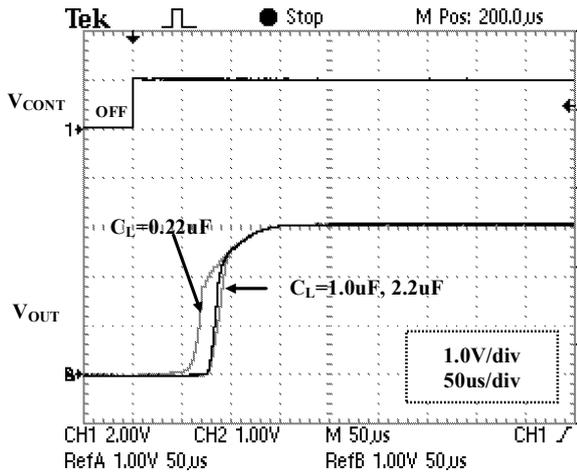
- Parameter: $C_L = 0.22\mu\text{F}, 1.0\mu\text{F}, 2.2\mu\text{F}$
Fixed: $C_{NP} = 0.001\mu\text{F}$



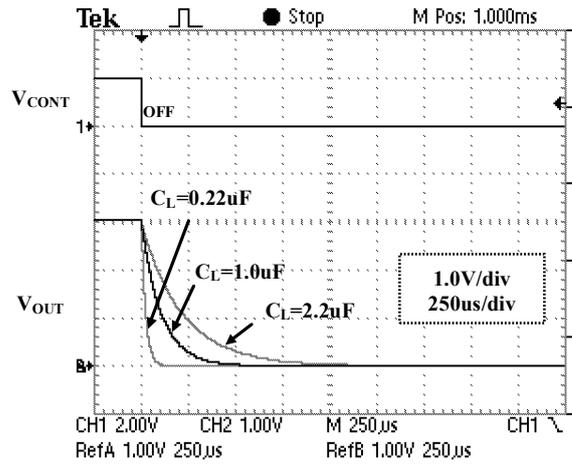
Common conditions are shown as follows:

- $V_{CONT} = 0\text{V} \leftrightarrow 2.0\text{V} @ f = 100\text{Hz}$
- $I_{OUT} = 30\text{mA}$
- $C_{IN} = 1.0\mu\text{F}$
- $C_L = 2.2\mu\text{F}$
- $C_{NP} = 0.001\mu\text{F}$

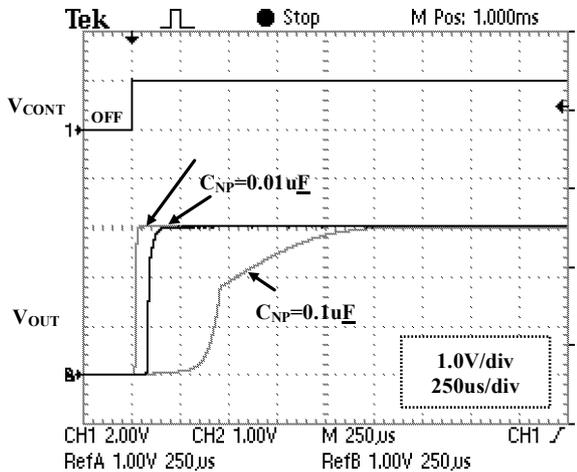
- Parameter: $C_L = 0.22\mu\text{F}, 1.0\mu\text{F}, 2.2\mu\text{F}$
Fixed: $C_{NP} = 0.01\mu\text{F}$



- Parameter: $C_L = 0.22\mu\text{F}, 1.0\mu\text{F}, 2.2\mu\text{F}$
Fixed: $C_{NP} = 0.01\mu\text{F}$



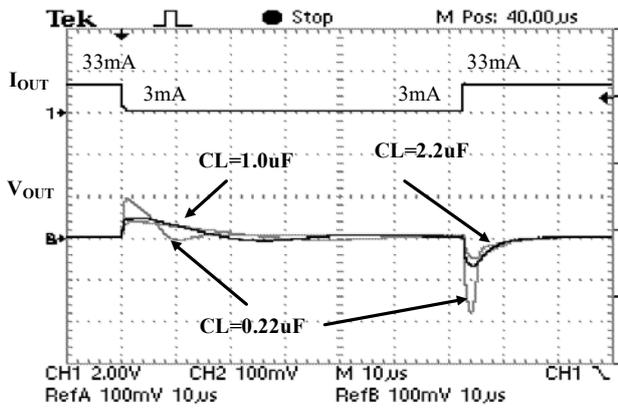
- Parameter: $C_{NP} = 0.001\mu\text{F}, 0.01\mu\text{F}, 0.1\mu\text{F}$
Fixed: $C_L = 1.0\mu\text{F}$



• Load Transient

IC can improve the load change to keep some flow of load current. When there is a fast large current change, please increase the load side capacitor. It can reduce the voltage fluctuation.

- Parameter: $C_L = 0.22\mu\text{F}, 1.0\mu\text{F}, 2.2\mu\text{F}$
- Fixed: $C_{NP} = 0.01\mu\text{F}$

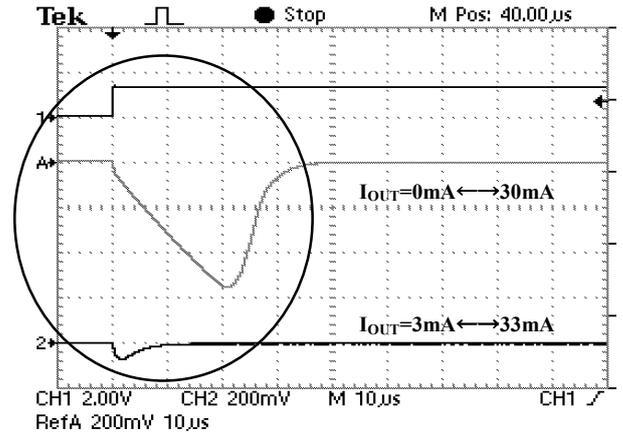
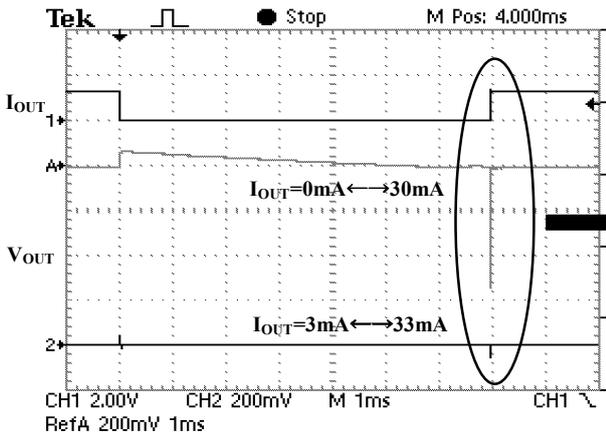


Common conditions are shown as follows:

- $V_{CONT} = 0\text{V} \leftrightarrow 1.8\text{V} @ f = 100\text{Hz}$
- $I_{OUT} = 30\text{mA}$
- $C_{IN} = 1.0\mu\text{F}$
- $C_L = 2.2\mu\text{F}$
- $C_{NP} = 0.01\mu\text{F}$

In addition, it can greatly improve the load change to keep some flow of load current.

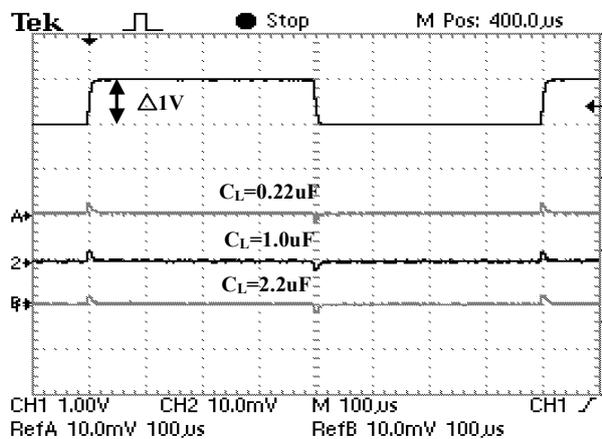
- $I_{OUT} = 0\text{mA} \leftrightarrow 30\text{mA}, 3\text{mA} \leftrightarrow 30\text{mA}$,



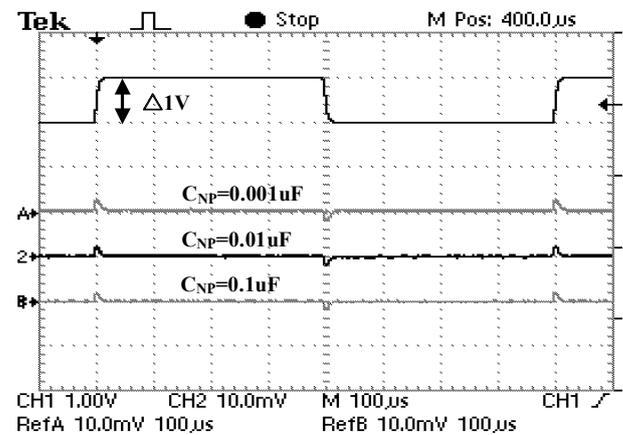
When there is a fast and large current change, please increase the load side capacitor. Please further flowing a little bit of current. Voltage variation can be small.

• Line Transient

■ Parameter : $C_L = 0.22\mu\text{F}, 1.0\mu\text{F}, 2.2\mu\text{F}$
Fixed : $C_{NP} = 0.01\mu\text{F}$



■ Parameter : $C_{NP} = 0.001\mu\text{F}, 0.01\mu\text{F}, 0.1\mu\text{F}$
Fixed : $C_L = 1.0\mu\text{F}$



11.4 About stable operation

AP1152 is required for input and output capacitors in order to maintain the regulator's loop stability.

• Input Capacitor (C_{IN})

The input capacitor is necessary when the battery is discharged, the power supply impedance increases, or the line distance to the power supply is long. This capacitor might be necessary on each individual IC even if two or more regulator ICs are used. It is not possible to determine this indiscriminately. Please confirm the stability while mounted.

The recommended value is $C_{IN} = 1.0\mu\text{F}$.

• Output Capacitor (C_L)

Operation is stabilized by $0.1\mu\text{F}$ ($V_{OUT} \geq 2.1V$) the output side capacitor (C_L). Without taking into account the ESR if C_L is equal to or greater than $0.1\mu\text{F}$ in the entire operating temperature range, it can also be used tantalum capacitor not only the ceramic capacitor.

However, since there are variations in the capacity component, can only capacity, please use larger. And large capacitance value as the output noise and ripple noise is reduced small, furthermore, also improves the response to further output side load fluctuation. The IC does not damage by increasing the capacity. In addition, since the low output voltage product is easier to be oscillation, please use or tantalum capacitor to increase the C_L capacity. More of the tantalum capacitor can be obtained the same stability with a smaller value. This serves as the ESR of the tantalum capacitor damping resistance, are considered IC to a more stable operation.

The recommended value is $C_{IN} = 1.0\mu\text{F}$.

Figure 3 means that IC stable operation with a ceramic capacitor of $0.1\mu\text{F}$ except for the small current region. In the low voltage and low current region does not stable operation is necessary to increase the capacity.

Please select the optimum output capacitor by using voltage and current used. The output side capacitor (C_L) is stable operating larger. (Stable operation area will spread). Please use only the large capacity can be.

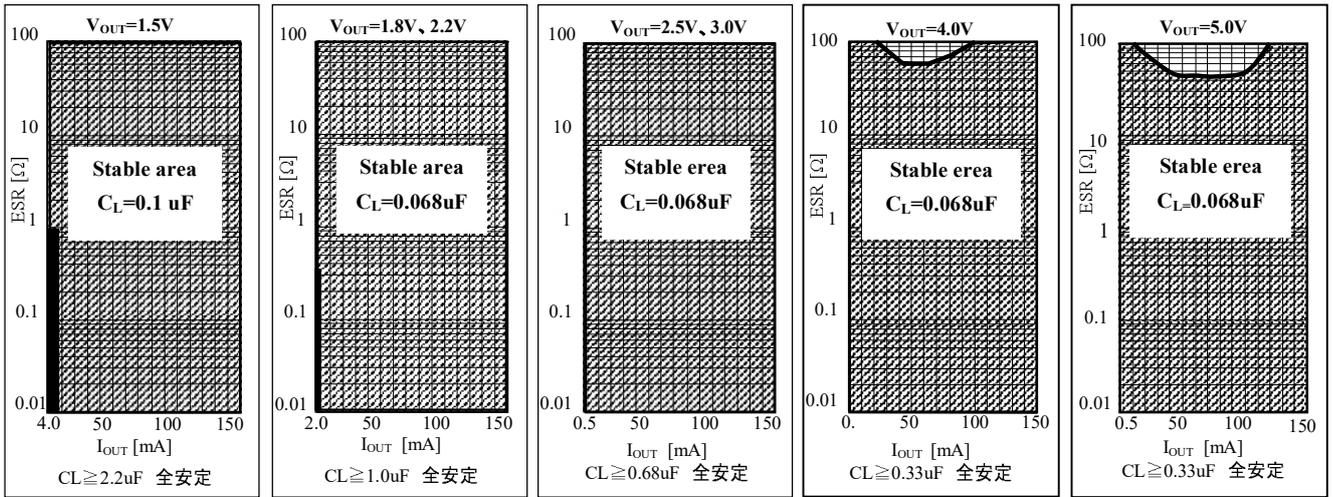


Figure 3. Stable operation area vs. voltage, current, and ESR

Note 6. Capacitor product was used in the evaluation

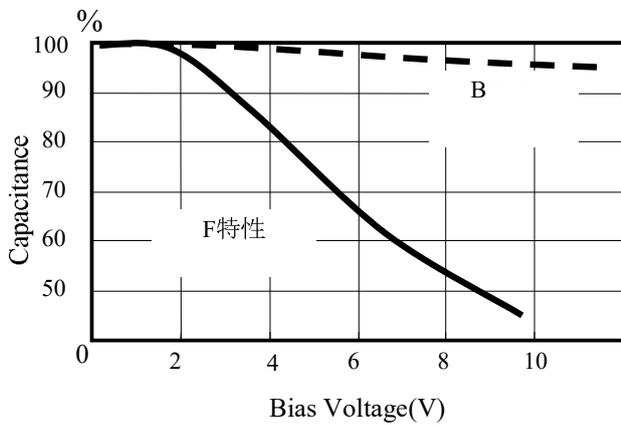
Kyocera:CM05B104K10AB,CM05B224K10AB,CM105B104K16A,CM105B224K16A,CM21B225K10A

Murata:GRM36B104K10,GRM42B104K10,GRM39B104K25,GRM39B224K10,GRM39B105K6.3

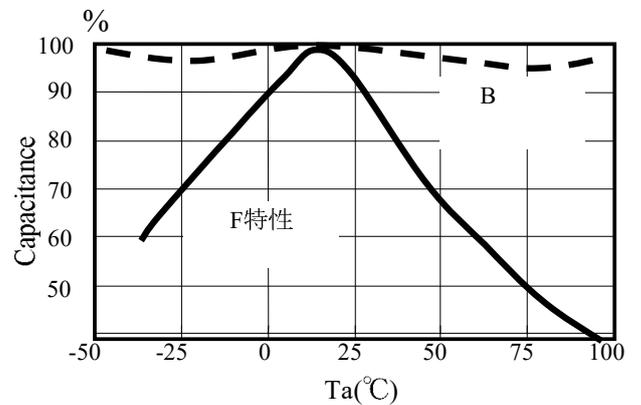
•Bias voltage and temperature characteristics of the ceramic capacitor

Generally, a ceramic capacitor has both a temperature characteristic and a voltage characteristic. Please consider both characteristics when selecting the part. The B curves are the recommend characteristics.

■ Capacitance versus Voltage



■ Capacitance versus Ambient Temperature



11.5 On/Off Control

It is recommended to turn the regulator off when the circuit following the regulator is non-operating. A design with little electric power loss can be implemented. We recommend the use of the on/off control of the regulator without using a high side switch to provide an output from the regulator. A highly accurate output voltage with low voltage drop is obtained. Because the control current is small, it is possible to control it directly by CMOS logic. The pull-down resistor (500kΩ) is built-in.

Table 4. Control terminal voltage and operating state

| Control terminal voltage (V_{CONT}) | Status |
|---|--------|
| $V_{CONT} > 1.8V$ | ON |
| $V_{CONT} < 0.35V$ | OFF |

The Figure 4 is multiple regulators being controlled by a single On/Off control signal. There is fear of overheating, because the power loss of the low voltage side IC (AP1152ADU20) is large. The series resistor (R) is put in the input line of the low output voltage regulator in order to prevent over-dissipation. The voltage dropped across the resistor reduces the large input-to-output voltage across the regulator, reducing the power dissipation in the device. When the thermal sensor works, a decrease of the output voltage, oscillation, etc. may be observed.

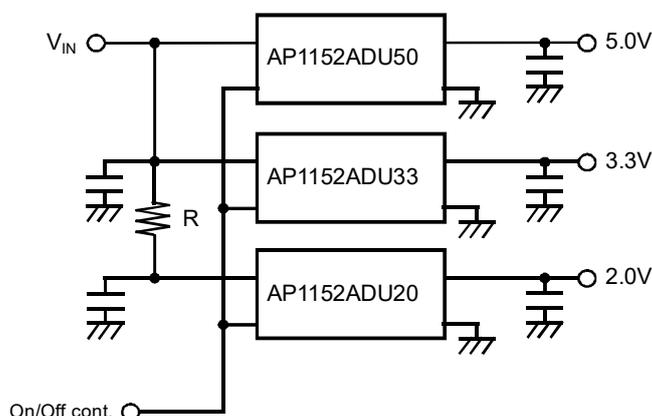


Figure 4. Parallel-Connected On/Off Control

11.6 Noise Pass Terminal

The noise and the ripple rejection characteristics depend on the capacitance on the Np terminal. The ripple rejection characteristic of the low frequency region improves by increasing the capacitance of CNP. A standard value is $C_{NP}=0.1\mu F$. Increase CNP in a design with important output noise and ripple rejection requirements. The IC will not be damaged if the capacitor value is increased. The On/Off switching speed changes depending on the NP terminal capacitance. The switching speed slows when the capacitance is large.

11.7 Notes on output terminal (VOUT) to GND short-circuit evaluation

The resonance phenomenon due to stick to the output terminal CL (C component) and the short-circuit line (L component), the output terminal will become a negative potential. Output terminal parasitic transistor operates in the IC enters the minus side, leads to the worst case burning for packages that latch-up phenomenon occurs in the IC (white smoke) or damage.

The resonance phenomenon appears remarkably In the ESR value is small ceramic capacitors and the like of the capacitor. As a measure of this phenomenon, we can to reduce the resonance phenomenon to be short-circuited by connecting the short-circuit line and the series in more than 2Ω resistance. This allows you to prevent latch-up phenomenon in the IC.

In large tantalum and electrolytic capacitor of ESR, it generally influence of there resonance phenomenon ESR value is greater than or equal to 2Ω is reduced. Also, if a constraint or the like on your set can not be performed the measures as described above, please insert a schottky diode between

GND terminal and the output terminal. This parasitic transistor in the internal IC will not work. A result, you can avoid the latch-up because the parasitic transistor does not work.

11.8 Thermal Resistance and Power Dissipation

•How to determine the thermal resistance when mounted on PCB

The thermal resistance when mounted is expressed as follows:

$$T_j = \theta_{JA} \times P_D + 25$$

T_j of IC is set around 150°C. P_D is the value when the thermal sensor is activated. If the ambient temperature is 25°C, then:

$$150 = \theta_{JA} \times P_D + 25$$

$$\theta_{JA} \times P_D + 25 = 150$$

$$\theta_{JA} \times P_D = 125$$

$$\theta_{JA} = \frac{125}{P_D} (\text{°C/W})$$

•Simple method to calculate Power Dissipation(P_D)

Mount the IC on the print circuit board. P_D will be $V_{IN} \times I_{IN}$ when the short circuit on the output side of the IC. The output terminal short-circuited with GND to measure gradually the input current gradually increase the input voltage. Increase gradually to 10V position the input voltage. Initial input current value is the maximum instantaneous output current value, but gradually decreased due to the temperature rise of the chip, it will eventually become a thermal equilibrium state (natural air cooling). This is calculated by using the input current value and the input voltage value when became constant.

$$P_D (\text{mW}) \cong V_{in}(\text{V}) \times I_{in}(\text{mA})$$

•Maximum available current at the maximum temperature流

Available at the time the highest operating temperature current, you can ask in the graph of [Figure 5](#). Than DP_D value obtained from the graph of [Figure 5](#), the maximum available current at the time of the maximum temperature can be calculated by the following equation.

$$I_{out} \cong \left\{ DP_D \div (V_{in,MAX} - V_{out}) \right\}$$

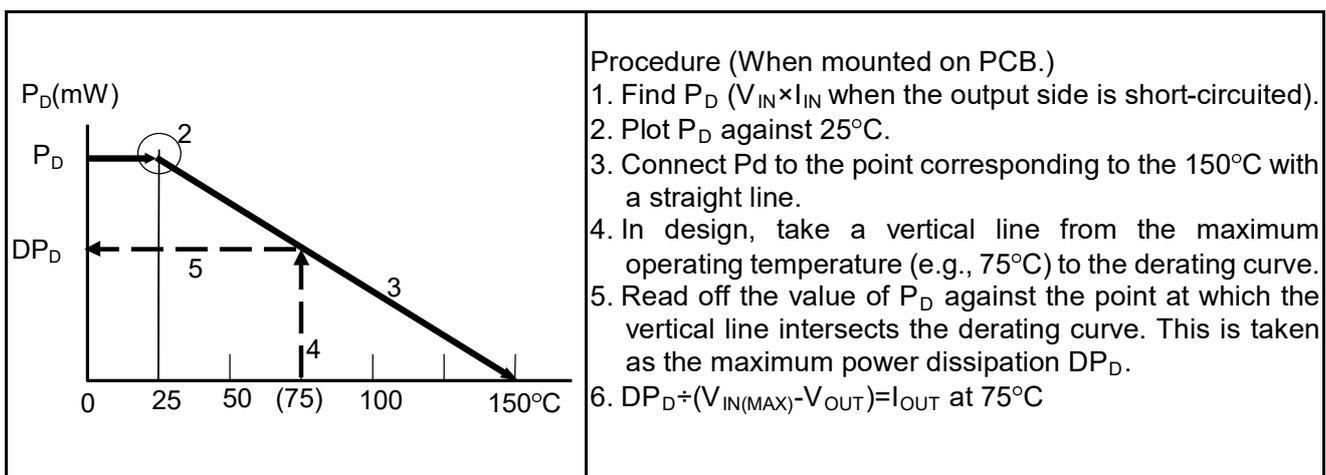


Figure 5. The simple method to calculate P_D

12. Definition of term

■ Characteristics

Each characteristic will be measured in a short period not to be influenced by joint temperature (T_j).

- **Output Voltage (V_{OUT})**

The output voltage is specified with $V_{IN}=(V_{OUT(TYP)}+1V)$ and $I_{OUT}=5mA$.

- **Output Current (I_{OUT})**

Normal output current that can be used. And a range of overheat protection does not operation.

- **Maximum Output Current ($I_{OUT(MAX)}$)**

The rated output current is specified under the condition where the output voltage drops 0.3V the value specified with $I_{OUT}=5mA$. The input voltage is set to $V_{OUT(TYP)}+1V$ and the current is pulsed to minimize temperature effect.

- **Dropout Voltage (V_{DROP})**

The dropout voltage is the difference between the input voltage and the output voltage at which point the regulator starts to fall out of regulation. Below this value, the output voltage will fall as the input voltage is reduced. It is dependent upon the load current and the junction temperature.

- **Line Regulation (LinReg)**

Line regulation is the ability of the regulator to maintain a constant output voltage as the input voltage changes. The line regulation is specified as the input voltage is changed from $V_{IN}=V_{OUT(TYP)}+1V$ to $V_{OUT(TYP)}+6V$. It is a pulse measurement to minimize temperature effect.

- **Load Regulation (LoaReg)**

Load regulation is the ability of the regulator to maintain a constant output voltage as the load current changes. It is a pulsed measurement to minimize temperature effects with the input voltage set to $V_{IN}=V_{OUT(TYP)}+1V$. The load regulation is specified output current step conditions of 5mA to 100mA.

- **Ripple Rejection (R.R)**

Ripple rejection is the ability of the regulator to attenuate the ripple content of the input voltage at the output. It is specified with 200mVrms, 1kHz super-imposed on the input voltage, where $V_{IN}=V_{OUT}+1.5V$. Ripple rejection is the ratio of the ripple content of the output vs. input and is expressed in dB.

- **Standby Current ($I_{STANDBY}$)**

Standby current is the current, which flows into the regulator when the output is turned off by the control function ($V_{CONT}=0V$).

■ Protections

- **Over Current Protection**

The over current sensor protects the device when there is excessive output current. It also protects the device if the output is accidentally connected to ground.

- **Thermal Shutdown Protection**

When the power loss of the regulator there are many, it is the ability to limit such that does not exceed the allowable power consumption. Output and the chip temperature reaches about 150°C is turned OFF. However, when the temperature of the chip is reduced, and the output is turned ON again.

13. Recommended External Circuit

■ Recommended External Circuit

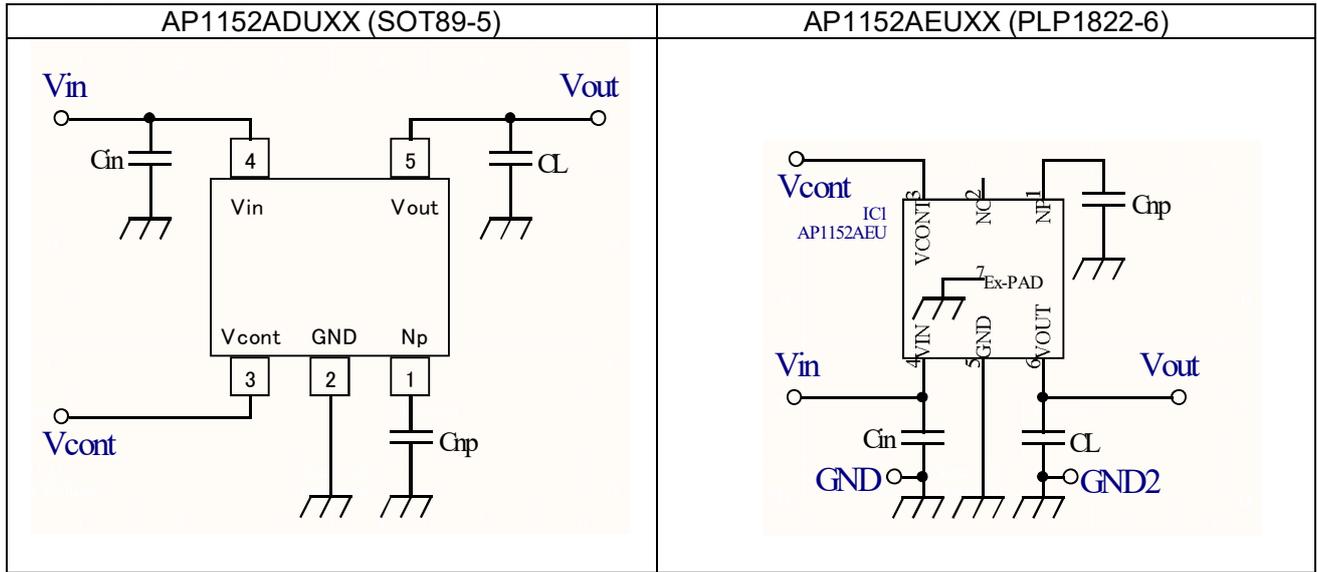


Figure 6. External connection circuit example

Table 5. Recommended external components example

| Parts | min | typ | max | Umit | 備考 |
|----------|-----|-------|-----|---------|----|
| C_{IN} | - | 1.0 | - | μF | |
| C_L | - | 1.0 | - | μF | |
| C_{NP} | - | 0.001 | - | μF | |

Note 7. The above table of values is the recommended example. Please apply the optimal value on the check prior to the time of your on your board.

■ Recommended Layout

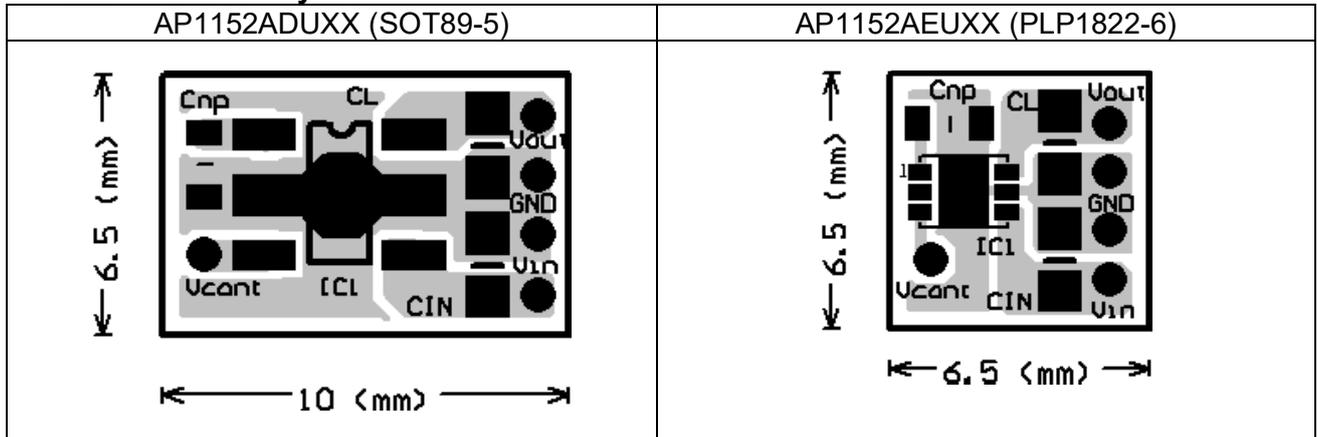
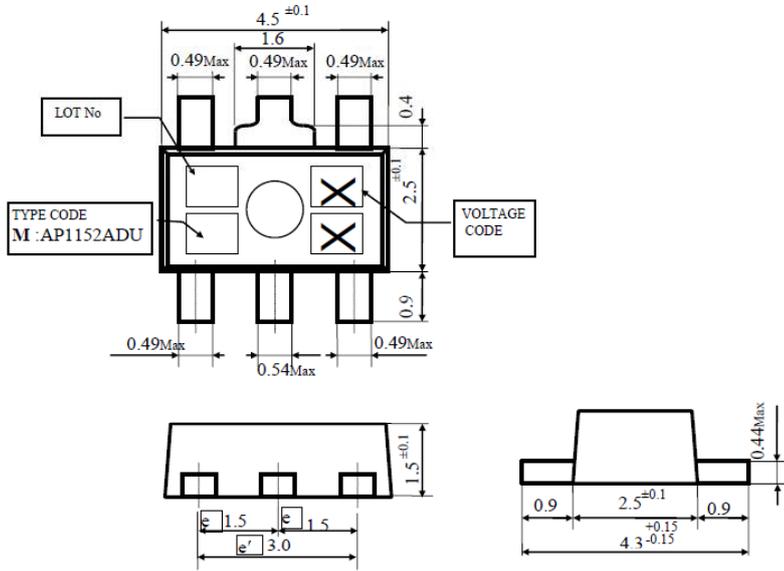


Figure 7. Layout pattern example

- ① Place the input capacitor C_{IN} as close as possible to the V_{IN} and GND.
- ② Place the output capacitor C_L as close as possible to the V_{OUT} and GND.
- ③ PCB wiring, so as to strengthen the GND area.
- ④ PLP1822-6 of Exposed-Pad has become a shared with the ground of the IC. Please connect to the PCB ground always. Vias (heat dissipation hole) is an effective heat dissipation to the PCB of each layer.

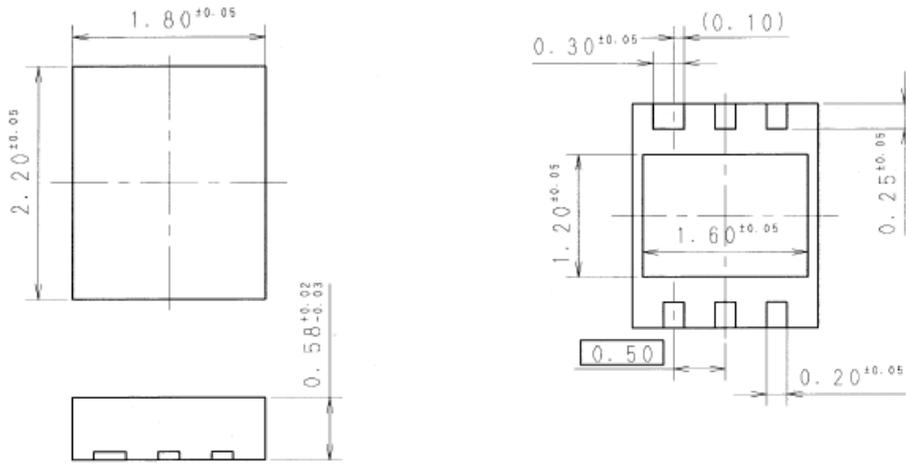
14. Package

■ Outline Dimensions
 • SOT89-5

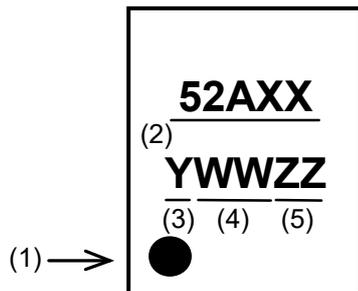


Unit : mm
 General tolerance : ±0.2

• PLP1822-6



Unit : mm



- (1) 1pin Indication
- (2) Market No. (XX:Output Voltage code)
- (3) Year code (last 1 digit)
- (4) Week code
- (5) Management code

| |
|---------------------------|
| 15. Revise History |
|---------------------------|

| Date (YY/MM/DD) | Revision | Page | Contents |
|--------------------|----------|------|--|
| 14/10/29 | 00 | - | First Edition |
| 14/12/05 | 01 | 24 | Changed horizontal width dimension tolerance of the package ; 4.5 ± 0.2 to 4.5 ± 0.1 Changed vertical width dimension tolerance of the package ; 2.5 ± 0.2 to 2.5 ± 0.1 (without pin length) Changed vertical width dimension tolerance of the package ; $4.5+0.5/-0.3$ to $4.3+0.15/-0.15$ (with pin length) Changed height dimension tolerance of the package ; 1.5 ± 0.2 to 1.5 ± 0.1 Changed pin length ; $1.0 \rightarrow 0.9$ Add General tolerance : ± 0.2 |
| 17/3/24 | 01 | - | Completely revised as PLP 1822-6 package is added |

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