HEF40240B

Octal inverting buffers with 3-state outputs

Rev. 5 — 15 November 2011 **Product data sheet**

1. General description

The HEF40240B is an octal inverting buffer with 3-state outputs. It features output stages with high current output capability suitable for driving highly capacitive loads.

The 3-state outputs are controlled by the output enable inputs $n\overline{OE}$. A HIGH on $n\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity. Schmitt-trigger action makes the inputs highly tolerant to slow input rise and fall times.

The HEF40240B is pin and functionally compatible with the TTL '240' device.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Tolerant of slow input rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from –40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from –40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
HEF40240BP	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
HEF40240BT	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Functional diagram

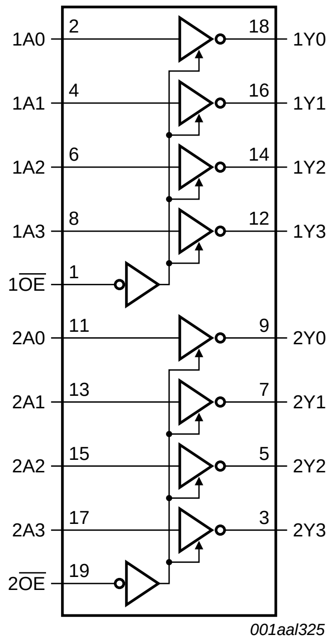


Fig 1. Functional diagram

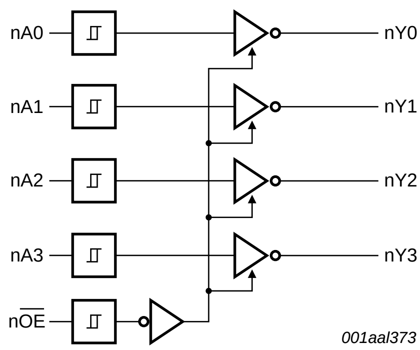


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

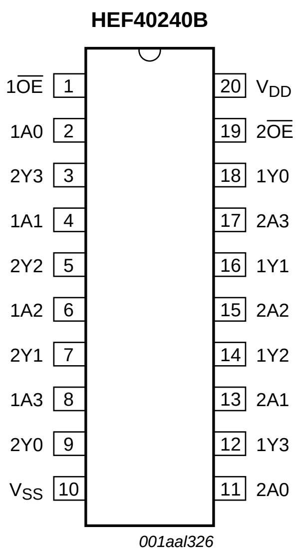


Fig 3. Pin configuration DIP20

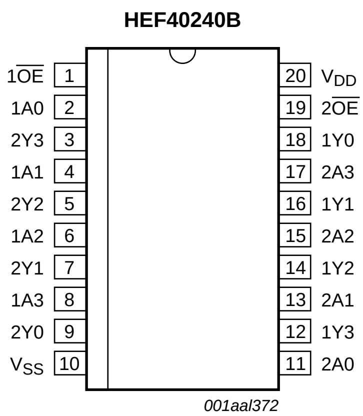


Fig 4. Pin configuration SO20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
V_{SS}	10	ground (0 V)
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
V_{DD}	20	supply voltage
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
$2\overline{OE}$	19	output enable input (active LOW)

6. Functional description

Table 3. Function table[1]

Inputs		Output
nAn	**$n\overline{OE}$**	**nYn**
H	L	L
L	L	H
X	H	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			–0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
I_I	input leakage current	into any input		-	±10	mA
I_O	output current	sink or source current	[1]	-	±25	mA
I_{DD}	supply current	to any supply terminal		-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C				
		DIP20 package	[2]	-	750	mW
		SO20 package	[3]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] See Figure 6.

[2] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] For SO20 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

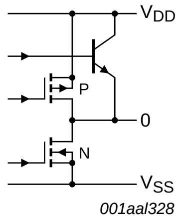
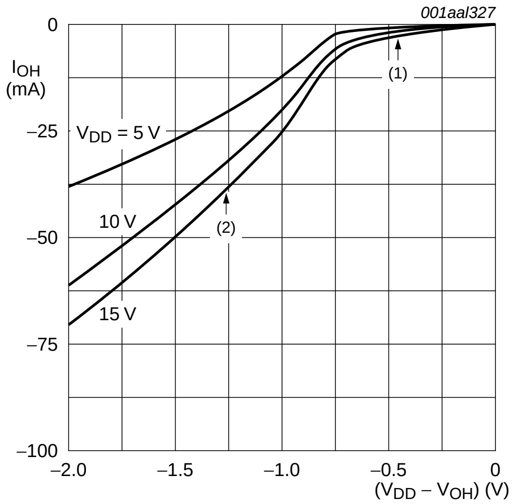


Fig 5. Schematic diagram of a buffer output stage



(1) P-channel MOS transistor conducting.

(2) P-channel MOS transistor and bipolar NPN transistor conducting.

Fig 6. Typical output source current characteristic

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_H	hysteresis voltage	for any input	5 V	-	-	-	220.0	-	-	mV
			10 V	-	-	-	250.0	-	-	mV
			15 V	-	-	-	320.0	-	-	mV
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 3.6 V	5 V	-	−9.3	−24.0	−10.0	-	−10.7	mA
		V_O = 8.4 V	10 V	-	−14.4	−46.0	−15.0	-	−15.0	mA
		V_O = 13.2 V	15 V	-	−19.5	−62.0	−20.0	-	−19.8	mA
		V_O = 4.6 V	5 V	-	−0.75	−1.2	−0.6	-	−0.45	mA
		V_O = 9.5 V	10 V	-	−1.85	−3.0	−1.5	-	−1.1	mA
		V_O = 13.5 V	15 V	-	−14.5	−50.0	−15.0	-	−15.5	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	2.9	-	2.3	5.4	1.75	-	mA
		V_O = 0.5 V	10 V	9.5	-	7.6	17.0	5.50	-	mA
		V_O = 1.5 V	15 V	30.0	-	25.0	45.0	19.0	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{DD}	supply current	I_O = 0 A	5 V	-	4	-	4	-	30	μA
			10 V	-	8	-	8	-	60	μA
			15 V	-	16	-	16	-	120	μA
I_{OZ}	OFF-state output current		15 V	-	1.6	-	1.6	-	12	μA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

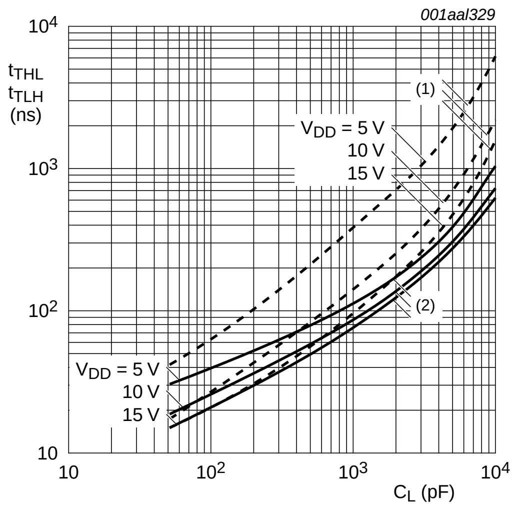
10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 10; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Figure 8	5 V	[1]	83 ns + (0.24 ns/pF)C_L	-	95	190	ns
			10 V		35 ns + (0.10 ns/pF)C_L	-	40	80	ns
			15 V		26 ns + (0.07 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Figure 8	5 V	[1]	82 ns + (0.06 ns/pF)C_L	-	85	170	ns
			10 V		38 ns + (0.03 ns/pF)C_L	-	40	80	ns
			15 V		29 ns + (0.02 ns/pF)C_L	-	30	60	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nYn; nYn is HIGH; see Figure 9	5 V			-	70	140	ns
			10 V			-	35	70	ns
			15 V			-	30	60	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nYn; nYn is LOW; see Figure 9	5 V			-	75	150	ns
			10 V			-	40	80	ns
			15 V			-	30	60	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn; nYn goes HIGH; see Figure 9	5 V			-	80	160	ns
			10 V			-	35	70	ns
			15 V			-	30	60	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn; nYn goes LOW; see Figure 9	5 V			-	90	180	ns
			10 V			-	40	80	ns
			15 V			-	30	60	ns
t_{THL}	HIGH to LOW output transition time	see Figure 7 and Figure 8	5 V			-	40	80	ns
			10 V			-	20	40	ns
			15 V			-	15	30	ns
t_{TLH}	LOW to HIGH output transition time	see Figure 7 and Figure 8	5 V			-	30	60	ns
			10 V			-	20	40	ns
			15 V			-	15	30	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).



(1) t_{THL}.

(2) t_{TLH}.

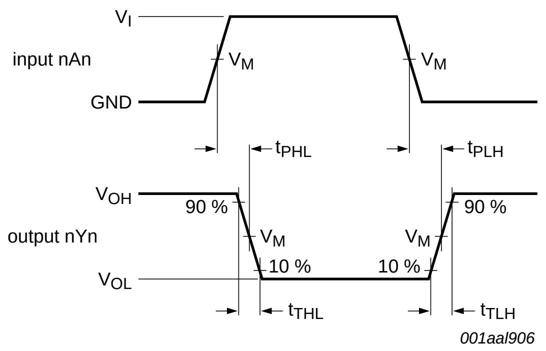
Fig 7. Output transition times as a function of the load capacitance

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

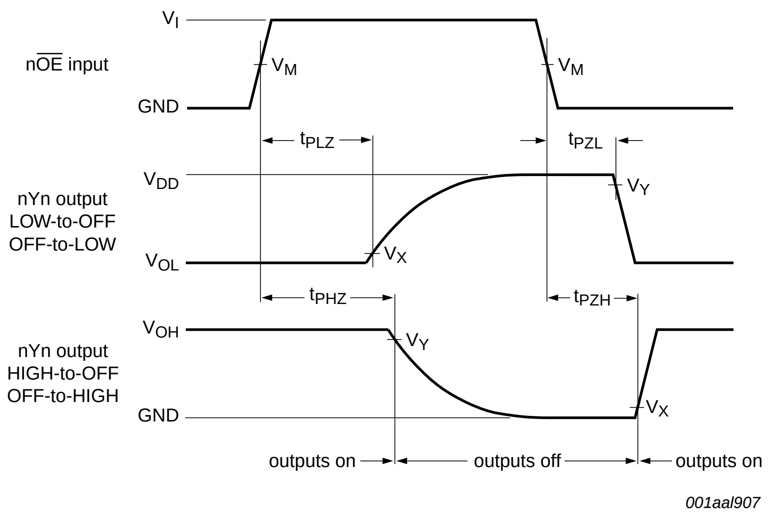
Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 4250 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 17000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 46000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms



Measurement points are given in Table 9, V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. Waveforms showing propagation and transition delays

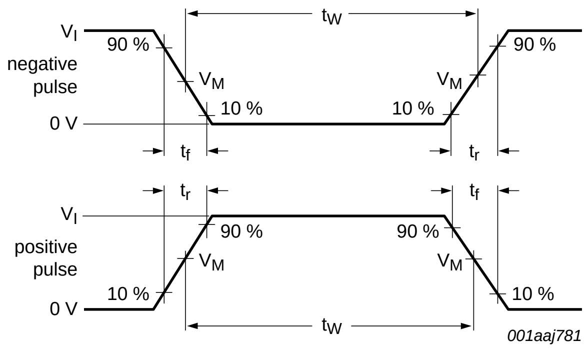


Measurement points are given in Table 9, V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

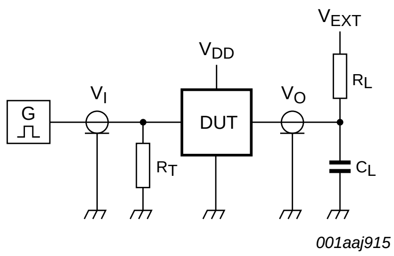
Fig 9. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



a. Input waveforms



b. Test circuit

For test data see Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

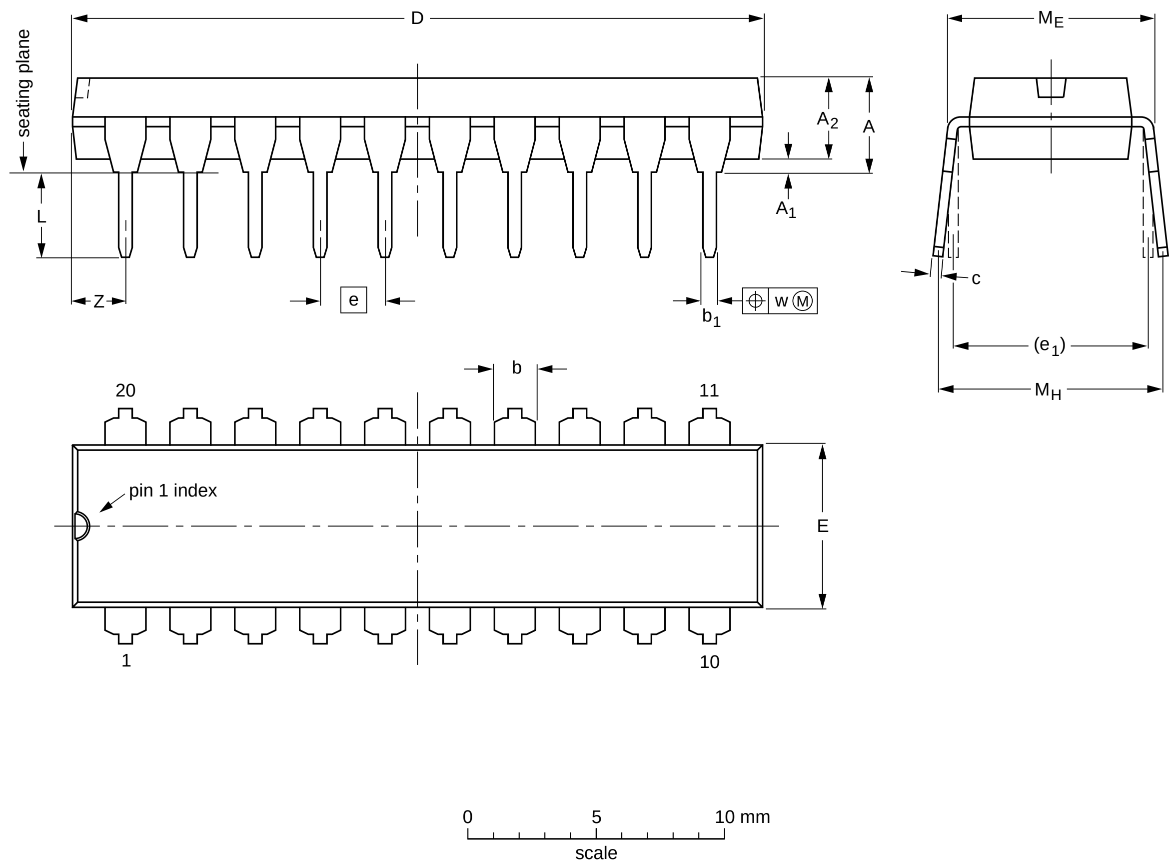
Fig 10. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{DD}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF	1 kΩ	open	V_{DD}	GND

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D [(1)]	E [(1)]	e	e_1	L	M_E	M_H	w	Z [(1)] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

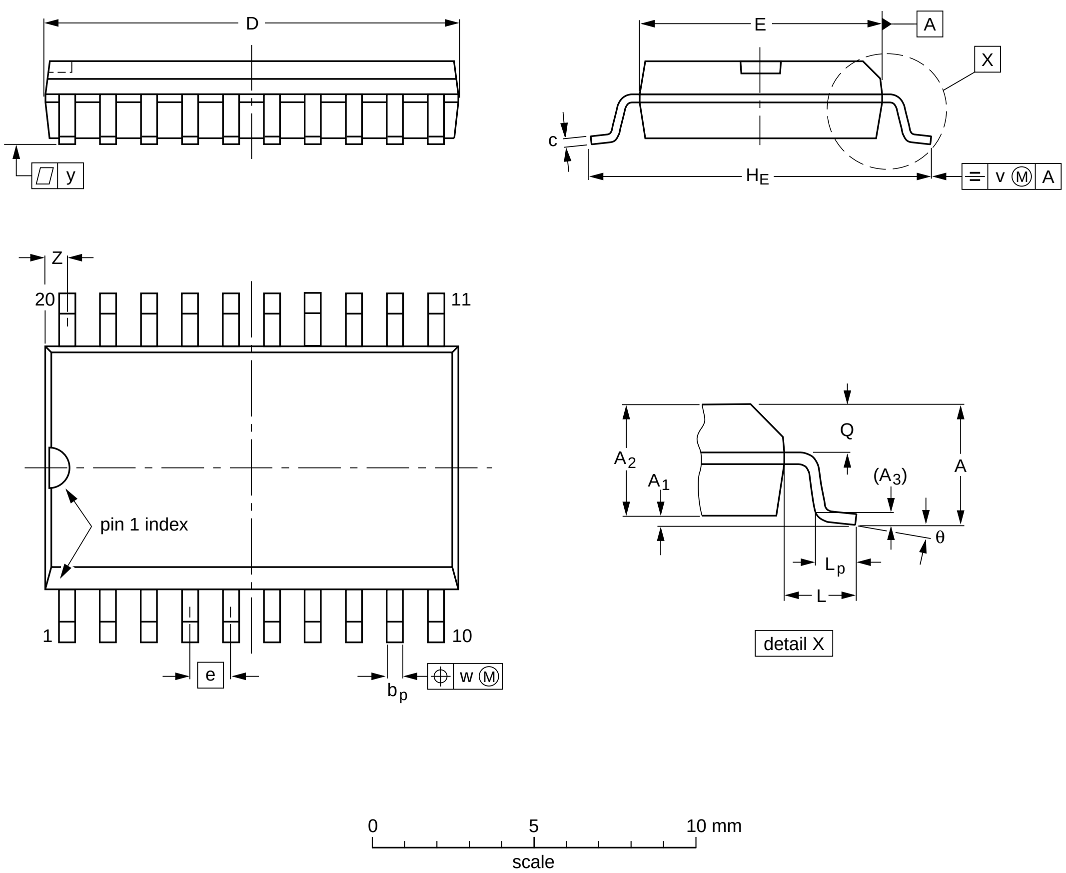
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 11. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT163-1 (SO20)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
DUT	Device Under Test
MOS	Metal Oxide Semiconductor
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40240B v.5	20111115	Product data sheet	-	HEF40240B v.4
Modifications:	• Section Applications removed • Table 6: I_{OH} minimum values changed to maximum			
HEF40240B v.4	20100420	Product data sheet	-	HEF40240B_CNV v.3
HEF40240B_CNV v.3	19950101	Product specification	-	HEF40240B_CNV v.2
HEF40240B_CNV v.2	19950101	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

17. Contents

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