CBTV24DD12

12-bit bus switch/multiplexer for DDR4-DDR3-DDR2 applications

Rev. 3.2 — 19 April 2016 Product data sheet

1. General description

CBTV24DD12 is designed for 1.8 V/2.5 V/3.3 V supply voltage operation and it supports Pseudo Open Drain (POD), SSTL_12, SSTL_15 or SSTL_18 signaling and CMOS select input levels. This device is designed for operation in DDR4, DDR3 or DDR2 memory bus systems, with speeds up to 3200 MT/s.

The CBTV24DD12 has a 1 : 2 switch or 2 : 1 multiplex topology and offers a 12-bit wide bus. Each 12-bit wide A-port can be switched to one of two ports B and C, for all bits simultaneously. Each port is non-directional due to the use of FET switches, allowing a multitude of applications requiring high-bandwidth switching or multiplexing.

The selection of the port is by a simple CMOS input (SELect). Another CMOS input ($\overline{\text{EN}}$able) is available to allow all ports to be disconnected. The SEL0, SEL1 and $\overline{\text{EN}}$ input signals are designed to operate transparently as CMOS input level signals up to 3.3 V.

CBTV24DD12 uses NXP’s proprietary high-speed switch architecture providing high bandwidth, very little insertion loss, return loss, and very low propagation delay, allowing use in many applications requiring switching or multiplexing of high-speed signals. It is available in a 3.0 mm × 8.0 mm TFBGA48 package with 0.65 mm ball pitch, for optimal size versus board layout density considerations. It is characterized for operation from –10 °C to +85 °C.

2. Features and benefits

2.1 Topology

- 12-bit bus width
- 1 : 2 switch/MUX topology
- Bidirectional operation
- Simple CMOS select pins (SEL0, SEL1)
- Simple CMOS enable pin ($\overline{\text{EN}}$)

2.2 Performance

- 3200 MT/s throughput
- 7.4 GHz bandwidth (for both single-ended and differential signals)
- Low ON insertion loss
- Low return loss
- Low crosstalk
- High OFF isolation

- POD_12, SSTL_12, SSTL_15 or SSTL_18 signaling
- Low R_{ON} (8 Ω typical)
- Low ΔR_{ON} (<1 Ω)

2.3 General attributes

- 1.8 V/2.5 V/3.3 V supply voltage operation
- Very low supply current (600 μA typical)
- Back current protection on all the I/O pins of these switches
- ESD robustness exceeds 2.5 kV HBM, 1 kV CDM
- Available in TFBGA48 package, 3.0 mm × 8.0 mm × 1 mm size, 0.65 mm pitch, Pb-free/Dark Green

3. Applications

- DDR4/DDR3/DDR2 memory bus systems
- NVDIMM module
- Systems requiring high-speed multiplexing
- Flash memory array subsystem

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
CBTV24DD12ET	V2412	TFBGA48	plastic low profile fine-pitch ball grid array package; 48 balls; body 3 × 8 × 1 mm; 0.65 mm pitch	SOT1365-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
CBTV24DD12ET	CBTV24DD12ETY	TFBGA48	Reel 13” Q1/T1 *Standard mark SMD dry pack	4500	T_{amb} = −10 °C to +85 °C

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5. Functional diagram

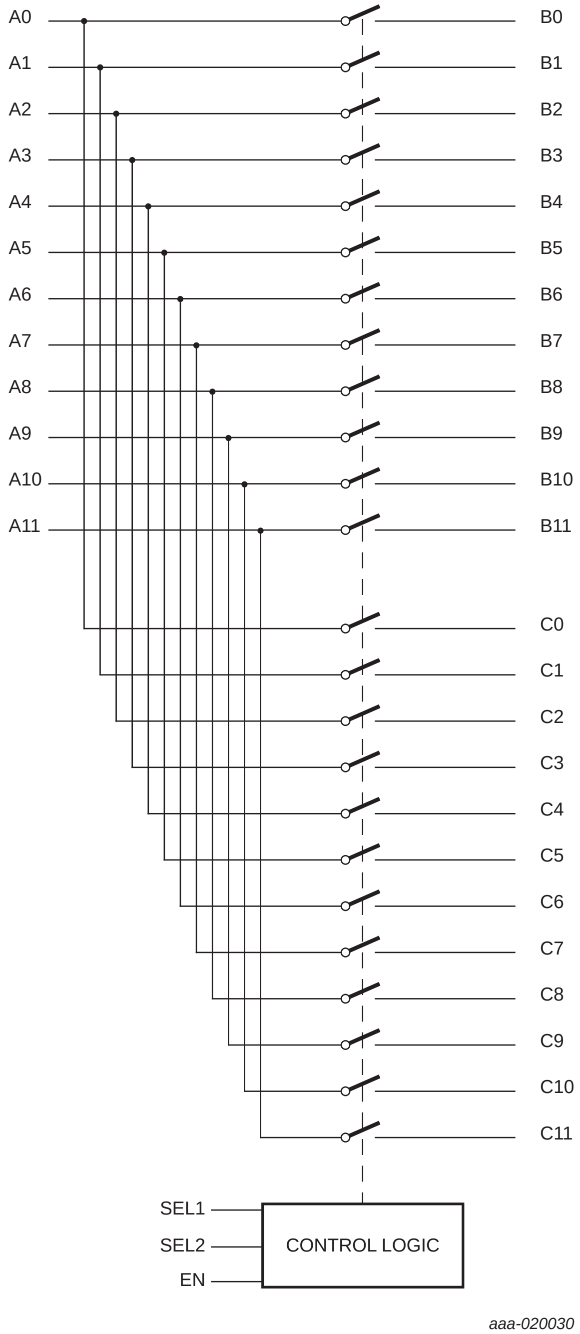

Fig 1. Functional diagram

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6. Pinning information

6.1 Pinning

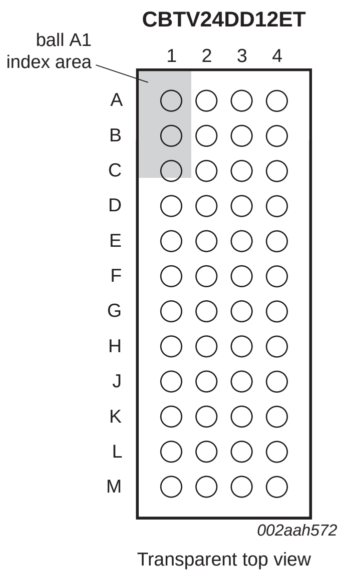

Fig 2. Pin configuration for TFBGA48

	1	2	3	4
A	A0	SEL0	B0	C0
B	A1	GND	B1	C1
C	A2	V_{DD}	B2	C2
D	A3	GND	B3	C3
E	A4	GND	B4	C4
F	A5	GND	B5	C5
G	A6	V_{DD}	B6	C6
H	A7	$\overline{EN}$	B7	C7
J	A8	GND	B8	C8
K	A9	V_{DD}	B9	C9
L	A10	GND	B10	C10
M	A11	SEL1	B11	C11

Transparent top view

002aah573

Fig 3. Ball mapping for TFBGA48

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
A[0:11]	A1, B1, C1, D1, E1, F1, G1, H1, J1, K1, L1, M1	high-speed I/O	12-bit wide input/output, port A
B[0:11]	A3, B3, C3, D3, E3, F3, G3, H3, J3, K3, L3, M3	high-speed I/O	12-bit wide input/output, port B
C[0:11]	A4, B4, C4, D4, E4, F4, G4, H4, J4, K4, L4, M4	high-speed I/O	12-bit wide input/output, port C
SEL0, SEL1	A2, M2	CMOS input	CMOS input signal. When SEL0 = LOW, port A[0,1,4,5,8,9] and port B[0,1,4,5,8,9] are mutually connected. When SEL0 = HIGH, port A[0,1,4,5,8,9] and port C[0,1,4,5,8,9] are mutually connected. When SEL1 = LOW, port A[2,3,6,7,10,11] and port B[2,3,6,7,10,11] are mutually connected. When SEL1 = HIGH, port A[2,3,6,7,10,11] and port C[2,3,6,7,10,11] are mutually connected.

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Table 3. Pin description *...continued*

Symbol	Pin	Type	Description
$\overline{EN}$	H2	CMOS input	CMOS input signal. When HIGH, all ports are mutually isolated. When LOW, connection is set using the SEL[0:1] input signals.
V_{DD}	C2, G2, K2	supply	Must be connected to supply voltage power plane.
GND	B2, D2, E2, F2, J2, L2	ground	Must be connected to GND plane for both electrical grounding and thermal relief.

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7. Functional description

Refer to Figure 1 “Functional diagram”.

CBTV24DD12 supports 1.8 V, 2.5 V or 3.3 V power supply voltages. All signal paths are implemented using high-bandwidth pass-gate technology and are non-directional. No clock or reset signal is needed for the multiplexer to function. The switch position for the channels is selected using the select signals (SEL0, SEL1). The detailed operation is described in Section 7.1.

7.1 Function selection

The internal multiplexer switch position is controlled by three logic inputs, SEL0, SEL1 and $\overline{EN}$, as described in Table 4.

When a channel is not being used, Port B and Port C of this channel should be tied to ground. For example, if Channel 2 is not used, B2 and C2 should be tied to ground and A2 should be left open.

Table 4. Function selection

X = don’t care.

Inputs		Switch position	
$\overline{EN}$	SELx	A ↔ B	A ↔ C
HIGH	X	OFF (isolated)	OFF (isolated)
LOW	SEL0 = LOW	A[0,1,4,5,8,9] ↔ B[0,1,4,5,8,9]	OFF (isolated)
LOW	SEL0 = HIGH	OFF (isolated)	A[0,1,4,5,8,9] ↔ C[0,1,4,5,8,9]
LOW	SEL1 = LOW	A[2,3,6,7,10,11] ↔ B[2,3,6,7,10,11]	OFF (isolated)
LOW	SEL1 = HIGH	OFF (isolated)	A[2,3,6,7,10,11] ↔ C[2,3,6,7,10,11]

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.3	+4.4	V
T_{stg}	storage temperature		–65	+150	°C
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	2500	V
		CDM [2]	-	1000	V

[1] Human Body Model: ANSI/ESDA/JEDEC JDS-001-2012 (Revision of ANSI/ESDA/JEDEC JS-001-2011), ESDA/JEDEC Joint standard for ESD sensitivity testing. Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.; JEDEC Solid State Technology Association, Arlington, VA, USA.

[2] Charged-Device Model: JESD22-C101E December 2009 (Revision of JESD22-C101D, October 2008), standard for ESD sensitivity testing, Charged-Device Model - Component level; JEDEC Solid State Technology Association, Arlington, VA, USA.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		1.62	-	3.63	V
V_I	input voltage	channel inputs/outputs	–0.3	-	+1.8	V
		control inputs	–0.3	-	+3.6	V
T_{amb}	ambient temperature	operating in free air	–10	-	+85	°C

10. Static characteristics

Table 7. Static characteristics

Typical V_{DD}; T_{amb} = –10 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{DD}	supply current	$\overline{EN}$ = LOW	-	0.6	1.3	mA
		$\overline{EN}$ = HIGH	-	-	45	μA
I_{IH}	HIGH-level input current	High-speed I/O; A, B and C ports; V_I = 1.8 V	-	-	±5	μA
		Control pins; SEL0, SEL1 and EN; V_I = 3.6 V	-	-	±10	μA
I_{IL}	LOW-level input current	V_I = GND	-	-	±5	μA
V_{IH}	HIGH-level input voltage	SEL0, SEL1, $\overline{EN}$ pins	1.4	-	-	V
V_{IL}	LOW-level input voltage	SEL0, SEL1, $\overline{EN}$ pins	–0.5	-	+0.4	V
V_{IK}	input clamping voltage	voltage on high-speed channel pins; I_I = –18 mA	-	-	–1.2	V

[1] Typical values are at V_{DD} = 2.5 V; T_{amb} = 25 °C, and maximum loading.

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11. Dynamic characteristics

Table 8. Dynamic characteristics for CBTV24DD12

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{startup}$	start-up time	supply voltage valid or $\overline{EN}$ going HIGH to channel specified operating characteristics		-	90	300	µs
t_{rcfg}	reconfiguration time	SEL[0:1] state change to channel specified operating characteristics; measuring from 50 % of SELx to 90 % of channel output	[1]	-	-	30	ns
α_{il}	insertion loss	channel is on; 0 Hz ≤ f ≤ 4 GHz		-	–1.5	-	dB
		channel is on; f = 7 GHz		-	–3.0	-	dB
		channel is off; 0 Hz ≤ f ≤ 4 GHz		-	–20	-	dB
RL_{in}	input return loss	channel is on; 0 Hz ≤ f ≤ 4 GHz		-	–16	-	dB
α_{ct}	crosstalk attenuation	adjacent channels are on; 0 Hz ≤ f ≤ 4 GHz		-	–24	-	dB
B	bandwidth	–3.0 dB intercept (for both single-ended and differential signals)		-	7.4	-	GHz
t_{PD}	propagation delay	from A port to B port or C port or vice versa		-	65	-	ps
t_{sk}	skew time	from any output to any output		-	3	6	ps
R_{ON}	ON resistance	from any input to any output		5	6.5	9	Ω
$R_{ON(flat)}$	ON resistance (flatness)		[2]	-	1.5	-	Ω
ΔR_{ON}	ON resistance mismatch between channels		[3][4]	-	0.4	1	Ω

[1] Smooth transition without glitch under DDR termination schemes.

[2] $R_{ON(flat)}$ is the difference of the R_{ON} in a given channel across all V_I voltage ranges.

[3] ΔR_{ON} is the difference of R_{ON} from one port to any other ports when the same V_I voltage is applied to all channels.

[4] Guaranteed by design.

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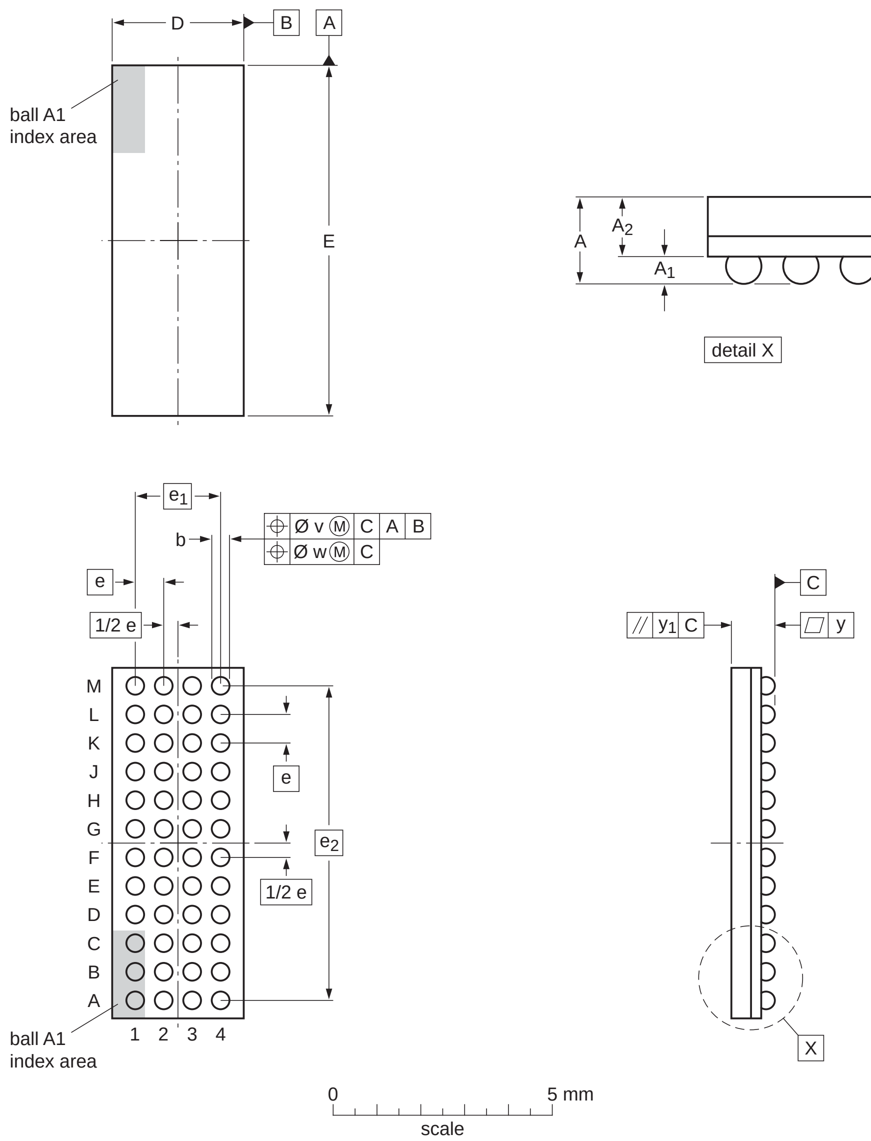
12. Package outline

TFBGA48: plastic low profile fine-pitch ball grid array package; 48 balls **SOT1365-1**



Dimensions

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
	max	1.05	0.35	0.73	0.45	3.1	8.1							
mm	nom	0.98	0.30	0.68	0.40	3.0	8.0	0.65	1.95	7.15	0.15	0.05	0.08	0.1
	min	0.88	0.25	0.63	0.35	2.9	7.9							

sot1365-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1365-1	- - -	- - -	- - -			~~14-01-03~~ 14-08-12

Fig 4. Package outline TFBGA48 (SOT1365-1)

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13. Packing information

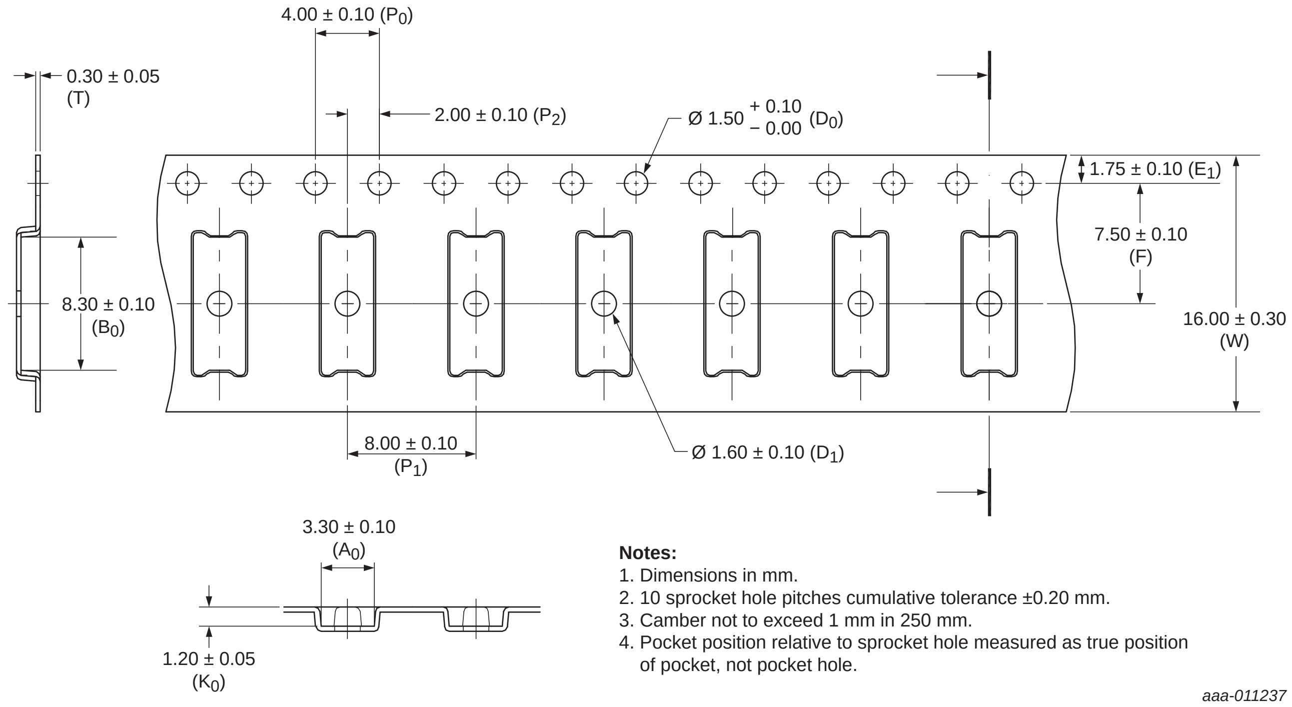
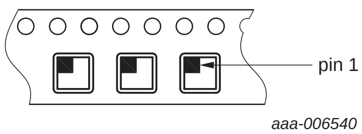


Fig 5. Carrier tape



Pin 1 (ball A1) is in Quadrant 1.

Fig 6. Product orientation in carrier tape

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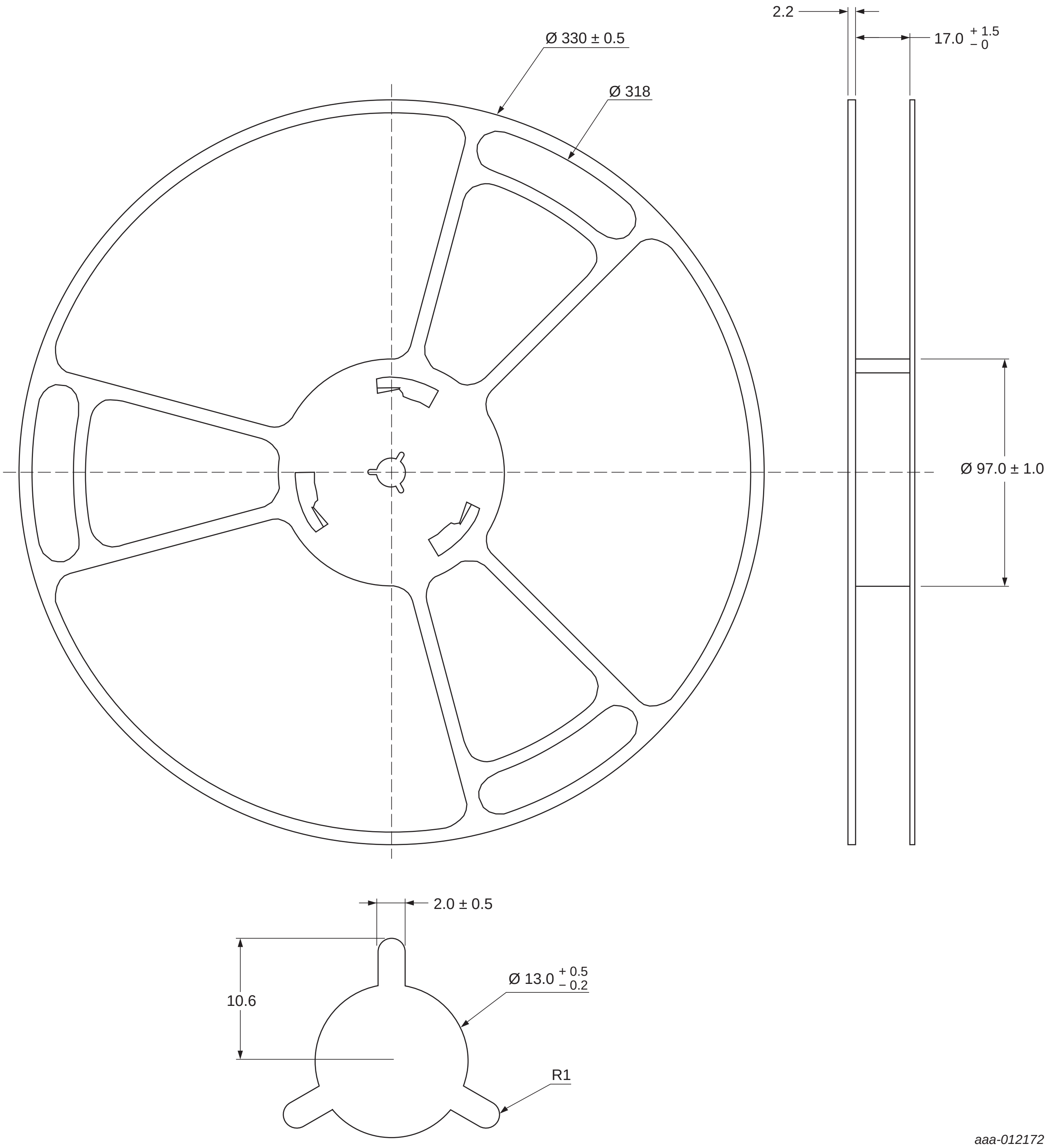

Fig 7. 13-inch reel

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14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.

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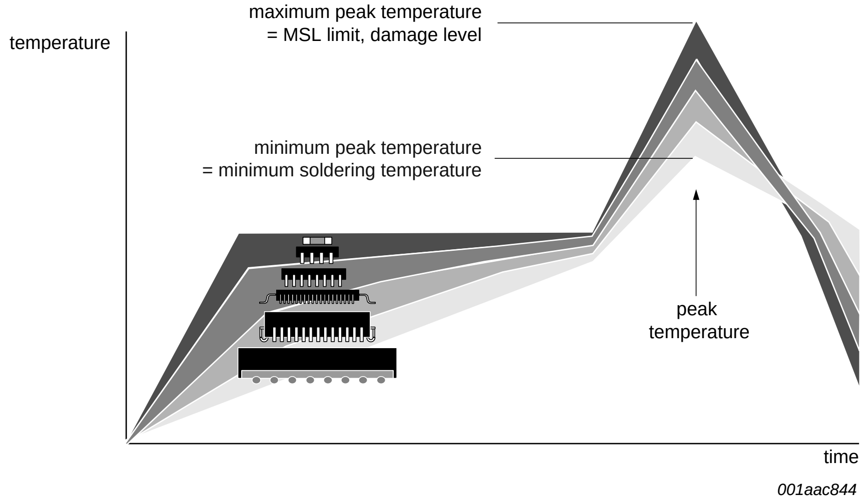

MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

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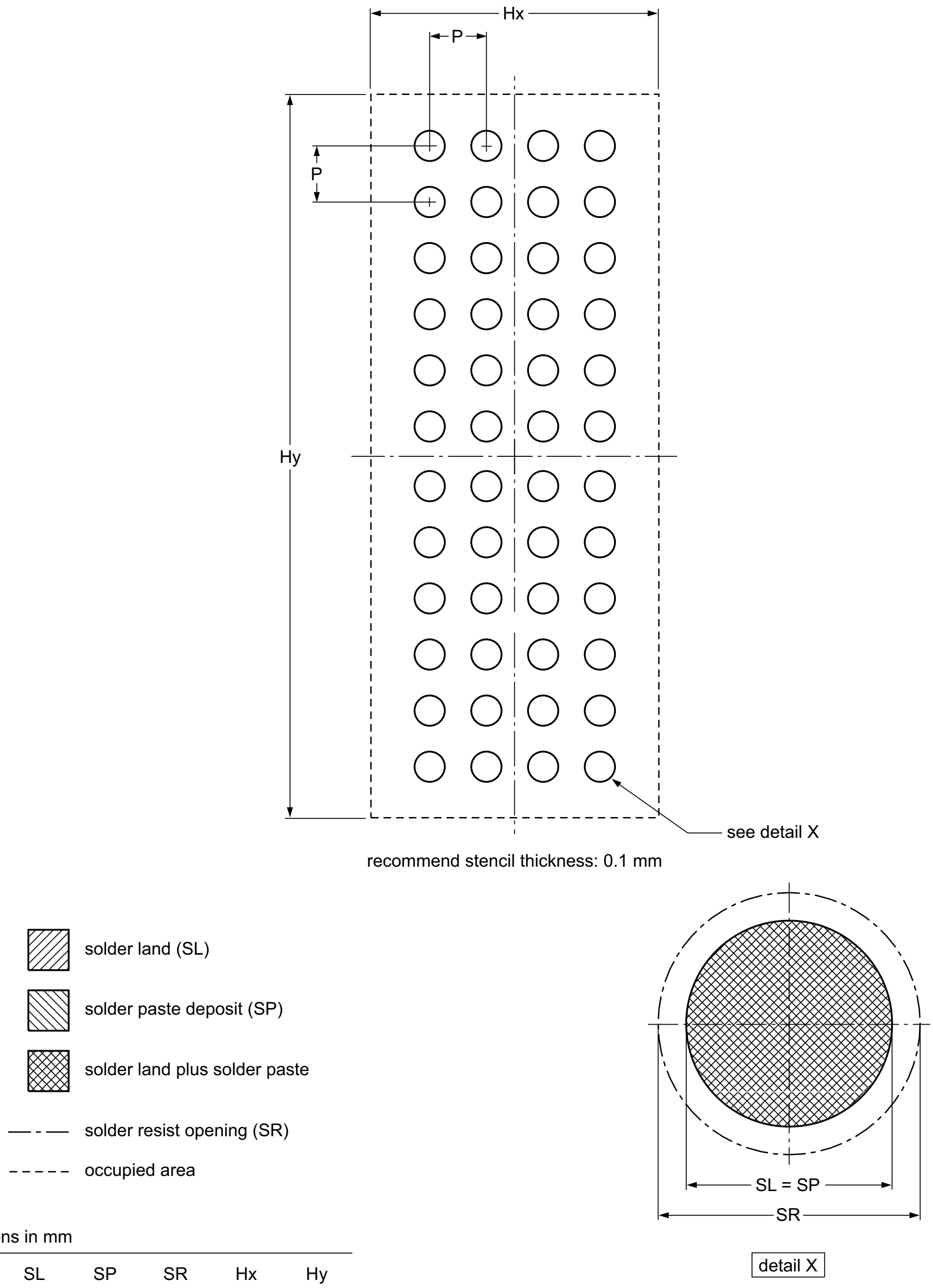
15. Soldering: PCB footprints

Footprint information for reflow soldering of TFBGA48 package **SOT1365-1**



Dimensions in mm

P	SL	SP	SR	Hx	Hy
0.65	0.35	0.35	0.45	3.3	8.3

Issue date ~~14-03-13~~ 14-07-31

sot1365-1_fr

Fig 9. PCB footprint for SOT1365-1 (TFBGA48); reflow soldering

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16. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DDR2	Double Data Rate 2
DDR3	Double Data Rate 3
DDR4	Double Data Rate 4
DRAM	Dynamic Random Access Memory
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
I/O	Input/Output
MT/s	Mega Transfers per second
NVDIMM	Non-Volatile Dual In-line Memory Module
POD	Pseudo Open Drain
SSTL_12	Stub Series Terminated Logic for 1.2 V
SSTL_15	Stub Series Terminated Logic for 1.5 V
SSTL_18	Stub Series Terminated Logic for 1.8 V

17. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTV24DD12 v.3.2	20160419	Product data sheet	-	CBTV24DD12 v.3.1
Modifications:	• Section 2.3 “General attributes”: Added “Back current protection...”			
CBTV24DD12 v.3.1	20151020	Product data sheet	-	CBTV24DD12 v.3
Modifications:	• Updated Figure 1 “Functional diagram”			
CBTV24DD12 v.3	20150820	Product data sheet	-	CBTV24DD12 v.2
Modifications:	• Table 7 “Static characteristics”: Changed max value for I_{IH} control pins from “±5” to “±10” • Table 8 “Dynamic characteristics for CBTV24DD12”: Updated conditions for t_{rcfg}; changed min/typ/max values for R_{ON} • Changed document status from “Company Confidential” to “Company Public”			
CBTV24DD12 v.2	20140828	Product data sheet	-	CBTV24DD12 v.1
CBTV24DD12 v.1	20140814	Product data sheet	-	-

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18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 19 April 2016

Document identifier: CBTV24DD12