Doc No. TT4-EA-13636

Revision. 4

# **Panasonic**

MOS FET

### MTM131270BBF

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### Silicon P-channel MOS FET

### For switching

#### ■ Features

- Low Drain-source On-state Resistance : RDS(on) typ = 92 m $\Omega$  (VGS = -4.0 V)
- Low drive voltage: 1.8 V drive
- Halogen-free / RoHS compliant

(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol :EU

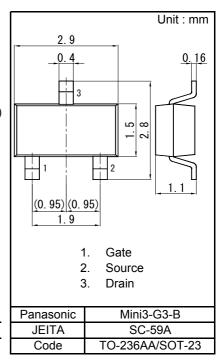
#### ■ Packaging

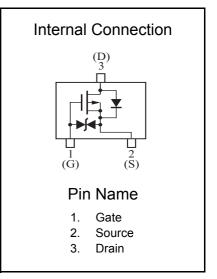
Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Absolute Maximum Ratings Ta - 25	C		
項目	記号	定格	単位
Drain-source Voltage	VDS	-20	V
Gate-source Voltage	VGS	±10	V
Drain current	ID	-2	Α
Peak drain current *1	IDp	-8	Α
Power dissipation *2	PD	700	mW
Channel temperature	Tch	150	°C
Operating ambient temperature	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C

- Note \*1 Pulse width  $\leq$ 10 µs, Duty cycle  $\leq$ 1 %
  - \*2 Measuring on ceramic board at  $40 \times 38 \times 0.1$  mm. Absolute maximum rating PD without heat sink shall be made 200 mW.





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#### ■ Electrical Characteristics Ta = 25 °C ± 3 °C

項目	記号	条件	最小	標準	最大	単位	
Drain-source surrender voltage	VDSS	ID = -1 mA, VGS = 0 V	-20			V	
Drain-source cutoff current	IDSS	VDS = -20 V, VGS = 0 V			-1	^	
Gate-source cutoff current	IGSS	$VGS = \pm 8 \text{ V}, VDS = 0 \text{ V}$			±10	μΑ	
Gate threshold voltage	Vth	ID = -1 mA, VDS = -10 V	-0.4	-0.75	-1.1	V	
	RDS(on)1	ID = -1 A, VGS = -4 V		92	130		
Drain-source ON resistance *1	RDS(on)2	ID = -1 A, VGS = -2.5 V		115	210	mΩ	
	RDS(on)3	ID = -0.5 A, VGS = -1.8 V		161	280		
Forward transfer admittance *1	Yfs	ID = -1 A, VDS = -10 V, f = 1 kHz	3			S	
Short-circuit input capacitance (Common source)	Ciss	VDS = -10 V, VGS = 0 V		300		pF	
Short-circuit output capacitance (Common source)	Coss	f = 1 MHz		30			
Reverse transfer capacitance (Common source)	Crss	1 – 1 IVITIZ		35			
Turn-on Delay Time *2	td(on)	VDD = -10 V, VGS = 0 to -4 V		6			
Rise Time *2	tr	ID = -1 A		8		no	
Turn-off Delay Time *2	td(off)	VDD = -10 V, VGS = -4 to 0 V		57		ns	
Fall Time *2	tf	ID = -1 A		55			

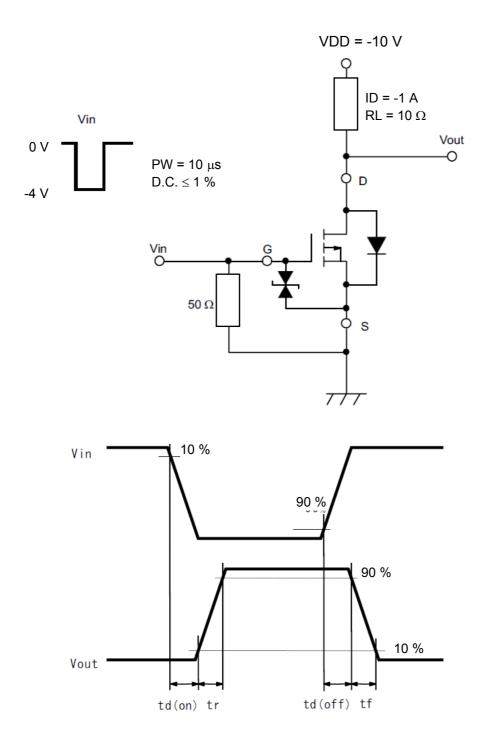
Note: 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

<sup>2. \*1</sup> Pulse test

<sup>\*2</sup> Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

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\*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

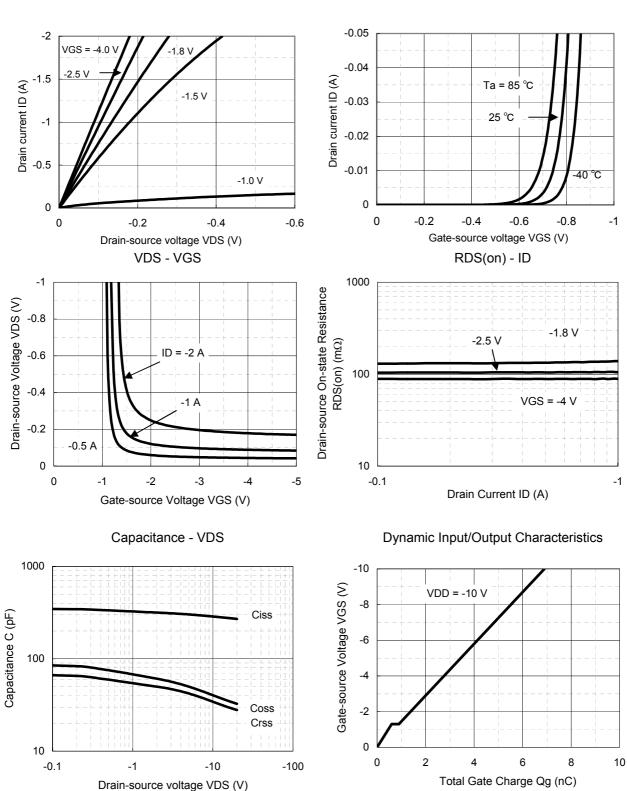


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# Technical Data (reference)

ID - VDS

ID - VGS



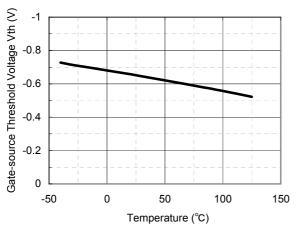
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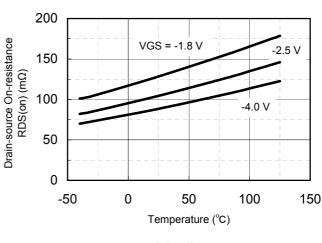
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# Technical Data (reference)

Vth - Ta

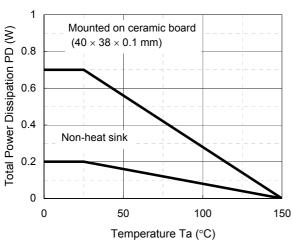
RDS(on) - Ta





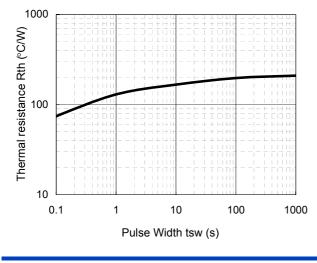
PD - Ta

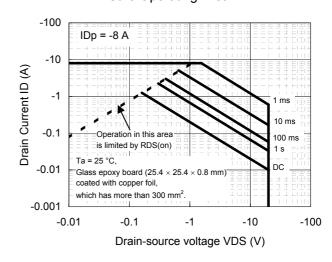
PD - Tc



Rth - tsw

Safe Operating Area

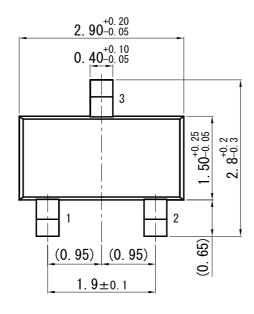


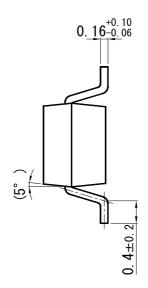


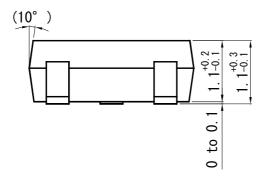
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Mini3-G3-B

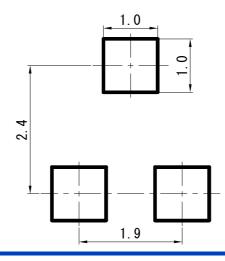
Unit: mm







■ Land Pattern (Reference) (Unit : mm)



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