

Vishay Siliconix

N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)			
	0.0027 at V _{GS} = 4.5 V	34				
12	0.0032 at V _{GS} = 2.5 V	31	33 nC			
	0.0040 at V _{GS} = 1.8 V	28				

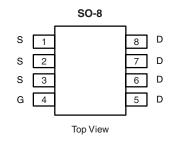
FEATURES

- · Halogen-free
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested

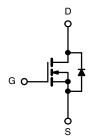


APPLICATIONS

Low V_{IN} DC/DC



Ordering Information: Si4838BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unle	ss otherwise n	oted	
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	12	V	
Gate-Source Voltage		V _{GS}		
	T _C = 25 °C		34	
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	1 .	27	
Continuous Diain Current (1) = 150 C)	T _A = 25 °C	I _D	22.5 ^{b, c}	
	T _A = 70 °C		18.0 ^{b, c}	
Pulsed Drain Current	I _{DM}	70	A	
Continuous Course Drain Diada Current	T _C = 25 °C	I.	5.1	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.2 ^{b, c}	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	20	
Avalanche Energy		E _{AS}	20	mJ
	T _C = 25 °C	P _D	5.7	
Maximum Dawar Dissipation	T _C = 70 °C		3.6	\exists w
Maximum Power Dissipation	T _A = 25 °C	r _D	2.50 ^{b, c}	
	T _A = 70 °C		1.6 ^{b, c}	
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b,d}	t ≤ 10 s	R _{thJA}	39	50	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	18	22	C/ VV	

- a. Based on T_C = 25 °C.
 b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under Steady State conditions is 85 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static		<u>'</u>				I	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	12			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050A		12		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 3.2			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.4		1.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zana Oata Walkana Buain Ouwant	I _{DSS}	V _{DS} = 12 V, V _{GS} = 0 V			1		
Zero Gate Voltage Drain Current		V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	30			Α	
		V _{GS} = 4.5 V, I _D = 15 A		0.0021	0.0027	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 2.5 V, I _D = 12 A		0.0025	0.0032		
	, ,	V _{GS} = 1.8 V, I _D = 10 A		0.0031	0.0040		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		105		S	
Dynamic ^b		<u> </u>				l	
Input Capacitance	C _{iss}			5760		pF	
Output Capacitance	C _{oss}	V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz		1730			
Reverse Transfer Capacitance	C _{rss}			1145			
Tieveree manerer expansion	Q _g	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 10 A		56	84	nC	
Total Gate Charge		30 30 2		33	50		
Gate-Source Charge	Q _{gs}	$V_{DS} = 6 \text{ V}, V_{GS} = 2.5 \text{ V}, I_{D} = 10 \text{ A}$		5.9			
Gate-Drain Charge	Q _{gd}			12.5			
Gate Resistance	R _g	f = 1 MHz	0.2	0.65	1.3	Ω	
Turn-On Delay Time	t _{d(on)}			25	50		
Rise Time	t _r	$V_{DD} = 6 \text{ V}, R_{L} = 0.6 \Omega$		29	55		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		140	240	1	
Fall Time	t _f			35	65		
Turn-On Delay Time	t _{d(on)}			12	24	ns	
Rise Time	t _r	$V_{DD} = 6 \text{ V}, R_{L} = 0.6 \Omega$		13	26	- - -	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$		56	100		
Fall Time	t _f	-		10	20		
Drain-Source Body Diode Characteristi	cs	<u>'</u>					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			5.1	Α	
Pulse Diode Forward Current ^a	I _{SM}				70		
Body Diode Voltage	V_{SD}	I _S = 3 A		0.60	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}			52	100	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	Q_{rr} I _E = 10 A, dl/dt = 100 A/µs, T ₁ = 25 °C		40	80	nC	
Reverse Recovery Fall Time	t _a			21		1	
Reverse Recovery Rise Time	t _b			31		ns	

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

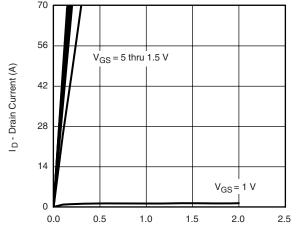
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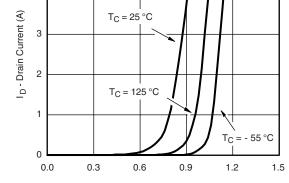


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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

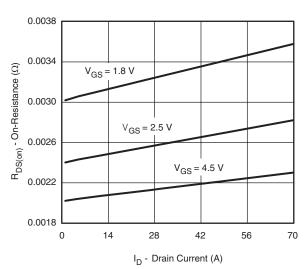


 V_{DS} - Drain-to-Source Voltage (V)

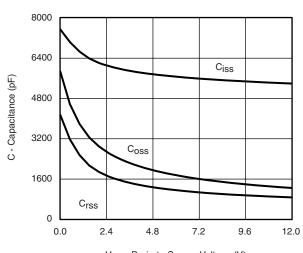


V_{GS} - Gate-to-Source Voltage (V) **Transfer Characteristics**

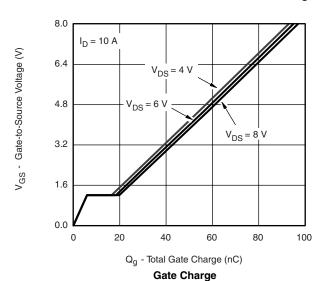
Output Characteristics

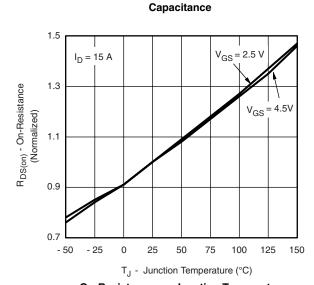


On-Resistance vs. Drain Current and Gate Voltage



 ${\rm V}_{\rm DS}$ - Drain-to-Source Voltage (V)





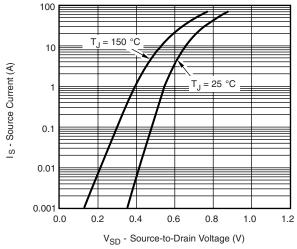
On-Resistance vs. Junction Temperature

Si4838BDY

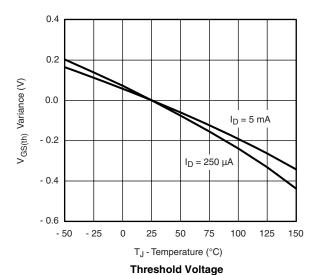
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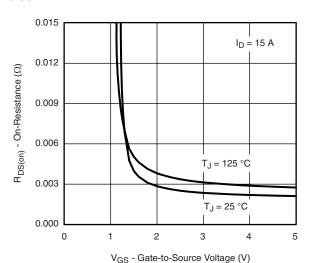
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

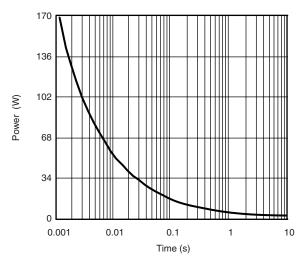


Source-Drain Diode Forward Voltage

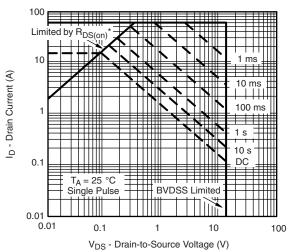




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



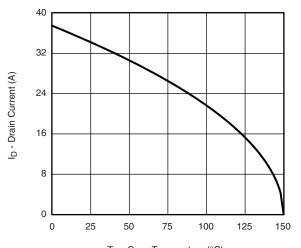
 * V $_{GS}$ > minimum V $_{GS}$ at whicht R $_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



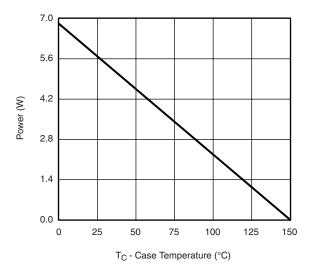
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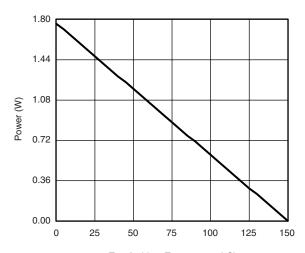
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $T_{\mbox{\scriptsize C}}$ - Case Temperature (°C)

Current Derating*





T_A - Ambient Temperature (°C)

Power, Junction-to-Foot

Power, Junction-to-Ambient

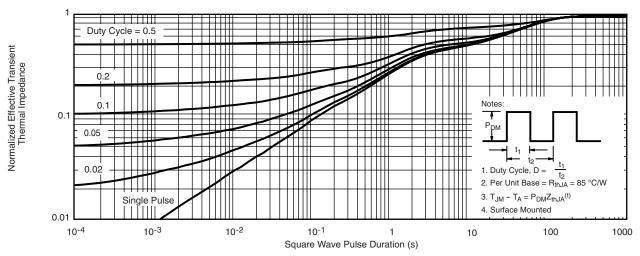
*The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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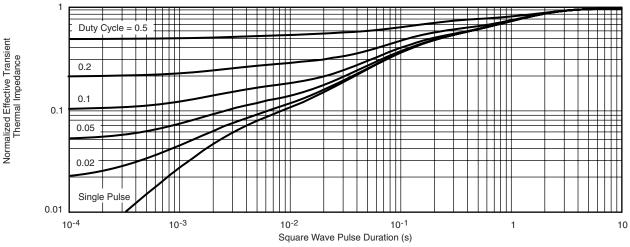
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



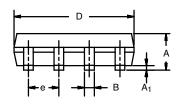
Normalized Thermal Transient Impedance, Junction-to-Foot

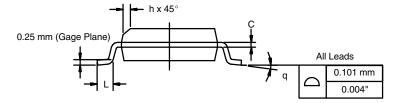
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS INCHES			HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050	0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

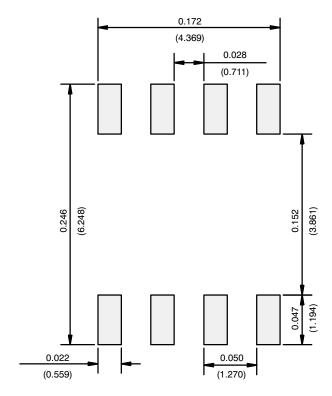
DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

LON NOTE



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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