

9-BIT HOLD REGISTER

SY10E143 SY100E143

# FEATURES

- 700MHz min. operating frequency
- Extended 100E VEE range of -4.2V to -5.5V
- 9 bits wide for byte-parity applications
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75kΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E143
- Available in 28-pin PLCC package

### **BLOCK DIAGRAM**



### DESCRIPTION

The SY10/100E143 are high-speed 9-bit hold registers designed for use in new, high-performance ECL systems. The E143 can hold current data or load new data. The nine inputs, D0-D8, accept parallel input data.

The SEL (Select) control pin serves to determine the mode of operation; either HOLD or LOAD. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK1 or CLK2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E143 is designed for applications requiring highspeed registers, pipeline registers, synchronous operation, and is also suitable for byte-wide parity.

#### PIN NAMES

Pin	Function
D0-D8	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q8	Data Outputs
NC	No Connection
Vcco	Vcc to Output

### PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

# Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E143JC	J28-1	Commercial	SY10E143JC	Sn-Pb
SY10E143JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E143JC	Sn-Pb
SY100E143JC	J28-1	Commercial	SY100E143JC	Sn-Pb
SY100E143JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E143JC	Sn-Pb
SY10E143JZ <sup>(3)</sup>	J28-1	Commercial	SY10E143JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E143JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E143JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E143JZ <sup>(3)</sup>	J28-1	Commercial	SY100E143JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E143JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E143JZ with Pb-Free bar-line indicator	Matte-Sn

#### Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^{\circ}C$ , DC Electricals only.

2. Tape and Reel.

3. Pb-Free package is recommended for new designs.

### TRUTH TABLE

SEL	MODE
L	LOAD
Н	HOLD

# DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		TA = +25°C			TA = +85°C					
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
Ін	Input HIGH Current	—	—	150			150	Ι		150	μΑ	—
IEE	Power Supply Current										mA	
	10E	—	120	145	—	120	145	—	120	145		
	100E	—	120	145	—	120	145	—	138	165		

# **AC ELECTRICAL CHARACTERISTICS**

#### VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		TA = +25°C			TA = +85°C					
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
fmax	Max. Toggle Frequency	700	900	—	700	900		700	900	_	MHz	—
tPD	Propagation Delay to Output CLK MR	600 600	800 800	1000 1000	600 600	800 800	1000 1000	600 600	800 800	1000 1000	ps	_
ts	Set-up Time D SEL	50 300	-100 150	_	50 300	-100 150	_	50 300	-100 150		ps	_
tн	Hold Time D SEL	300 75	100 -150	_	300 75	100 -150	_	300 75	100 -150		ps	_
trr	Reset Recovery Time	900	700	_	900	700		900	700		ps	—
tPW	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	_	—	ps	_
tskew	Within-Device Skew	—	75	_	—	75	_	—	75		ps	1
tr tf	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

#### 28-PIN PLCC (J28-1)



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