INTEGRATED CIRCUITS



Product data Supersedes data of 1995 Sep 06 2002 Dec 17



74ABT651

FEATURES

- Independent registers for A and B buses
- The 74ABT651 is the inverting version of the 74ABT652
- Multiplexed real-time and stored data
- 3-State outputs
- Live insertion/extraction permitted.
- Power-up 3-State
- Power-up reset
- Output capability: +64 mA / -32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT651 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT651 transceiver/register consists of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output Enable (OEAB, \overline{OEBA}) and Select (SAB, SBA) pins are provided for bus management.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT651.

The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay CPBA to An or CPAB to Bn	C _L = 50 pF; V _{CC} = 5 V	3.8 4.4	ns
C _{IN}	Input capacitance	$V_I = 0 V \text{ or } V_{CC}$	4	pF
C _{I/O}	I/O capacitance	Outputs disabled; $V_0 = 0 V \text{ or } V_{CC}$	7	pF
I _{CCZ}	Total supply current	Outputs disabled; V_{CC} = 5.5 V	110	μΑ

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
24-Pin Plastic DIP	–40 °C to +85 °C	74ABT651N	SOT222-1
24-Pin plastic SO	–40 °C to +85 °C	74ABT651D	SOT137-1
24-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74ABT651PW	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 23	CPAB / CPBA	A to B clock input / B to A clock input
2, 22	SAB / SBA	A to B select input / B to A select input
3, 21	OEAB / OEBA	A to B Output Enable input / B to A Output Enable input (active–LOW)
4, 5, 6, 7, 8, 9, 10, 11	A0 – A7	Data inputs/outputs (A side)
20, 19, 18, 17, 16, 15, 14, 13 B0 – B7		Data inputs/outputs (B side)
12	GND	Ground (0 V)
24	V _{CC}	Positive supply voltage

Product data

Octal transceiver/register, inverting (3-State)

74ABT651





LOGIC SYMBOL

Product data

74ABT651

FUNCTION TABLE

		INPUT	6			DAT	A I/O	OPERATING MODE
OEAB	OEBA	CPAB	СРВА	SAB	SBA	An	Bn	OFERATING MODE
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B data
X H	H H	$\uparrow \uparrow$	H or L ↑	X **	X X	Input	Unspecified output*	Store A, Hold B Store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X **	Unspecified output*	Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time \overline{B} data to A bus Stored \overline{B} data to A bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real time \overline{A} data to B bus Store \overline{A} data to B bus
Н	L	H or L	H or L	н	Н	Output	Output	Stored \overline{A} data to B bus Stored \overline{B} data to A bus

H = HIGH voltage level L = LOW voltage level X = Don't care

X ↑ LOW-to-HIGH clock transition =

The data output function may be enabled or disabled by various signals at the OEBA and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

** If both Select controls (SAB and SBA) are LOW, then clocks can occur simultaneously. If either Select control is HIGH, the clocks must be staggered in order to load both registers.

LOGIC DIAGRAM



74ABT651

ABSOLUTE MAXIMUM RATINGS^{1, 2}

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SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0 V	-18	mA
VI	DC input voltage ³		-1.2 to +7.0	V
I _{ОК}	DC output diode current	V _O < 0 V	-50	mA
V _{OUT}	DC output voltage ³	age ³ output in Off or HIGH state		V
I _{OUT}	DC output current	output in LOW state	128	mA
T _{stg}	Storage temperature range		-65 to 150	°C

NOTES:

 Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIM	UNIT	
STMBOL	TANAMETEN	Min	Max	ONT
V _{CC}	DC supply voltage	4.5	5.5	V
VI	Input voltage	0	V _{CC}	V
V _{IH}	HIGH-level input voltage	2.0		V
V _{IL}	LOW-level Input voltage		0.8	V
I _{ОН}	HIGH-level output current		-32	mA
I _{OL}	LOW-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

Philips Semiconductors

Product data

Octal transceiver/register, inverting (3-State)

74ABT651

DC ELECTRICAL CHARACTERISTICS

						LIMITS				
SYMBOL	PARAMETER		TEST CONDITIONS	T _{ar}	_{nb} = +25	°C	T _{amb} = −40 °C to +85 °C		UNIT	
				Min	Тур	Max	Min	Max		
V _{IK}	Input clamp vo	ltage	$V_{CC} = 4.5 \text{ V}; \text{ I}_{IK} = -18 \text{ mA}$		-0.9	-1.2		-1.2	V	
			V_{CC} = 4.5 V; I_{OH} = -3 mA; V_I = V_{IL} or V_{IH}	2.5	3.2		2.5		V	
V _{OH}	HIGH-level out	put voltage	V_{CC} = 5.0 V; I_{OH} = -3 mA; V_I = V_{IL} or V_{IH}	3.0	3.7		3.0		V	
			V_{CC} = 4.5 V; I_{OH} = -32 mA; V_I = V_{IL} or V_{IH}	2.0	2.30		2.0		V	
V _{OL}	LOW-level out	out voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V	
V _{RST} ³	Power-up outp	ut low voltage	V_{CC} = 5.5 V; I_{O} = 1 mA; V_{I} = GND or V_{CC}		0.13	0.55		0.55	V	
ų	Input leakage	Control pins	$V_{CC} = 5.5 \text{ V}; \text{ V}_{I} = \text{GND or } 5.5 \text{ V}$		±0.01	±1.0		±1.0	μΑ	
1	current	Data pins	$V_{CC} = 5.5 \text{ V}; \text{ V}_{I} = \text{GND or } 5.5 \text{ V}$		±5	±100		±100	μΑ	
I _{OFF}	Power-off leaka	age current	V_{CC} = 0.0 V; V_O or $V_1 \ \leq \ 4.5 \ V$		±5.0	±100		±100	μΑ	
I _{PU} /I _{PD}	Power-up/down output current ⁴		$V_{CC} = 2.1 \text{ V}; V_O = 0.5 \text{ V}; \text{ V} \overline{OE} = \text{Don't Care};$ $V_I = \text{GND or V}_{CC}$		±5.0	±50		±50	μA	
I _{IH} + I _{OZH}	3-State output	HIGH current	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.7 \text{ V}; V_{I} = V_{IL} \text{ or } V_{IH}$		5.0	50		50	μA	
I _{IL} + I _{OZL}	3-State output	LOW current	$V_{CC} = 5.5 \text{ V}; V_O = 0.5 \text{ V}; V_I = V_{IL} \text{ or } V_{IH}$		-5.0	-50		-50	μΑ	
I _{CEX}	Output High lea	akage current	V_{CC} = 5.5 V; V_{O} = 5.5 V; V_{I} = GND or V_{CC}		5.0	50		50	μA	
Ι _Ο	Output current	1	$V_{CC} = 5.5 \text{ V}; V_{O} = 2.5 \text{ V}$	-40	-65	-180	-40	-180	mA	
I _{CCH}			V_{CC} = 5.5 V; Outputs High, V_I = GND or V_{CC}		110	250		250	μΑ	
I _{CCL}	Quiescent supply current		V_{CC} = 5.5 V; Outputs Low, V_{I} = GND or V_{CC}		20	30		30	mA	
I _{CCZ}			V_{CC} = 5.5 V; Outputs 3–State; V _I = GND or V _{CC}		110	250		250	μA	
ΔI_{CC}	Additional supp input pin ²	oly current per	V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V _{CC} or GND; V _{CC} = 5.5 V		0.3	1.5		1.5	mA	

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

2. This is the increase in supply current for each input at 3.4 V.

3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

4. This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 msec. From V_{CC} = 2.1 V to V_{CC} = 5 V \pm 10%, a transition time of up to 100 µsec is permitted.

AC CHARACTERISTICS

GND = 0 V; t_{R} = t_{F} = 2.5 ns; C_{L} = 50 pF, R_{L} = 500 Ω

		LIMITS						
SYMBOL	PARAMETER	WAVEFORM		ר _{amb} = +25 ° V _{CC} = +5.0 ₪		$\begin{array}{c} T_{amb} = -40 \\ V_{CC} = +5. \end{array}$	°C to +85 °C .0 V ±0.5 V	UNIT
			Min	Тур	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	125	300		125		MHz
t _{PLH} t _{PHL}	Propagation delay CPAB to Bn or CPBA to An	1	2.2 1.7	3.8 4.4	5.1 5.1	2.2 1.7	5.6 5.6	ns
t _{PLH} t _{PHL}	Propagation delay An to Bn or Bn to An	2	1.5 1.5	3.2 3.7	5.1 4.6	1.5 1.5	6.2 5.4	ns
t _{PLH} t _{PHL}	Propagation delay SAB to Bn or SBA to An	3	1.5 1.5	3.8 4.4	5.1 4.9	1.5 1.5	6.5 5.9	ns
t _{PZH} t _{PZL}	Output enable time OEBA to An	5 6	1.3 2.5	3.7 4.7	4.6 6.8	1.3 2.5	5.8 8.5	ns
t _{PHZ} t _{PLZ}	Output disable time OEBA to An	5 6	1.5 1.5	4.0 3.2	4.5 3.8	1.5 1.5	5.0 4.1	ns
t _{PZH} t _{PZL}	Output enable time OEAB to Bn	5 6	1.8 2.9	3.4 4.5	6.1 6.5	1.8 2.9	6.5 7.4	ns
t _{PHZ} t _{PLZ}	Output disable time OEAB to Bn			3.8 3.1	4.5 4.4	1.5 1.5	5.5 5.1	ns

AC SET-UP REQUIREMENTS

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF, R_L = 500 Ω

					LIMITS	
SYMBOL PARAMETER		WAVEFORM	$T_{amb} = +25 °C V_{CC} = +5.0 V$		T _{amb} = −40 °C to +85 °C V _{CC} = +5.0 V ±0.5 V	UNIT
			Min	Тур	Min	
t _s (H) t _s (L)	Set-up time An to CPAB, Bn to CPBA	4	3.0 3.0	1.2 0.8	3.0 3.0	ns
t _h (H) t _h (L)	Hold time An to CPAB, Bn to CPBA	4	0.0 0.0	-0.8 -0.9	0.0 0.0	ns
t _w (H) t _w (L)	Pulse width, HIGH or LOW CPAB or CPBA	1	4.0 4.0	1.2 1.1	4.0 4.0	ns

AC WAVEFORMS

 V_{M} = 1.5 V; V_{IN} = GND to 3.0 V



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Propagation Delay, An to Bn or Bn to An







Waveform 4. Data Set-up and Hold Times



Waveform 5. 3–State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level



Waveform 6. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORM





inches

Note

0.185

OUTLINE

VERSION

SOT222-1

0.015

0.155

IEC

0.045

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

0.017

JEDEC

MS-001

0.010

REFERENCES

1.240

0.246



SOT222-1

74ABT651

9

EIAJ

0.100

0.300

0.120

0.30

EUROPEAN

PROJECTION

F

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0.300

0.01

ISSUE DATE

99-04-28

99-12-27

0.081

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1 D Α Х HE = v 🕅 A $\overline{\Pi}$ у 13 Q 4 ٩0 (A_3) А pin 1 index 12 detail X ↓<mark>↓</mark> bp е 10 mm 0 5 scale DIMENSIONS (inch dimensions are derived from the original mm dimensions) Α z⁽¹⁾ D ⁽¹⁾ E⁽¹⁾ UNIT Α1 A₂ Α3 H_E Lp Q θ bp с L v w У е max. 0.30 2.45 0.49 0.32 15.6 7.6 10.65 1.1 1.1 0.9 2.65 0.1 mm 0.25 1.27 1.4 0.25 0.25 0.10 2.25 0.36 0.23 15.2 7.4 10.00 0.4 1.0 0.4 8⁰ 0^{o} 0.043 0.035 0.012 0.096 0.019 0.013 0.61 0.30 0.419 0.043 inches 0.10 0.050 0.055 0.004 0.01 0.01 0.01 0.004 0.089 0.014 0.009 0.60 0.29 0.394 0.016 0.039 0.016 Note 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included. REFERENCES OUTLINE EUROPEAN **ISSUE DATE** PROJECTION VERSION IEC JEDEC EIAJ 97-05-22 SOT137-1 075E05 MS-013 \odot £

74ABT651

99-12-27



2002 Dec 17

REVISION HISTORY

Rev	Date	Description
_2	20021216	Product data (9397 750 10849); ECN 853-1783 29290 of 12 December 2002. Supersedes data of 06 September 1995.
		Modifications:
		 Ordering information table: remove "North America" column; remove 74ABT651DB package offering.
_1	19950906	Product specification. ECN 853-1783 15703 of 06 September 1995.

74ABT651

Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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