

XRD9827 12-Bit Linear CIS/CCD Sensor Signal Processor with Serial Control

Color and Grayscale Flatbed Scanners

General Purpose CIS or CCD Imaging

Simple and Direct Interface to Canon 600 DPI

Multifunction Peripherals

Low Cost Data Acquisition

Digital Color Copiers

Color and Grayscale Sheetfed Scanners

APPLICATIONS

Sensors

December 2000-2

FEATURES

- 12-Bit Resolution, No Missing Codes
- One-channel 6MSPS Pixel Rate
- Triple-channel 2MSPS Pixel Rate
- 6-Bit Programmable Gain Amplifier
- 8-Bit Programmable Offset Adjustment
- CIS or CCD Compatibility
- Internal Clamp for CIS or CCD AC Coupled Configurations
- 3.0V or 5V Operation & I/O Compatibility
- Serial Load Control Registers
- Low Power CMOS: 200mW-typ
- Low Cost 20-Lead Packages
- USB Compliant

GENERAL DESCRIPTION

The XRD9827 is a complete linear CIS or CCD sensor signal processor on a single monolithic chip. The XRD9827 includes a high speed 12-Bit resolution ADC, a 6-Bit Programmable Gain Amplifier with gain adjustment of 1 to 10, and 8-Bit programmable input referred offset calibration range of 800mV.

In the CCD configuration the input signal is AC coupled with an external capacitor. An internal clamp sets the black level. In the CIS configuration, the clamp switch can be disabled and the CIS output signal is DC coupled from the CIS sensor to the XRD9827. The CIS signal is level shifted to VRB in order to use the full range of the ADC. In the CIS configuration the input can also be AC coupled similar to the CCD configuration. This enables CIS signals with large black levels to be internally clamped to a DC reference equal to the black level. The DC reference is internally subtracted from the input signal.

The CIS configuration can also be used in other applications that do not require CDS function, such as low cost data acquisition.

ORDERING INFORMATION

Rev. 3.00

PackageType	TemperatureRange	PartNumber
20-Lead SOIC	0°C to +70°C	XRD9827ACD
20-Lead SSOP	0°C to +70°C	XRD9827ACU



Figure 1. Functional Block Diagram







PINCONFIGURATION



20-Lead SOIC

PIN DESCRIPTION

Pin#	Symbol	Description
1	DVDD	Digital VDD (for Output Drivers)
2	DB0	Data Output Bit 0
3	DB1	Data Output Bit 1
4	DB2	Data Output Bit 2
5	DB3	Data Output Bit 3
6	DB4	Data Output Bit 4
7	DB5/SCLK	Data Output Bit 5 & Data Input SCLK
8	DB6/SDATA	Data Output Bit 6 & Data Input SDATA
9	DB7/LD	Data Output Bit 7 & LD
10	DGND	Digital Ground (for Output Drivers)
11	ADCCLK	A/D Converter Clock
12	CLAMP	Clamp and Video Sample Clock
13	SYNCH	Start of New Line and Serial Data Input Control
14	AGND	Analog Ground
15	VREF+	A/D Positive Reference for Decoupling Cap
16	VDCEXT	External DC Reference
17	BLU	Blue Input
18	GRN	Green Input
19	RED	Red Input
20	AVDD	Analog Power Supply

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ELECTRICAL CHARACTERISTICS

Test Conditions: $AV_{DD} = DV_{DD} = 5V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

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Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
Power Suppli	ies					
AV	Analog Power Supply	3.0	3.3	5.5	V	(Note 2)
	Digital I/O Power Supply	3.0	3.3	5.5	V	$DV_{DD} \le AV_{DD}$
I _{DD}	Supply Current	25	40	60	mA	V _{DD} =5V
	Power Down Power Supply Current			50	μA	V _{DD} =5V
ADC Specific	ations			4		
RES	Resolution	12			Bits	
Fs	Maximum Sampling Rate	12			MSPS	
DNL	Differential Non-Linearity		±0.5		LSB	
INL	Integral Non-Linearity		±1.0		LSB	
MON	Monotonicity		Yes			
V _{RT}	Top Reference Voltage	3.50	3.70	3.90	V	$AV_{DD} = DV_{DD} = 5.0V$
V _{RB}	Bottom Reference Voltage		0.5		V	$AV_{DD} = DV_{DD} = 5.0V$
DV_{REF}	Differential Reference Voltage	0.6 AV _{DD}	3.35V		V	$AV_{DD} = DV_{DD} = 5.0V$
	(V _{RT} - V _{RB})					
R_{L}	Ladder Resistance	300	600	780	Ω	
PGA & Offse	t DAC Specifications					
PGARES	PGA Resolution	6			Bits	
PGAG _{MIN}	Minimum Gain	0.950	1.0	1.050	V/V	
	Maximum Gain	9.5	10.0	10.50	V/V	
PGAGD	Gain Adjustment Step Size		0.14		V/V	
V_{black}	Black Level Input Range	-100		500	mV	DC Configuration
DACRES	Offset DAC Resolution	8			Bits	
	Minimum Offset Adjustment	-250	-200	-150	mV	Mode 111, D5=0 (Note 1)
	Maximum Offset Adjustment	+500	+600	+700	mV	Mode 111, D5=0
OFF	Minimum Offset Adjustment	-450	-400	-350	mV	Mode 111, D5=1 (Note 1)
	Maximum Offset Adjustment	+350	+400	+450	mV	Mode 111, D5=1
OFF∆	Offset Adjustment Step Size		3.14		mV	

Note 1: The additional ±100 mV of adjustment with respect to the black level input range is needed to compensate for any additional offset introduced by the XRD9827 Buffer/PGA internally.

Note 2: It is not recommended to operate the part between 3.6V and 4.4V.

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ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD} = DV_{DD} = 5V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
Buffer Sp	ecifications					
I,	Input Leakage Current			100	nA	
CIN	Input Capacitance		10		рF	
VIN _{PP}	AC Input Voltage Range	0		AV _{DD} -1.4	V	CIS AC; INT V _{DCREF} , Config Reg => XXX010XX Gain=1 (Note 1)
	AC Input Voltage Range	0		DV_{REF}	V	CCD AC; INT V _{DCREF} Config Reg=> XXX011XX Gain=1 (Note 1)
VIN	DC Input Voltage Range	-0.1		AV _{DD} -1.4	V	CIS DC; INT V _{DCREF,} Config Reg => XXX000XX Gain=1 (Note 2)
	DC Input Voltage Range	V _{dcext} -0.1		V _{dcext} + DV _{ref}	V	CIS DC; EXT V_{DCREF} Config Reg=> XXX100XX Gain=1 (Note 3) V_{DCEXT} +D $V_{REF} \le AV_{DD}$
V _{dcext}	External DC Reference	0.3		2.5	V	$AV_{DD} = DV_{DD} = 5.0V$ CIS DC; EXT V _{DCREF} Config Reg=> XXX100XX
VIN	Input Dondwidth (Small Signal)		10			
VIN _{BW}	Input Bandwidth (Small Signal) Channel to Channel Crosstalk		-		MHz dB	
VIN _{ct}	Clamp Specifications		-60		αв	
	Clamp Voltage		AGND	50	mV	CIS (AC) Config, $AV_{DD} = DV_{DD} = 5.0V$
V _{CLAMP}	Champ Voltage	3.5	V _{RT}		V	CCD (AC) Config, $AV_{DD} = DV_{DD} = 5.0V$
R _{INT}	Clamp Switch On Resistance	0.0	100	150	Ω	$AV_{DD} = DV_{DD} = 5.0V$
R _{OFF}	Clamp Switch Off Resistance	10			MΩ	$AV_{DD} = DV_{DD} = 5.0V$

Note 1: VIN_{PP} is the signal swing before the external capacitor tied to the MUX inputs.

Note 2: The -0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference (clamp) voltage.

Note 3: The V_{DCEXT}-0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference voltage.

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ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD} = DV_{DD} = 5V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

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Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
System Spe	cifications (MUX + Buffer + PG	A + ADC)				Note 1
SYS	System DNL	-1.0	±0.5	+4.0	LSB	$AV_{DD} = DV_{DD} = 5.0V$
SYS_{LIN}	System Linearity		±6.0		LSB	
SYS_{GE}	System Gain Error	-5.0		+5.0	%	
IRN	Input Referred Noise		1.5		mV _{rms}	Gain=1
	Input Referred Noise		0.5		mV _{rms}	Gain=10
System Tim	ng Specifications			•		
tcklw	ADCCLK Low Pulse Width	50	83		ns	
tckhw	ADCCLK High Pulse Width	70	83		ns	
tckpd	ADCCLK Period	120	166		ns	
tsypw	SYNCH Pulse Width	30			ns	
trars	Rising ADCCLK to rising SYNCH	0				SYNCH must rise equal to or after ADCCLK, See Figure 18
tclpw	CLAMP Pulse Width	30			ns	Note 2
Write Timing	Specifications					
tsclkw	SCLK Pulse Width	40			ns	
tdz	LD Low to SCLK High	20			ns	
tds	Input Data Set-up Time	20			ns	
tdh	Input Data Hold Time	0			ns	
tdl	SCLK High to LD High	50			ns	
ADC Digital	Output Specifications					•
tap	Aperture Delay		10		ns	
td∨	Output Data Valid		20	40	ns	
tsa	SYNCH to ADCCLK	15			ns	3ch Pixel Md
tlat	Latency		8		cycles	Config 00, 11
tlat	Latency		6		pixels	Config 01, 10
Digital Input	Specifications					
V _{IH}	Input High Voltage	AV _{DD} -2.5			V	
V _{IL}	Input Low Voltage			1	V	
I _{IH}	High Voltage Input Current		5		μA	
I _{IL}	Low Voltage Input Current		5		μA	
C _{IN}	Input Capacitance		10		pF	

Note 1: System performance is specified for typical digital system timing specifications.

Note 2: The actual minimum 'tclpw' is dependent on the external capacitor value, the CIS output impedance. During 'clamp' operation, sufficient time needs to be allowed for the external capacitor to charge up to the correct operating level. Refer to the description in Theory of Operation, CIS Config.

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ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD} = DV_{DD} = 5V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
Digital Output	Digital Output Specifications					
V _{OH}	Output High Voltage	80			(%)DVDD	I _L =1mA
V _{ol}	Output Low Voltage			20	(%)DVDD	I _L =-1mA
I _{Oz}	Output High-Z Leakage Current	-10		10	μΑ	
C _{OUT}	Output Capacitance		10		pF	
SR	Slew Rate (10% to 90% DV_{DD})	2		15	ns	$C_L = 10 pF, DV_{DD} = 3.3 V$



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ELECTRICAL CHARACTERISTICS

Test Conditions: $AV_{DD} = DV_{DD} = 3V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

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Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
Power Suppl	ies					
AV	Analog Power Supply	3.0	3.3	5.5	V	(Note 2)
	Digital I/O Power Supply	3.0	3.3	5.5	V	$DV_{DD} \le AV_{DD}$
I _{DD}	Supply Current			60	mA	V _{DD} =3V
	Power Down Power Supply Current			50	μA	V _{DD} =3V
ADC Specific	ations					•
RES	Resolution	12			Bits	
F_{s}	Maximum Sampling Rate	12			MSPS	
DNL	Differential Non-Linearity		±0.5		LSB	
INL	Integral Non-Linearity		±1.0		LSB	
MON	Monotonicity		Yes			
V _{rt}	Top Reference Voltage	2.1	2.2	2.34	V	$AV_{DD} = DV_{DD} = 3.0V$
V _{RB}	Bottom Reference Voltage		0.3		V	$AV_{DD} = DV_{DD} = 3.0V$
DV_{REF}	Differential Reference Voltage		2.0V		V	$AV_{DD} = DV_{DD} = 3.0V$
	(V _{RT} - V _{RB})					
$R_{\scriptscriptstyle L}$	Ladder Resistance	300	600	780	Ω	
PGA & Offse	t DAC Specifications					
PGARES	PGA Resolution	6			Bits	
PGAG _{MIN}	Minimum Gain	0.950	1.0	1.050	V/V	
$PGAG_{MAX}$	Maximum Gain	9.5	10.0	10.50	V/V	
PGAGD	Gain Adjustment Step Size		0.14		V/V	
V_{black}	Black Level Input Range	-100		500	mV	DC Configuration
DACRES	Offset DAC Resolution	8			Bits	
	Minimum Offset Adjustment		-200		mV	Mode 111, D5=0 (Note 1)
OFF_{MAX}	Maximum Offset Adjustment		+600		mV	Mode 111, D5=0
	Minimum Offset Adjustment		-400		mV	Mode 111, D5=1 (Note 1)
OFF _{MAX}	Maximum Offset Adjustment		+400		mV	Mode 111, D5=1
OFFΔ	Offset Adjustment Step Size		3.14		mV	

Note 1: The additional ±100 mV of adjustment with respect to the black level input range is needed to compensate for any additional offset introduced by the XRD9827 Buffer/PGA internally.

Note 2: It is not recommended to operate the part between 3.6V and 4.4V.

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ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD} = DV_{DD} = 3V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
Buffer Sp	ecifications					
I,	Input Leakage Current			100	nA	
CIN	Input Capacitance		10		pF	
VIN _{PP}	AC Input Voltage Range	0		AV _{DD} -1.4	V	CIS AC; INT V _{DCREF,} Config Reg => XXX010XX Gain=1 (Note 1)
	AC Input Voltage Range	0		DV _{REF}	V	CCD AC; INT V _{DCREF} Config Reg=> XXX011XX Gain=1 (Note 1)
VIN	DC Input Voltage Range	-0.1		AV _{DD} -1.4	V	CIS DC; INT V _{DCREF,} Config Reg => XXX000XX Gain=1 (Note 2)
	DC Input Voltage Range	V _{DCEXT} -0.1		V _{dcext} + DV _{ref}	V	CIS DC; EXT V_{DCREF} Config Reg=> XXX100XX Gain=1 (Note 3) V_{DCEXT} +D $V_{REF} \le AV_{DD}$
V _{dcext}	External DC Reference	0.3		1.3	V	$AV_{DD} = DV_{DD} = 3.0V$ CIS DC; EXT V_{DCREF} Config Reg=> XXX100XX
\/INI			10			
VIN _{BW}	Input Bandwidth (Small Signal) Channel to Channel Crosstalk				MHz dB	
VIN _{ct}	Clamp Specifications		-60		αв	
	Clamp Voltage		AGND	50	mV	CIS (AC) Config, $AV_{DD} = DV_{DD} = 3.0V$
V_{clamp}	Champ Voltage	2.1	V _{RT}	50	V	CCD (AC) Config, $AV_{DD} = DV_{DD} = 3.0V$ CCD (AC) Config, $AV_{DD} = DV_{DD} = 3.0V$
R _{INT}	Clamp Switch On Resistance		100	250	Ω	$AV_{DD} = DV_{DD} = 3.0V$
R _{OFF}	Clamp Switch Off Resistance	10			MΩ	$AV_{DD} = DV_{DD} = 3.0V$

Note 1: VIN_{PP} is the signal swing before the external capacitor tied to the MUX inputs.

Note 2: The -0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference (clamp) voltage.

Note 3: The V_{DCEXT}-0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference voltage.

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ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD} = DV_{DD} = 3V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
System Spe	cifications (MUX + Buffer + PG	A + ADC)				Note 1
SYS	System DNL	-1.0	±0.5	+6.0	LSB	$AV_{DD} = DV_{DD} = 3.0V$
a \/a						
SYS_{LIN}	System Linearity		±6.0		LSB	
SYS_{GE}	System Gain Error	-5.0		+5.0	%	
IRN	Input Referred Noise		1.5		mV _{rms}	Gain=1
	Input Referred Noise		0.5		mV _{rms}	Gain=10
System Tim	ing Specifications	-			-	
tcklw	ADCCLK Low Pulse Width	50	83		ns	
tckhw	ADCCLK High Pulse Width	70	83		ns	
tckpd	ADCCLK Period	120	166		ns	
tsypw	SYNCH Pulse Width	30			ns	
trars	Rising ADCCLK to rising	0				SYNCH must rise equal to
	SYNCH					or after ADCCLK, See Figure 18
tclpw	CLAMP Pulse Width	30			ns	Note 2
Write Timing	Specifications				-	
tsclkw	SCLK Pulse Width	40			ns	
tdz	LD Low to SCLK High	20			ns	
tds	Input Data Set-up Time	20			ns	
tdh	Input Data Hold Time	0			ns	
tdl	SCLK High to LD High	50			ns	
ADC Digital	Output Specifications					
tap	Aperture Delay		15		ns	
td∨	Output Data Valid		30	50	ns	
tsa	SYNCH to ADCCLK	20			ns	3ch Pixel Md
tlat	Latency		8		cycles	Config 00, 11
tlat	Latency		6		pixels	Config 01, 10
Digital Input	Specifications					
V _{IH}	Input High Voltage	AV _{DD} -0.5			V	
V _{IL}	Input Low Voltage	00		1	V	
I _{II}	High Voltage Input Current		5		μA	
I _{IL}	Low Voltage Input Current		5		μΑ	
	Input Capacitance		10		pF	
IN						

Note 1: System performance is specified for typical digital system timing specifications.

Note 2: The actual minimum 'tclpw' is dependent on the external capacitor value, the CIS output impedance. During 'clamp' operation, sufficient time needs to be allowed for the external capacitor to charge up to the correct operating level. Refer to the description in Theory of Operation, CIS Config.

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ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: $AV_{DD} = DV_{DD} = 3V$, ADCCLK=6MHz, 50% Duty Cycle, $T_A = 25^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Conditions
Digital Output	Digital Output Specifications					
V _{OH}	Output High Voltage	80			(%)DVDD	I _L = 1mA
V _{ol}	Output Low Voltage			20	(%)DVDD	I _L = -1mA
I _{Oz}	Output High-Z Leakage Current	-10		10	μA	
C _{OUT}	Output Capacitance		10		pF	
SR	Slew Rate (10% to 90% DV_{DD})	2		15	ns	$C_{L} = 10 pF, DV_{DD} = 3.3 V$





THEORY OF OPERATION

CIS Configuration (Contact Image Sensor)

The XRD9827 has two configurations for CIS applications. Each configuration is set by the control registers accessed through the serial port.

Mode 1. DC Coupled

If the CIS does not have leading or trailing black pixels as shown in Figure 2, then DC couple the CIS output to the XRD9827 input.



Figure 2. Typical Output CIS Mode

Adjust the offset of the CIS (-100 mV to 500 mV) by setting the internal registers of the XRD9827 to set the black pixel value when the LEDs of the CIS are off. When the LEDs are on, use the XRD9827 Programmable Gain to maximize the ADCs dynamic range. Figure 3 shows a typical application for a CIS with an offset of -100mV to 500mV.







Figure 3. Application with Offset in the Range (-100mv to 500mv)

The input is added to VRB before the signal passes through the ADC. If the CIS output is zero, then the output of the ADC will be zero code. This enables the CIS to be referenced to the bottom ladder reference voltage to use the full range of the ADC.

Some CIS sensors have an output with an offset voltage of greater than 500mV. If the CIS output is beyond the

offset range of the XRD9827 (see Offset Control DAC, Pg. 28) set the internal mode registers to external reference. An external reference voltage equal to the value of the CIS offset voltage can be applied to VDCEXT (Figure 4) in order to meet the dynamic range of the XRD9827. Figure 4 is a diagram of the XRD9827 in the external reference mode for CIS, DC coupled applications.







Figure 4. Application with Offset Greater Than (-100mv to 500mv)

The DC reference voltage applied to VDCEXT does not have to be accurate. The internal offset DAC voltage is still used in this mode for fine adjustment. VDCEXT

cannot be used as an input from the CIS. Any signal applied to VDCEXT will be subtracted from the output signal of the multiplexer.







Figure 5. Typical Application Circuitry CIS DC Coupled Non-Inverted Mode





CIS Mode Timing -- DC Coupled (CLAMP disabled)



Figure 6. Timing Diagram for Figure 5

ADCCLK	Events
\downarrow	ADC Sample & PGA Start Tracking next Pixel
	MSB Data Out
Ŷ	LSB Data Out
HI	ADC Track PGA Output
LO	ADC Hold/Convert



Mode 2. AC Coupled

If the CIS signal has a black reference for the video signal, an external capacitor $\rm C_{\rm EXT}$ is used. When CLAMP (clamp) pin is set high an internal switch allows

one side of the external capacitor to be set to ground. It then is level shifted to correspond to the bottom ladder reference voltage of the ADC (Figure 7).

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Figure 7. CIS AC Coupled Application

This value corresponds to the black reference of the image sensor. When the CLAMP pin is set back to low, the ADC samples the video signal with respect to the black reference. The typical value for the external capacitor is 100pF. This value should be adjusted according to the time constant (Tc) needed in a particular application. The CLAMP pin has an internal 150 ohm impedance (R_{INT}) which is in series with the external capacitor (C_{EXT}).

Therefore, $Tc = 1/R_{INT}C_{EXT}$

If the input to the external capacitor has a source impedance (R $_{\rm EXT}$), then:

$$T_c = 1/(R_{INT} + R_{EXT})C_{EXT}$$







Figure 8. Typical Application Circuitry CIS AC Coupled Non-Inverted







CIS Mode Timing -- AC Coupled (CLAMP enabled)

Figure 9. Timing Diagram for Figure 8

ADCCLK	Events
\downarrow	ADC Sample & PGA Start Track of next Pixel
	MSB Data Out
\uparrow	LSB Data Out
HI	ADC Track PGA Output
LO	ADC Hold/Convert

Table 3.

CLAMP	Events
HI	PGA Tracks V _{CLAMP} & C _{EXT} is Charged to
	$V_{_{BLACK}}$ - $V_{_{CLAMP}}$, which is equal to $V_{_{BLACK}}$
LO	PGA Tracks VIN _{PP}

Table 4.

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Internal CIS Reference Circuit (DB 4 = 1)

The XRD9827 has an internal register reserved for interfacing to the Canon CIS model number CVA-60216K. When this register is selected, the VDCEXT (Pin 16) becomes an output voltage of 1.24 volts. This voltage can be directly connected to the VREF (Pin 5) of the Canon sensor. This reduces the amount of components needed for biasing the Canon CIS sensor (the external diodes and resistors typically used in this application have been included inside the XRD9827 for this mode of operation). Below is a typical application circuit using the XRD9827 and the Canon CVA-60216K CIS sensor.



Figure 10. Typical Application Circuitry Internal CIS Reference Circuit Mode CANON CIS Sensor, Model #CVA=60216k





CIS Line-By-Line Rotating Gain and Offset (Configuration DB1 = 1, DB0 = 1)

Line-by-line rotating gain and offset minimizes the amount of write cycles per scan. Pre-loaded values of gain and offset can be loaded for each color before the first line is scanned. Each gain and offset is cycled through line-by-line so that the gain and offset do not have to be loaded in between lines. Below is the typical application circuit and timing for this configuration.



Figure 11. Typical Application Circuitry Internal CIS Rotating Gain and Offset Line-By-Line





Note: Y = Previous State

Figure 12. Timing Diagram for Figure 11

CCD Configuration (Charge Coupled Device)

Mode 1. AC Coupled

In the CCD configuration of operation, an external capacitor needs to be chosen according to the equations below. The typical value for the external capacitor is 100pF. This value should be adjusted according to the time constant (Tc) needed in a particular application. The CLAMP pin has an internal 150 ohm impedance (R_{INT}) which is in series with the external capacitor (C_{EXT}).

Therefore, $Tc = 1/R_{INT}C_{EXT}$

If the input to the external capacitor has a load impedance ($\rm R_{\rm \tiny Ext}$), then

When CLAMP (clamp) pin is set high an internal switch allows one side of the external capacitor to be set to VRT (Figure 13). This value corresponds to the black reference of the CCD. When the CLAMP pin is set back to low, the ADC samples the video signal with respect to the black reference. The difference between the black reference and the video signal is the actual pixel value of the video content. Since this value is referenced to the top ladder reference voltage of the ADC a zero input signal would yield a full scale output code. Therefore, the output of the conversion is inverted (internally) to correspond to zero scale output code.







Figure 13. CCD AC Coupled Application

Area or Linear CCD Applications

Figure 13 is a block diagram for applications with Area or Linear CCDs (The timing for Area CCDs and B/W CCDs is the same). For Area or Linear CCD applications, a global offset is loaded into the serial port at the beginning of a line. The gain is set to adjust for the highest color intensity of the CCD output. Once the pixel values have been sampled, the gain and offset are adjusted at the beginning of the next line. For example, if there is a line-to-line variation between the black reference pixels, the offset is adjusted. The gain is always adjusted for the highest color intensity.







Figure 14. Typical Application Circuitry Single Channel CCD AC Coupled Inverted Mode









Figure 15. Timing Diagram for Figure 14

Triple Channel CCD Application

Figure 16 is a block diagram for pixel-by-pixel applications with triple channel CCDs. During the optically shielded section of a pixel, CLAMP must go high to store the black reference on each capacitor to the input. The gain and offset is automatically rotated to adjust for each channel input. The MSBs are available on the output bus on the falling edge of ADCCLK. The LSBs are available on the rising edge of ADCCLK.









Figure 16. CCD AC Coupled Application







Figure 17. Typical Application Circuitry Triple Channel CCD AC Coupled Inverted Mode







PIXEL-BY-PIXEL 3 CHANNEL CCD -- AC Coupled



Figure 18. Timing Diagram for Figure 17

ADCCLK	Events
3rd ↓	Simultaneous RED/GRN/BLU Sample Every 3rd CLK.
	Convert RED, S/H GRN, S/H BLU.
All ↓	MSB Data Out
\uparrow	LSB Data Out
HI	ADC Track PGA Output
LO	ADC Hold/Convert
CLAMP	Events
HI	Internal Clamp Enabled
LO	Internal RED/GRN/BLU Tracking Enabled
SYNCH	Events
HI	Reset Internal Mux to Red, Output Bus is Tri-stated
LO	Increment Mux Color on Falling Edge of ADCCLK

Table 5.

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XRD9827



Mode 2. DC Coupled

Typical CCDs have outputs with black references. Therefore, DC Coupled is not recommended for CCD applications.

Offset Control DAC

The offset DAC is controlled by 8 bits. The offset range is 800 mV ranging from -200 mV to +600 mV (when DB5 is set to 0) and -400 mV to +400 mV (when DB5 is set to 1). Therefore, the resolution of the 8-Bit offset DAC is 3.14 mV. However, the XRD9827 has +/- 100 mV reserved for internal offsets. Therefore, the effective range for adjusting for CIS offsets or black reference is 600 mV. The offset adjustment is used primarily to correct for the difference between the black level of the image sensor and the bottom ladder reference voltage (VRB) of the ADC. By adjusting the black level to correspond to VRB, the entire range of the ADC can be used.

If the offset of the CIS output is greater than 500 mV an external reference can be applied to VDCEXT. The external reference can be used to adjust for large offsets only when the internal mode is configured through the serial port.

Since the offset DAC adjustment is done before the gain stage, it is gain-dependent. For example, if the gain needs to be changed between lines (red to blue, etc.), the offset is calibrated before the signal passes through the PGA.

PGA (Programmable Gain Amplifier) DAC

The gain of the input waveform is controlled by a 6-Bit PGA. The PGA is used along with the offset DAC for the purpose of using the entire range of the ADC. The PGA has a linear gain from 1 to 10. Figure 20 is a plot of the transfer curve for the PGA gain.



Figure 20. Transfer Curve for the 6-Bit PGA

After the signal is level shifted to correspond with the bottom ladder reference voltage, the system can be calibrated such that a white video pixel can represent the top ladder reference voltage to the ADC. This allows for a full scale conversion maximizing the resolution of the ADC.

Analog to Digital Converter

The ADC is a 12-Bit, 10 MSPS analog-to-digital converter for high speed and high accuracy. The ADC uses a subranging architecture to maintain low power consumption at high conversion rates. The output of the ADC is on 8-bit databus. The 8-bit databus supports 6x6 or 8x4 output data. ADCCLK samples the input on its falling edge. After the input is sampled, the MSB is latched to the output drivers. On the rising edge of the ADCCLK, the LSB is latched to the output drivers. The output needs to be demultiplexed with external circuitry or a digital ASIC. There is an 8 clock cycle latency (Config 00, 11) or 6 pixel count latency (Config 01, 10) for the analog-to-digital converter.

The V_{RT} and V_{RB} reference voltages for the ADC are generated internally, unless the external V_{RT} is selected. In the external V_{RT} mode, the V_{RT} voltage is set through the VREF+ pin. This allows the user to select the dynamic range of the ADC.

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Serial Load Control Registers

The serial load registers are controlled by a three wire serial interface through the bi-directional parallel port to reduce the pin count of this device. When SYNCH is set to high, the output bus is tri-stated and the serial interface is activated. DB7/LD, DB5/SCLK and DB6/ SDATA are the three input signals that control this process. The DB7/LD signal is set low to initiate the loading of the internal registers.

There are internal registers that are accessed via an 11bit data string. Data is shifted in on the rising edge of SCLK and loaded to the registers on the rising edge of LD. The data on pin DB6/SDATA is latched automatically after eleven DB5/SCLKs have been counted. If eleven clocks are not present on DB5/SCLK before the DB7/LD signal returns high, no data will be loaded into the internal registers. If more than 11 clocks are present on DB5/SCLK, the additional clocks will be ignored. The data corresponding to the first eleven DB5/SCLKs will be loaded only. The first three MSBs choose which internal register will be selected. The remaining 8 LSBs contain the data needed for programming the internal register for a particular configuration.

Power-Up State of the Internal Registers

The control register settings upon initial power-up are for CIS, DC Coupled configuration (V_{RT} is set to internal, Input DC Reference=AGND and the input to the ADC is selected through the RED channel). Gain is unity and Offset is set to zero. The test modes are disabled in the power-up state.



Figure 21. Write Timing





Output Bus Format

ADC Output -> DO11(MSB):DO0(LSB)

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
MSB	DO11	DO10	DO9	DO8	DO7	DO6	Х	Х
LSB	DO5	DO4	DO3	DO2	DO1	DO0	Х	Х

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
MSB	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4
LSB	DO3	DO2	DO1	DO0	Х	Х	Х	Х

Table 9.	8 MSB + 4 LSB	Output Bus Format
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Control Registers

Function (Register S2/S1/S0)	D7	D6	D5	D4	D3	D2	D1	D0	Power-up State (Note 1)
Red Gain (000)	G5 (MSB)	G4	G3	G2	G1	G0 (LSB)	х	х	000000XX
Red Offset (001)	O7 (MSB)	O6	O5	O4	O3	O2	O1	O0 (LSB)	01000000
Grn Gain (010)	G5 (MSB)	G4	G3	G2	G1	G0 (LSB)	х	х	000000XX
Grn Offset (011)	O7 (MSB)	O6	O5	O4	O3	O2	O1	O0 (LSB)	01000000
Blu Gain (100)	G5 (MSB)	G4	G3	G2	G1	G0 (LSB)	х	х	000000XX
Blu Offset (101)	O7 (MSB)	O6	O5	O4	O3	O2	O1	O0 (LSB)	01000000
Mode (110)	POWER DOWN			INPUTDC REFERENCE (V _{DCREF})	DC/AC	SIGNAL POLARITY	CONFIG	GNAL SURATION	00000000
	0: NORMAL 1: POWER DOWN	0: NO RESET 1:RESET (REGISTERS ARE RESETTO POWER-UP STATES)	0: INTERNAL 1: EXTERNAL	0: INTERNAL (V _{DCREF} =AGND) 1: EXTERNAL (V _{DCREF} =V _{DCEXT})	0: DC 1: AC	0: Non- Inverted (CIS) 1: Inverted (CCD/CIS)	RED inpu 01: Singl REL RED/C gain/off pixel- 10: Triple RED/C input/gain/ pixel- 11: Triple RED/C input/gain/	e-Channel t/gain/offset e-Channel) input RN/BLU set cycle by-pixel e-Channel iRN/BLU offset cycle by-pixel e-Channel RN/BLU offset cycle by-line	
Mode &Test (111)	OUTPUT BUS CONTROL	OUTPUT DISABLE	OFFSET DAC RANGE	INTERNALCIS REFERENCE CIRCUIT	TEST4	TEST3	TEST2	TEST1	00000000
	0: 6 MSB + 6 LSB 1: 8 MSB + 4 LSB	0:OUTPUTS ENABLED 1:OUTPUTS DISABLED	0:-200mV to +600mV 1:-400mV to +400mV	0:NORMAL 1:REFERENCE CIRCUIT ENABLED	0: TEST4 DISABLED 1: OUTPUT OF BUFFER TIED TO BLU	0: TEST3 DISABLED 1: OUTPUT OF PGA TIED TO VDCEXT	0: TEST2 DISABLED 1: INPUT OF ADC TIED TO GRN	0:NORMAL 1: TEST1 ENABLED	

Note : These are the control register settings upon initial power-up. The previous register settings are retained following a logic power-down initiated by the power down bit except the signal configuration. When de-selecting the power down bit (D7 = 0, Normal), the signal configuration (D5 and D0) has to be reprogrammed.

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20 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00





	INC	HES	MILLIN	IETERS
SYMBOL	MIN	MAX	MIN	MAX
А	0.093	0.104	2.35	2.65
A ₁	0.004	0.012	0.10	0.30
В	0.013	0.020	0.33	0.51
С	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
Е	0.291	0.299	7.40	7.60
е	0.0	50 BSC	1.2	7 BSC
н	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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20 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP) Rev. 2.00

D 11 20 н С H С A_2 Seating Plane α → | ← -В е A,

L

	INC	HES	MILLIN	IETERS
SYMBOL	MIN	MAX	MIN	MAX
A	0.067	0.079	1.70	2.00
A1	0.002	0.006	0.05	0.15
A2	0.065	0.073	1.65	1.85
В	0.009	0.015	0.22	0.38
С	0.004	0.010	0.09	0.25
D	0.272	0.296	6.90	7.50
E	0.197	0.221	5.00	5.60
е	0.025	6 BSC	0.65	BSC
Н	0.292	0.323	7.40	8.20
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

Note: The control dimension is the inch column







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