

74LVT240

3.3 V Octal inverting buffer/line driver; 3-state

Rev. 4 — 28 July 2021

Product data sheet

1. General description

The 74LVT240 is an 8-bit inverting buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1 \overline{OE} and 2 \overline{OE}), each controlling four of the 3-state outputs. A HIGH on n \overline{OE} causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs.

2. Features and benefits

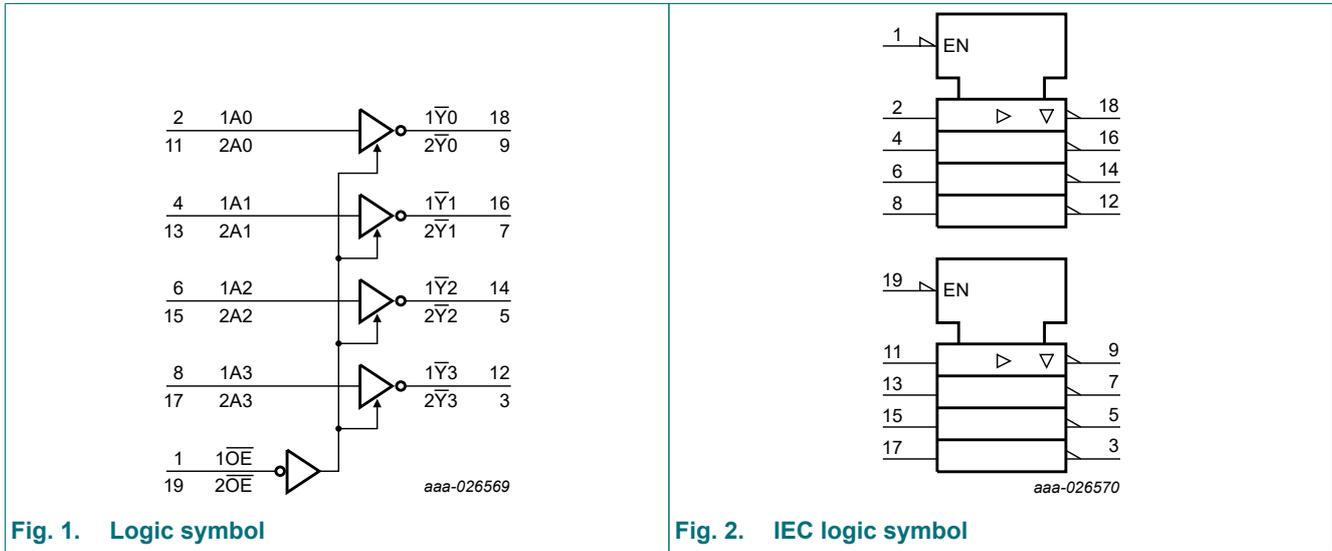
- Octal bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standard JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - MIL STD 883 method 3015: exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

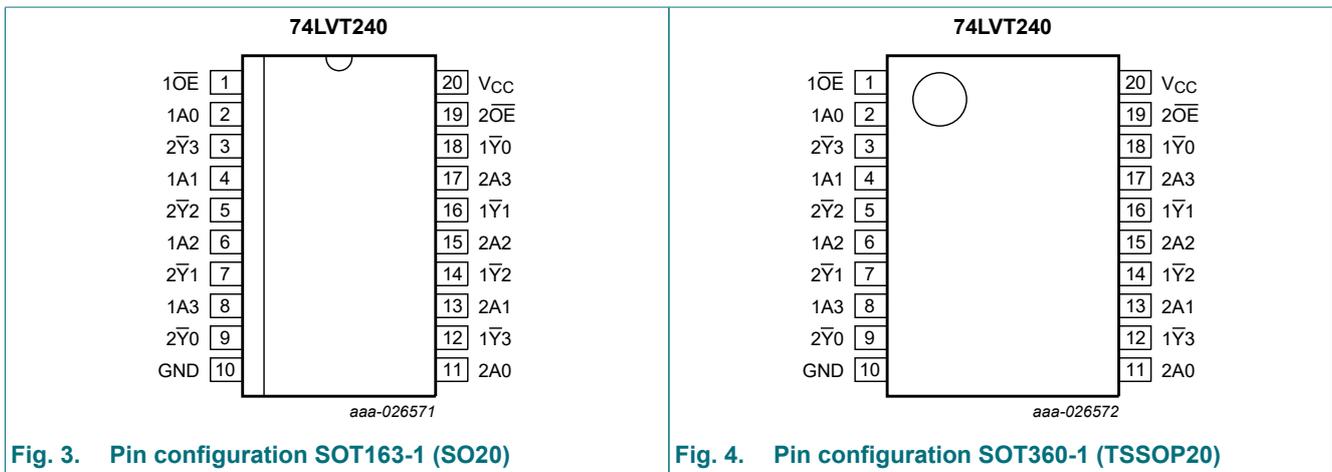
Type number	Package			Version
	Temperature range	Name	Description	
74LVT240D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT240PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	bus output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	bus output
VCC	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs		Outputs
nOE	nAn	nYn
L	L	H
L	H	L
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		[1] -0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH state	[1] -0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[2] -	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
I_{OH}	HIGH-level output current		-32	-	mA
I_{OL}	LOW-level output current		-	32	mA
		current duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	64	mA
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.9	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2	V _{CC} - 0.1	-	V
		V _{CC} = 2.7 V; I _{OH} = -8 mA	2.4	2.5	-	V
		V _{CC} = 3.0 V; I _{OH} = -32 mA	2.0	2.2	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 μA		0.1	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	all input pins				
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	1	10	μA
		control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	±0.1	±1	μA
		data pins [2]				
		V _{CC} = 3.6 V; V _I = V _{CC}	-	0.1	1	μA
		V _{CC} = 3.6 V; V _I = 0 V	-5	-1	-	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	1	±100	μA
I _{BHL}	bus hold LOW current	V _{CC} = 3.0 V; V _I = 0.8 V	75	150	-	μA
I _{BHH}	bus hold HIGH current	V _{CC} = 3.0 V; V _I = 2.0 V	-	-150	-75	μA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [3]	500	-	-	μA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [3]	-	-	-500	μA
I _{CEX}	output high leakage current	n \bar{Y} n output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V	-	60	125	μA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n $\bar{O}\bar{E}$ = don't care [4]	-	±1	±100	μA
I _{OZ}	OFF-state output current	V _{CC} = 3.6 V; V _O = 3.0 V	-	1	5	μA
		V _{CC} = 3.6 V; V _O = 0.5 V	-5	-1	-	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A				
		outputs HIGH	-	0.12	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled [5]	-	0.12	0.19	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 3.0 V to 3.6 V; one input = V _{CC} - 0.6 V; other inputs at V _{CC} or GND [6]	-	0.1	0.2	mA

3.3 V Octal inverting buffer/line driver; 3-state

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
C _I	input capacitance	V _I = 0 V or 3.0 V	-	4	-	pF
C _O	output capacitance	outputs disabled; V _O = 0 V or 3.0 V	-	8	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.

From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 ms is permitted. This parameter is valid for T_{amb} = +25 °C only.

[5] I_{CC} with the outputs disabled is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

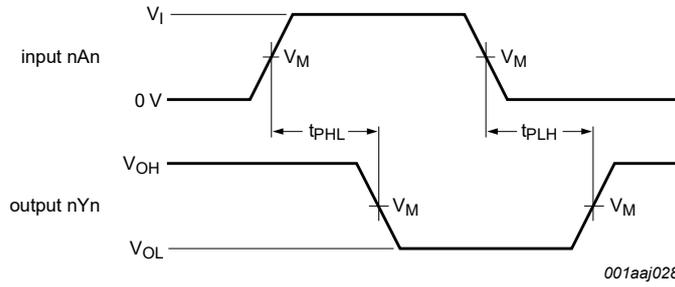
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t _{PLH}	LOW to HIGH propagation delay	nAn to n \bar{Y} n; see Fig. 5				
		V _{CC} = 2.7 V	-	-	5.2	ns
		V _{CC} = 3.3 V ± 0.3 V	1.0	2.5	4.3	ns
t _{PHL}	HIGH to LOW propagation delay	nAn to n \bar{Y} n; see Fig. 5				
		V _{CC} = 2.7 V	-	-	5.0	ns
		V _{CC} = 3.3 V ± 0.3 V	1.0	2.5	4.3	ns
t _{PZH}	OFF-state to HIGH propagation delay	n $\bar{O}\bar{E}$ to n \bar{Y} n; see Fig. 6				
		V _{CC} = 2.7 V	-	-	6.3	ns
		V _{CC} = 3.3 V ± 0.3 V	1.0	3.7	5.2	ns
t _{PZL}	OFF-state to LOW propagation delay	n $\bar{O}\bar{E}$ to n \bar{Y} n; see Fig. 6				
		V _{CC} = 2.7 V	-	-	6.7	ns
		V _{CC} = 3.3 V ± 0.3 V	1.0	3.1	5.2	ns
t _{PHZ}	HIGH to OFF-state propagation delay	n $\bar{O}\bar{E}$ to n \bar{Y} n; see Fig. 6				
		V _{CC} = 2.7 V	-	-	6.3	ns
		V _{CC} = 3.3 V ± 0.3 V	2.0	3.4	5.6	ns
t _{PLZ}	LOW to OFF-state propagation delay	n $\bar{O}\bar{E}$ to n \bar{Y} n; see Fig. 6				
		V _{CC} = 2.7 V	-	-	5.6	ns
		V _{CC} = 3.3 V ± 0.3 V	1.6	3.2	5.1	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

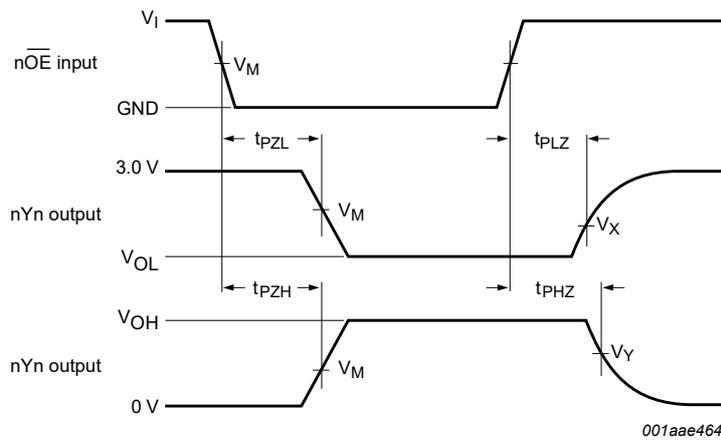
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Input (nAn) to output (nYn) propagation delays



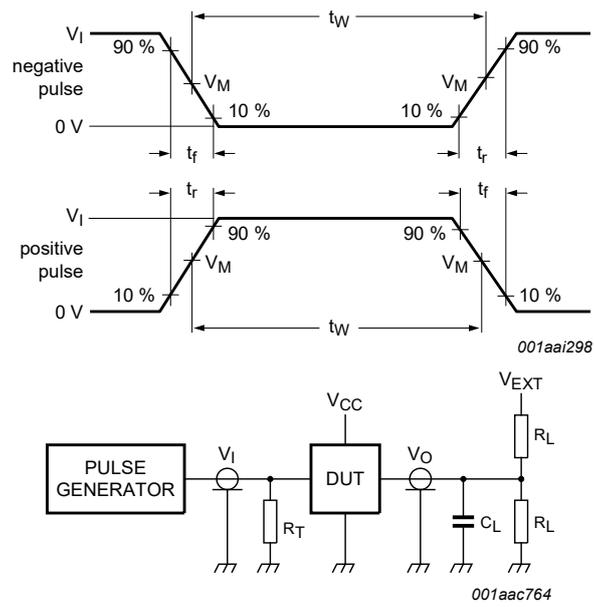
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

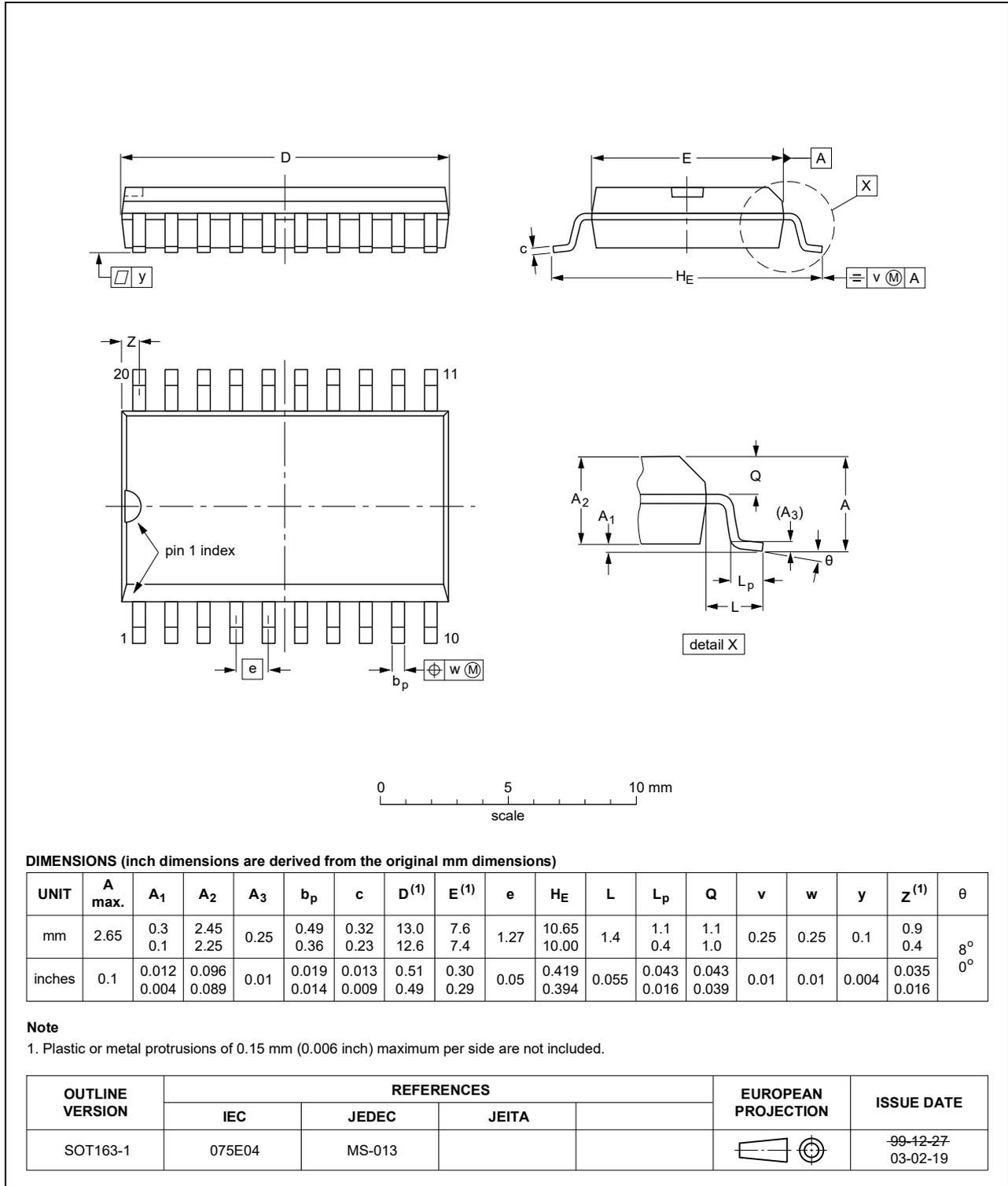


Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

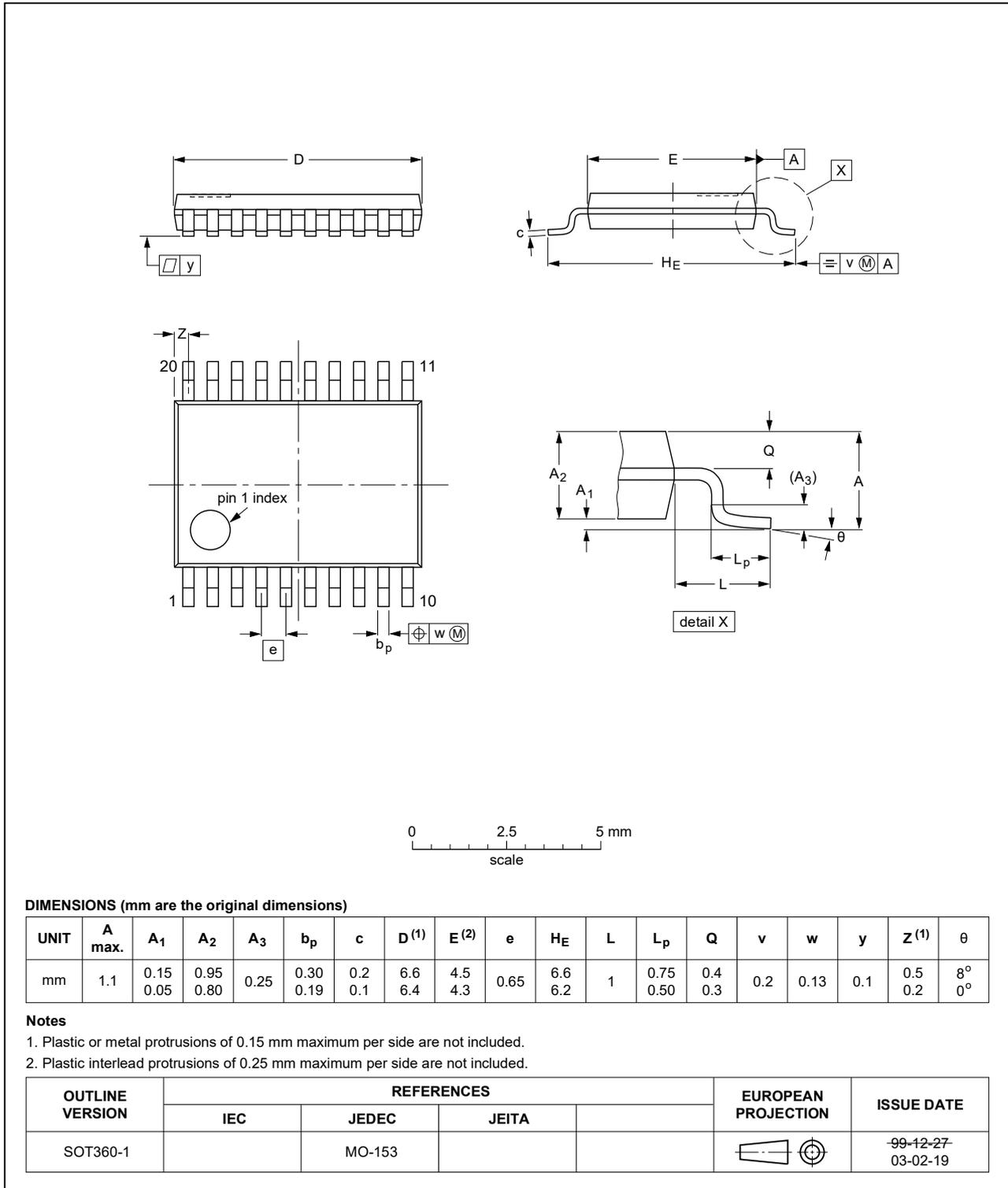


Fig. 9. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT240 v.4	20210728	Product data sheet	-	74LVT240 v.3
Modifications:	<ul style="list-style-type: none"> Type number 74LVT240DB (SOT339-1/SSOP20) removed. Section 1 and Section 2 updated. Section 7: Derating values for P_{tot} total power dissipation removed. 			
74LVT240 v.3	20170410	Product data sheet	-	74LVT240 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVT240 v.2	19980219	Product specification	-	74LVT240 v.1
74LVT240 v.1	19940516	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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