

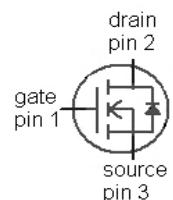
OptiMOS®2 Power-Transistor

Features

- N-channel, normal level
- Excellent gate charge $\times R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Ideal for high-frequency switching and synchronous rectification

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	11.8	mΩ
I_D	75	A



Type	IPS118N10N G
Package	PG-T0251-3
Marking	118N10N

Maximum ratings, at $T_j=25$ °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_c=25$ °C	75	A
		$T_c=100$ °C	53	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_c=25$ °C	300	
Avalanche energy, single pulse	E_{AS}	$I_D=75$ A, $R_{GS}=25$ Ω	120	mJ
Gate source voltage ³⁾	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_c=25$ °C	125	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

¹⁾J-STD20 and JESD22

²⁾ see figure 3

³⁾ $T_{jmax}=150$ °C and duty cycle D=0.01 for $V_{gs}<-5$ V

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.2	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ⁴⁾	-	-	40	

Electrical characteristics, at $T_j=25$ °C, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0$ V, $I_D=1$ mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=83$ µA	2	3	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=80$ V, $V_{GS}=0$ V, $T_j=25$ °C	-	0.1	1	µA
		$V_{DS}=80$ V, $V_{GS}=0$ V, $T_j=125$ °C	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20$ V, $V_{DS}=0$ V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10$ V, $I_D=75$ A	-	9.5	11.8	mΩ
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=75$ A	41	81	-	s

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0 \text{ V}, V_{DS}=50 \text{ V}, f=1 \text{ MHz}$	-	3250	4320	pF
Output capacitance	C_{oss}		-	489	650	
Reverse transfer capacitance	C_{rss}		-	29	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50 \text{ V}, V_{GS}=10 \text{ V}, I_D=35 \text{ A}, R_G=1.6 \Omega$	-	17	-	ns
Rise time	t_r		-	21	-	
Turn-off delay time	$t_{d(off)}$		-	32	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=50 \text{ V}, I_D=75 \text{ A}, V_{GS}=0 \text{ to } 10 \text{ V}$	-	18	-	nC
Gate to drain charge	Q_{gd}		-	12	-	
Switching charge	Q_{sw}		-	20	-	
Gate charge total	Q_g		-	49	65	
Gate plateau voltage	$V_{plateau}$		-	5.6	-	V
Output charge	Q_{oss}	$V_{DD}=50 \text{ V}, V_{GS}=0 \text{ V}$	-	52	69	nC

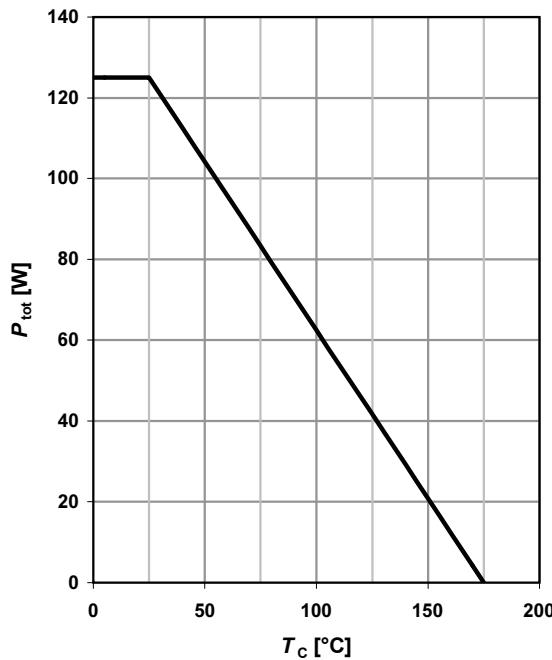
Reverse Diode

Diode continuous forward current	I_s	$T_c=25 \text{ }^\circ\text{C}$	-	-	75	A
Diode pulse current	$I_{s,pulse}$		-	-	300	
Diode forward voltage	V_{SD}	$V_{GS}=0 \text{ V}, I_F=75 \text{ A}, T_j=25 \text{ }^\circ\text{C}$	-	1	1.2	V
Reverse recovery time	t_{rr}	$V_R=50 \text{ V}, I_F=I_s, di_F/dt=100 \text{ A}/\mu\text{s}$	-	105	-	ns
Reverse recovery charge	Q_{rr}		-	255	-	nC

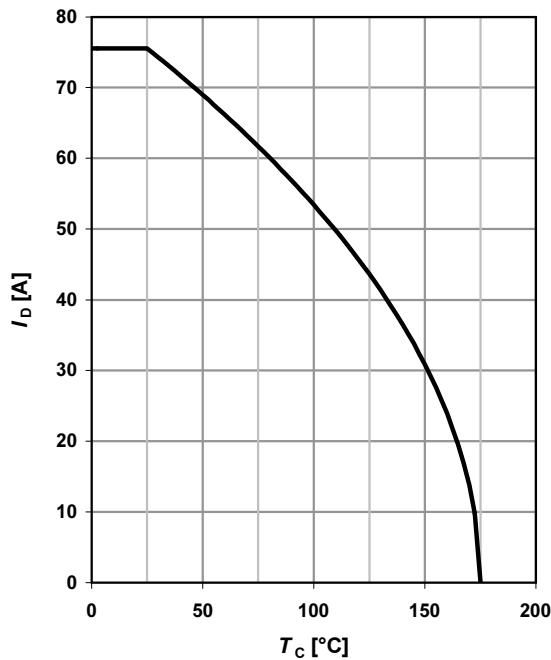
⁵⁾ See figure 16 for gate charge parameter definition

1 Power dissipation

$$P_{\text{tot}} = f(T_c)$$

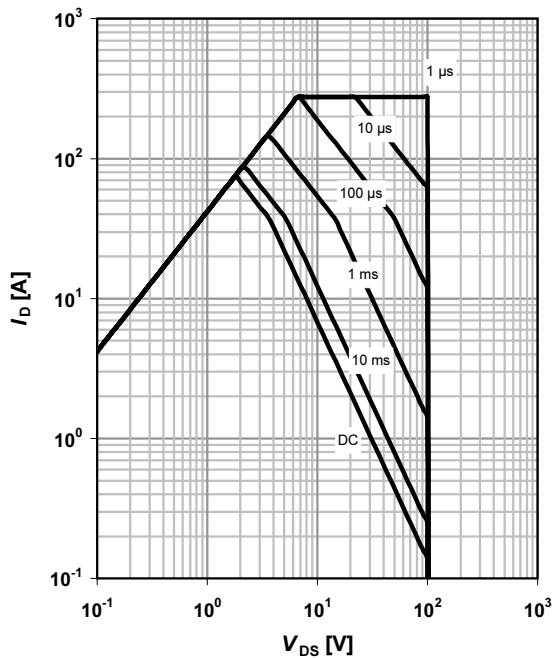

2 Drain current

$$I_D = f(T_c); V_{GS} \geq 10 \text{ V}$$


3 Safe operating area

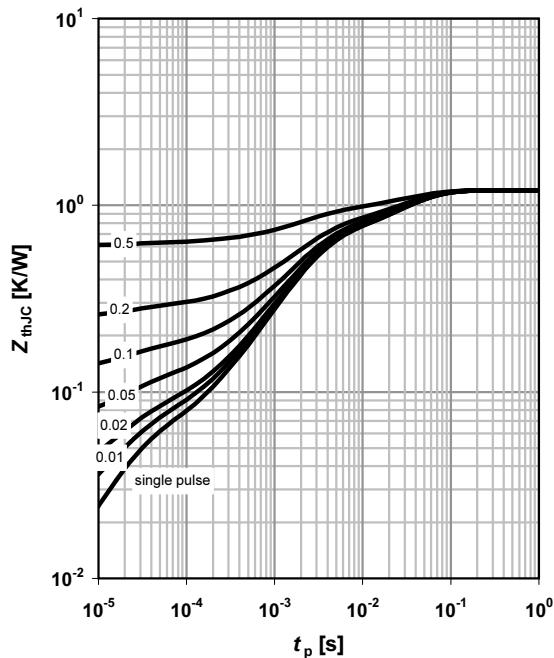
$$I_D = f(V_{DS}); T_c = 25 \text{ }^{\circ}\text{C}; D = 0$$

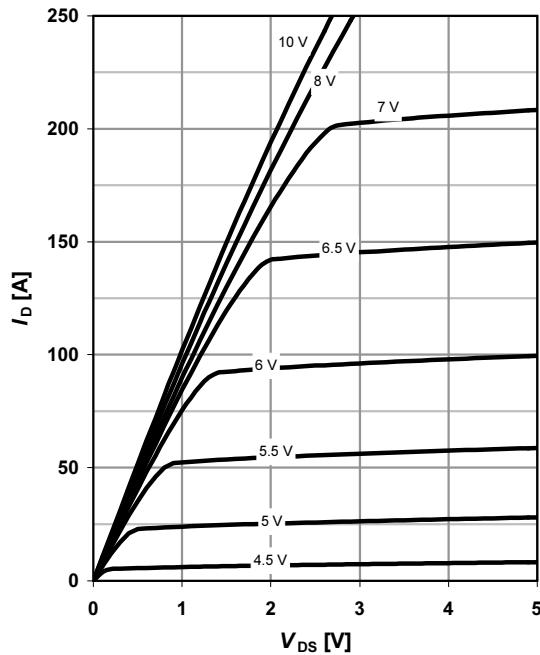
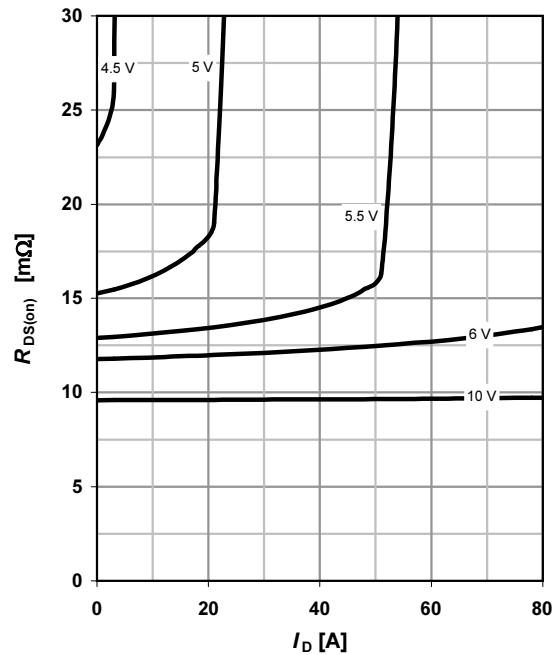
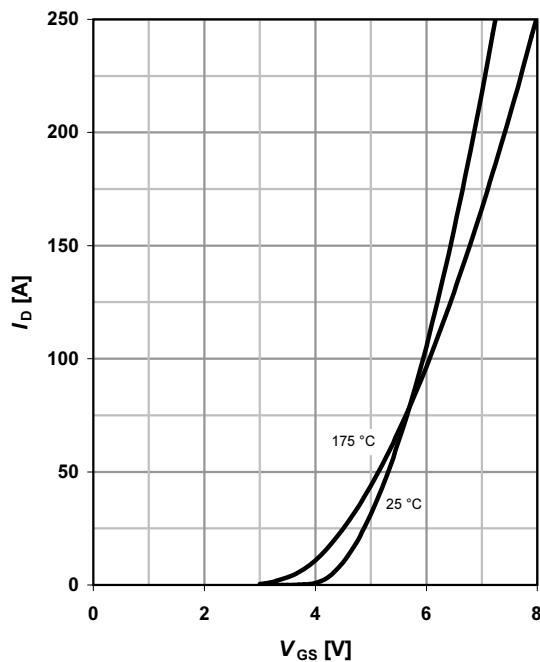
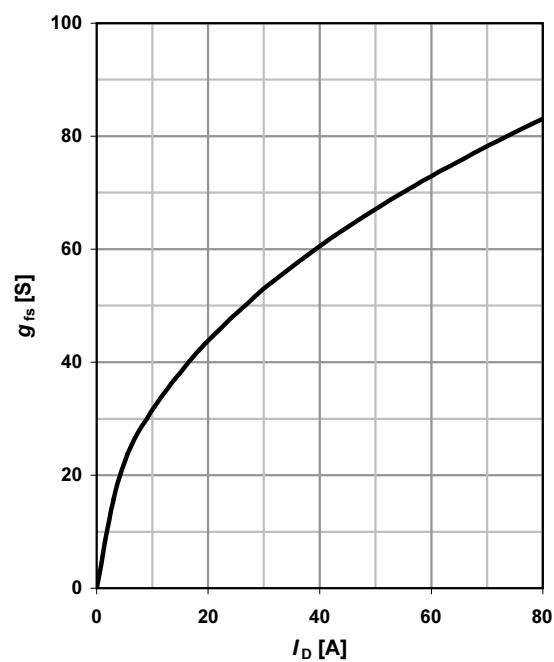
parameter: t_p

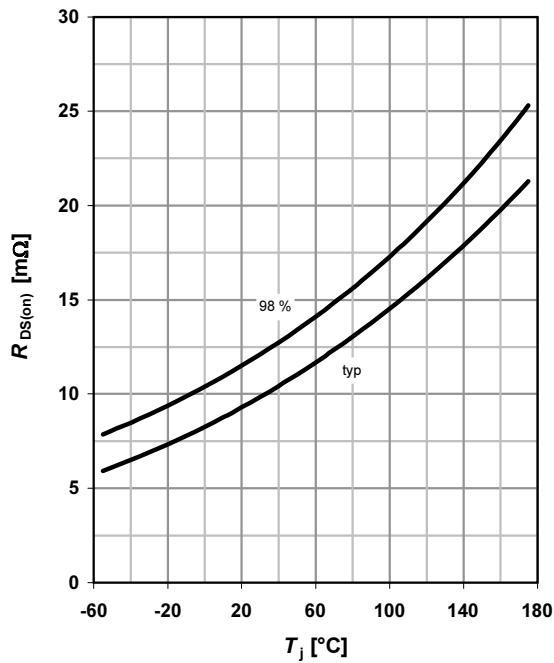

4 Max. transient thermal impedance

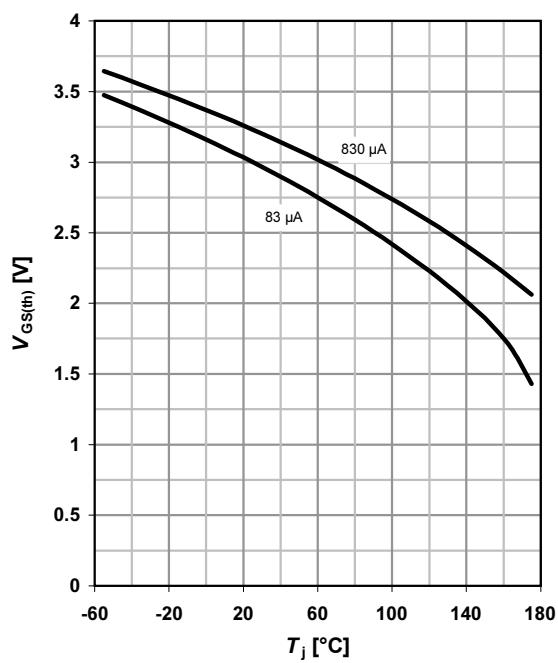
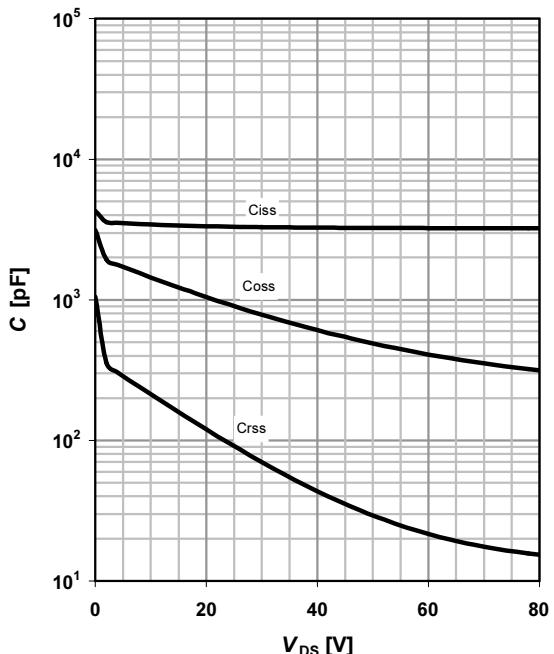
$$Z_{\text{thJC}} = f(t_p)$$

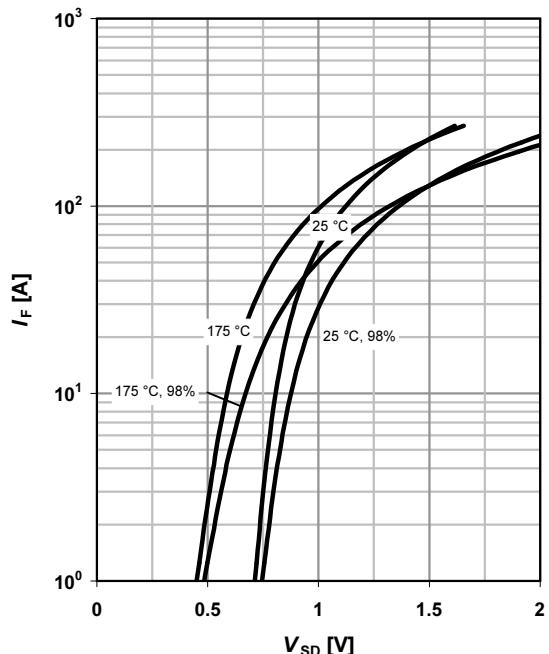
parameter: $D = t_p/T$



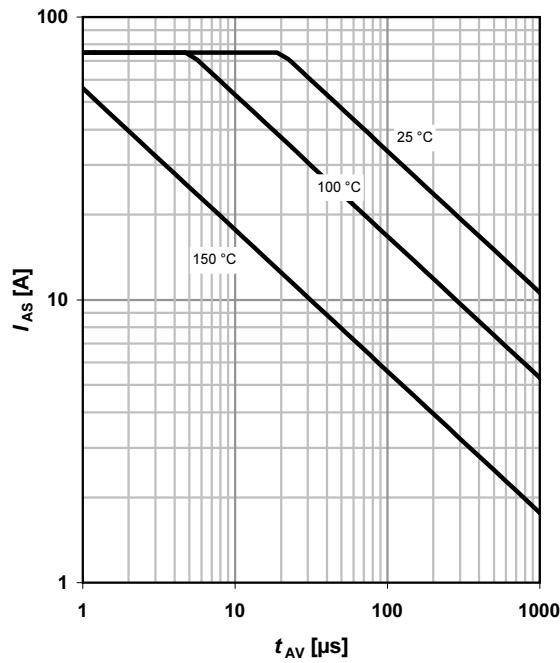
5 Typ. output characteristics
 $I_D = f(V_{DS})$; $T_j = 25 \text{ }^\circ\text{C}$
parameter: V_{GS} 
6 Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D)$; $T_j = 25 \text{ }^\circ\text{C}$
parameter: V_{GS} 
7 Typ. transfer characteristics
 $I_D = f(V_{GS})$; $|V_{DS}| > 2|I_D|R_{DS(on)max}$
parameter: T_j 
8 Typ. forward transconductance
 $g_{fs} = f(I_D)$; $T_j = 25 \text{ }^\circ\text{C}$


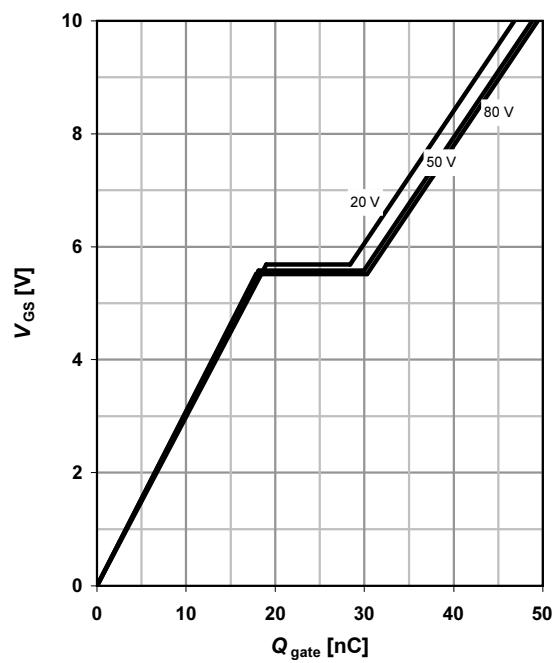
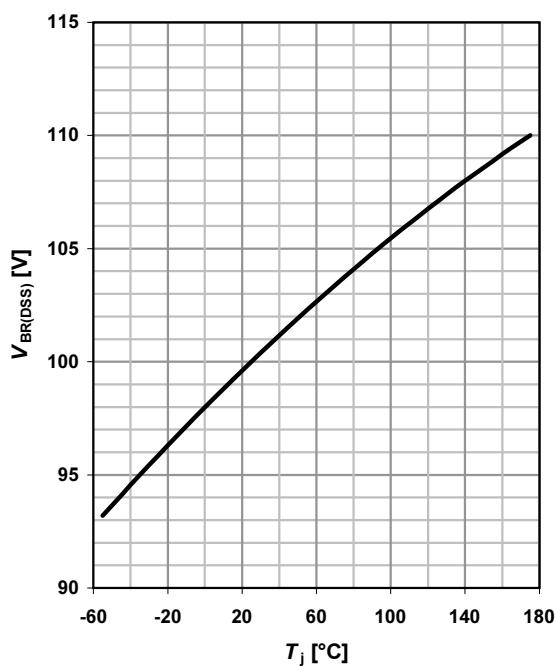
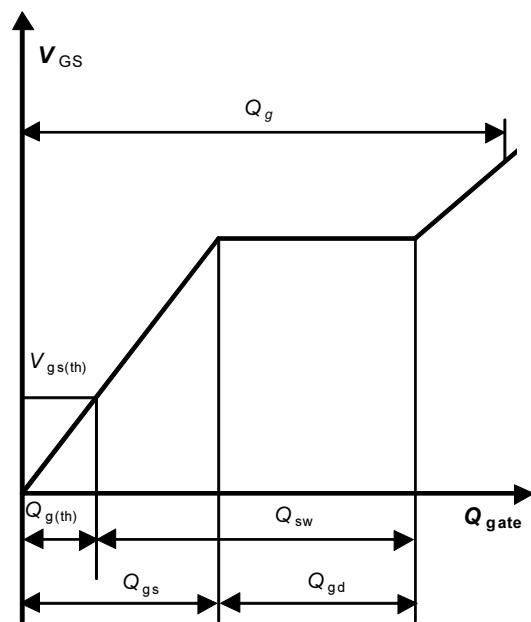
9 Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = 75 \text{ A}; V_{GS} = 10 \text{ V}$

10 Typ. gate threshold voltage
 $V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

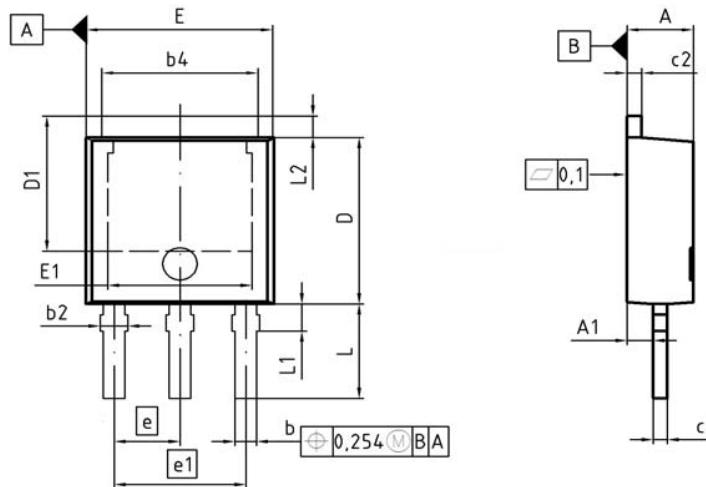
 parameter: I_D

11 Typ. capacitances
 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

12 Forward characteristics of reverse diode
 $I_F = f(V_{SD})$

 parameter: T_j


13 Avalanche characteristics
 $I_{AS} = f(t_{AV})$; $R_{GS} = 25 \Omega$

parameter: $T_{j(\text{start})}$

14 Typ. gate charge
 $V_{GS} = f(Q_{\text{gate}})$; $I_D = 75 \text{ A pulsed}$

parameter: V_{DD}

15 Drain-source breakdown voltage
 $V_{BR(DSS)} = f(T_j)$; $I_D = 1 \text{ mA}$

16 Gate charge waveforms


PG-T0251-3: Outline


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.44	0.198	0.214
E	6.35	6.73	0.250	0.265
E1	4.90	5.10	0.193	0.201
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.40	3.60	0.134	0.142
L1	0.90	1.10	0.035	0.043
L2	0.90	1.10	0.035	0.043

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