

UG387: Si5392 Evaluation Board User's Guide

This user guide is intended to be used with the Si5392 evaluation boards and can be used to evaluate the performance of the dual-output Si5392 jitter attenuating clocks. In this document Si5392 EVB refers to both the Si5392J-A-EVB and the Si5392E-A-EVB. The Si5392J-A-EVB and Si5392E-A-EVB both have integrated references and so do not require an external reference. The "J" version is the any-frequency, any-format version and the "E" is the version calibrated for specific 56G SerDes frequencies. There is no external reference version of the Si5392 evaluation board available. To evaluate the Si5392 with external reference, the Si5394A-A-EVB is recommended. The device grade and revision is distinguished by a white 1 inch x 0.187 inch label with the text "Si5392E-A-EVB" installed in the lower left hand corner of the board. (For ordering purposes only, the terms "EB" and "EVB" refer to the board and the kit respectively. For the purpose of this document, the terms are synonymous in context.)



KEY FEATURES

- Si5392J-A-EVB for evaluating internal reference versions Si5392J/K/L/M
- Si5392E-A-EVB for evaluating internal reference (precision grade)
- Powered from USB port or external power supply.
- ClockBuilder[®] Pro (CBPro) GUI programmable VDD supply allows device to operate from 3.3, 2.5, or 1.8 V.
- CBPro GUI programmable VDDO supplies allow each of the 2 outputs to have its own power supply voltage selectable from 3.3, 2.5, or 1.8 V.
- CBPro GUI allows control and measurement of voltage, current, and power of VDD and all VDDO supplies.
- Status LEDs for power supplies and control/ status signals of Si5392.
- SMA connectors for input clocks and output clocks

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UG387: Si5392 Evaluation Board User's Guide • Functional Block Diagram

1. Functional Block Diagram

Below is a functional block diagram of the Si5392J-A-EVB and Si5392E-A-EVB. This evaluation board can be connected to a PC via the main USB connector for programming, control, and monitoring. See 3. Quick Start or section 9. Installing ClockBuilder Pro Desktop Softwarefor more information.



Figure 1.1. Si5392 EVB Functional Block Diagram

UG387: Si5392 Evaluation Board User's Guide • Si5392 EVB Support Documentation and ClockBuilder Pro Software

2. Si5392 EVB Support Documentation and ClockBuilder Pro Software

All Si5392 EVB schematics, BOMs, User's Guides, and software can be found online: www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

UG387: Si5392 Evaluation Board User's Guide • Quick Start

3. Quick Start

- 1. Install ClockBuilder Pro desktop software from http://www.silabs.com/CBPro.
- 2. Connect a USB cable from Si5392 EVB to the PC where the software was installed.
- 3. Confirm jumpers are installed as shown in Table 4.1 Si5392 EVB Jumper Defaults* on page 6.
- 4. Launch the ClockBuilder Pro Software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5392 EVB.
- 6. Find the Si5392 data sheet:https://www.silabs.com/documents/public/data-sheets/si5395-94-92-a-datasheet.pdf

4. Jumper Defaults

Table 4.1. Si5392 EVB Jumper Defaults*

Location	Туре	l = Installed 0 = Open	Location	Туре	I = Installed 0 = Open
JP1	2 pin	I			
JP2	2 pin	1			
JP3	2 pin	1			
JP4	2 pin	I			
JP5	3 pin	1 to 2 (USB)			
JP13	2 pin	0			
			J17	5x2 Hdr	All 5 installed

5. Status LEDs

Location	Silkscreen	Color	Status Function Indication
D5	INTRB	Blue	DUT Interrupt
D7	LOLB	Blue	DUT Loss of Lock
D8	LOSXAXBB*	Blue	DUT Loss of Reference
D14	LOS0B	Blue	IN0 Loss of Signal indicator
D15	LOS1B	Blue	IN1 Loss of Signal indicator
D16	LOS3B	Blue	IN3 Loss of Signal indicator
D17	LOS2B	Blue	IN2 Loss of Signal indicator
D11	+5V MAIN	Green	Main USB +5V present
D12	READY	Green	MCU Ready
D13	BUSY	Green	MCU Busy

Table 5.1. Si5392 EVB Status LEDs

D5, D7, D8, D14, D15, D16, and D17 are status LEDs indicating the device alarms currently asserted. D11 is illuminated when USB +5 V supply voltage is present. D12 and D13 are status LEDs showing on-board MCU activity.



Figure 5.1. Status LEDs

UG387: Si5392 Evaluation Board User's Guide • Clock Input Circuits (INx/INxB)

6. Clock Input Circuits (INx/INxB)

The Si5392 EVB has eight SMA connectors (IN0/IN0B–IN3/IN3B) for receiving external clock signals. All input clocks are terminated as shown in Figure 6.1 Input Clock Termination Circuit on page 8 below. Note input clocks are ac-coupled and 50 Ω terminated. This represents four differential input clock pairs. Single-ended clocks can be used by appropriately driving one side of the differential pair with a single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5392 data sheet. Typically a 0.1 μ F dc block is sufficient, however, 10 μ F may be needed for lower input frequencies. Note that the EVB is populated with both dc block capacitor values.



Figure 6.1. Input Clock Termination Circuit

UG387: Si5392 Evaluation Board User's Guide • Clock Output Circuits (OUTx/OUTxB)

7. Clock Output Circuits (OUTx/OUTxB)

Each of the two output drivers (two differential pairs) is ac-coupled to its respective SMA connector. The output clock termination circuit is shown in Figure 7.1 Output Clock Termination Circuit on page 9 below. The output signal will have no dc bias. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5392 EVB provides an L-network at OUT1/OUT1B output pins for optional output termination resistors. Note that components with schematic "NI" designation are not normally populated.



Figure 7.1. Output Clock Termination Circuit

UG387: Si5392 Evaluation Board User's Guide • External Reference Clock (XA/XB) Not Supported

8. External Reference Clock (XA/XB) Not Supported

The Si5392J-A-EVB and Si5392E-A-EVB both do not support an external reference clock on XA/XB. The layout for the external XTAL is on the board, but the EVBs for this part are embedded XTAL versions only and therefore this circuit should remain disconnected and unused.



Figure 8.1. External Reference Clock Termination Circuit

UG387: Si5392 Evaluation Board User's Guide • Installing ClockBuilder Pro Desktop Software

9. Installing ClockBuilder Pro Desktop Software

To install the CBOPro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/CBPro and download ClockBuilder Pro software.

Installation instructions and User's Guide for ClockBuilder Pro can be found at the download link shown above. Please follow the instructions as indicated.

UG387: Si5392 Evaluation Board User's Guide • Using the Si5392 EVB

10. Using the Si5392 EVB

10.1 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown below.



Figure 10.1. EVB Connection Diagram

10.2 Overview of ClockBuilder Pro Applications

Note: The following instructions and screen captures may vary slightly depending on your version of ClockBuilder Pro. The ClockBuilder Pro installer will install two main applications:



Figure 10.2. Application #1: ClockBuilder Pro Wizard

Use the CBPro Wizard to:

- Create a new design
- · Review or edit an existing design
- · Export: create in-system programming

CB Si5392	E Rev A E	EVB - ClockBuilder Pro	D								– 🗆 X
File Help)										
Info D	UT SPI	DUT Settings Editor	DUT Register Editor	Phase INC/DEC	Regulators	All Voltages	GPIO	Status Registers		-	Control Registers
			Voltage	Current	Power						Soft Reset and Calibration
	VDI	D 1.80V 📳	On 1.767 V	121 mA	214 mW	Read					SOFT_RST_ALL
	VDD	A 3.30V	On 3.291 V	117 mA	385 mW	Read					SOFT_RST
	VDDO		Off 0 V	0 mA	0 mW						Hard Reset, Sync, & Power Down
	VDDO	1 1.80V	Off 0 V	0 mA	0 mW	Read					HARD_RST
(*	') VDDO	2 3.30V	On 3.285 V	7 mA	23 mW	Read					SYNC
(**) VDDO	3 3.30V 📳	On 3.323 V	7 mA	23 mW	Read					
			Total	252 mA	0.645 W	Read All	Ē				PDN: 0
All Ou	utput	Select Voltage	🔽	252 MA	0.045 W	Incode All					Frequency Adjust
Sup	plies	Power On P	Power Off Co	mpare Design Es	timates to Me	asurements					FINC
* Co	os to Dir	1 29 as VDDS					_				FDEC
		1 34 as VDDS									FDEC
Log											
Filtered		Auto Scroll: On 🗖	Insert Marker	Clear Cop	y to Clipboard	d Pause					
					, to enpoent					_	
Timestar		ource Message									
11:36:07	.629 E	_	Set_Voltage_Mux(settin	-							
11:36:07	.671 E		70 msec for voltage MU							- 11	
11:36:07	.743 E	VB Starting I	Read_ADC(num_sample	es=5)							
11:36:07	.747 E	VB finished	Read_ADC(num_sample	es=5) => 745.6							
11:36:07	.747 E	VB finished	Measure_Voltage(chani	nel=VDD_3_PIN) :	=> 3.528						
11:36:07	.747 E	VB finished 0.023W	Measure_Regulator(reg	ulator_id=VDD_3) => Voltage_	Reg: 3.323V, \	oltage_	Pin: 3.528V, Currer	t: 0.007A, Power:	-	
EVB Firmwa	are 1.6 [Device: Si5392 DUT I	Mode: SPI 4-Wire; FW Lo	w-Level Command	s					Clo	kBuilder Pro v2.30.1 [2019-02-19

Figure 10.3. Application #2: EVB GUI

Use the EVB GUI to:

- · Download configuration to EVB's DUT (Si5392)
- · Control the EVB's regulators
- · Monitor voltage, current, power on the EVB

10.3 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CBPro and the Si5392 EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- · Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Testing a User-Created Device Configuration
- Each is described in more detail in the following sections.

10.4 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



Figure 10.4. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CBPro automatically detects the EVB and device type.



Figure 10.5. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.



Figure 10.6. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5392 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.



Figure 10.7. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.



Figure 10.8. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the values defined in the device's default CBPro project file created by Silicon Labs, as shown below.

					_						
nfo Dl	UT SPI DU	UT Settings Editor	DUT Register E	ditor Phase INC/DEC	Regulators	All Voltages	GPIO	Status Registers		- Co	ontrol Registers
			Vo	ltage Current	Power					S	oft Reset and Calibratio
	VDD	1.80V	Dn 1.7	790 V 121 mA	217 mW	Read					SOFT_RST_ALL
	VDDA	3.30V 🔲 🖸	On 3.2	286 V 120 mA	394 mW	Read	-				SOFT_RST
	l			508 V 16 mA	40 mW						Hard Reset, Sync, &
	l										Power Down
	VDDO1	2.50V 🔽 🖸	On 2.4	195 V 16 mA	40 mW	Read					HARD_RST
(*)) VDDO2	3.30V	Dn 3.2	280 V 7 mA	23 mW	Read					
(**)	VDDO3	3.30V 📳 🚺	Dn 3.3	320 V 7 mA	23 mW	Read					
				T-1-1 007 1	0.707.00	Read All	n i				PDN: 0
All Ou	utput 🔽	Select Voltage		Total 287 mA	0.737 W	Read All					Frequency Adjust
Sup	plies 🗌	Power On Po	wer Off	Compare Design E	stimates to Me	asurements					FINC
* Con	ں es to Pin 29										FDEC
	es to Pin 29 es to Pin 34										PDEC
g											
g iltered	Aut	to Scroll: On 🔽	Insert Marker	r] Clear Cop	by to Clipboard	d Pause					
- iltered			Insert Marker	r Clear Cop	by to Clipboard	Pause					
- iltered imestam	np Sour	ce Message			by to Clipboard	D Pause					
- iltered	np Sour	ce Message Starting Se	et_Voltage_Mux	(setting=VDD_3_PIN)	by to Clipboard	d Pause					
- iltered imestan 1:41:36.	mp Sour .515 EVB .554 EVB	ce Message Starting Se Pausing 70		(setting=VDD_3_PIN) Ige MUX hold	by to Clipboard	d Pause					
- iltered imestan 1:41:36. 1:41:36.	mp Sour 515 EVB 554 EVB .625 EVB	ce Message Starting Se Pausing 70 Starting Re	et_Voltage_Mux) msec for volta ead_ADC(num_:	(setting=VDD_3_PIN) Ige MUX hold	by to Clipboard	Pause			_		
- iltered imestam 1:41:36. 1:41:36. 1:41:36.	mp Sour .515 EVB .554 EVB .625 EVB .629 EVB	ce Message Starting Se Pausing 70 Starting Re finished Re	et_Voltage_Mux 0 msec for volta ead_ADC(num_s ead_ADC(num_s	(setting=VDD_3_PIN) ige MUX hold samples=5)	· ·	Pause					

Figure 10.9. EVB GUI Window

10.4.1 Verify Free-Run Mode Operation

Assuming no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB") located around the perimeter of the EVB, the DUT should now be operating in free-run mode, as the DUT will be locked to the crystal in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

Note: Shutting "Off" then "On" of the VDD and VDDA supplies will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":



Figure 10.10. Write Design to EVB

Failure to do the step above will cause the device to read in a pre-programmed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run mode from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.

CB Si5392 EVB Default Configuration - ClockBuilder Pro	X
ClockBuilder Pro v2.30.1 🕏	SILICON LABS
Design Dashboard 🔻	Configuring Si5392E Rev A
Default plan for Si5392 EVB has been loaded. You can make edits to t	he EVB's configuration using the interactive Wizard.
Edit Configuration with Wizard Design ID & Notes • Host Interface • Application & Reference • Free Run • Inputs • Input Select • Outputs • I/O Skew • Hitless Switching Assistant • DSPLL • LOS • OOF • LOL • INTR	Evaluation Board Detected Si5392E Rev A EVB Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a design report (text) or create a draft datasheet addendum (PDF) for your design.	Documentation Si5395/94/92 Reference Manual Si5395/94/92 Data Sheet
Silicon Labs Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click here to get assistance.
🕒 Frequency Plan Valid 🥥 Design OK 😚 Pd: 641 mW, Tj: 84 °C	Home Close

Figure 10.11. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

<pre>Very very very very very very very very v</pre>	Si5392E Design Report		_		×
Variates Part: Si53932 Rev A Part: Si53932 Rev A Design ID: ClockBulder Pro v2.30.1 [2019-02-19] Timestamp: 2019-03-26 12:02:31 GMT-05:00 Design Rule Check Errors: Trors: Frors: To restrop a state of the					
Design ID: cnome> Created By: ClockBuilder Pro v2.30.1 [2019-02-19] Timestamp: 2019-03-26 12:02:31 GMT-05:00 Design Rule Check Errors: Errors: - No errors Warnings Design 					Ē
Created By: ClockBuilder Fro v2.30.1 [2019-02-19] Timestamp: 2019-03-26 12:02:31 GMT-05:00 Design Rule Check Errors: - No errors Marnings: - No warnings Design Host Interface: I/O Fower Supply: VDD (Core) SFI Mode: 4-Mire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) Internal Reference: 48 Miz (XTAL - Crystal) Internal Reference: 48 Miz (XTAL - Crystal) 10 Mix (XTAL - Cr	Part:	S15392E Rev A			
<pre>Timestamp: 2019-03-26 12:02:31 GMT-05:00 Design Rule Check Marnings: - No errors Marnings: - No varnings Design Host Interface: I/O Power Supply: VDD (Core) SFI Mode: 4-Wire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) Internal Reference: 48 MHz (XTAL - Crystal) Inputs: IN0: 25 MHz Standard IN1: Dumedd IN2: Dumedd IN2: Dumedd IN2: Dumedd IN2: Dumedd OUTputs: OUT0: 156.25 MHz [156 + 1/4 MHz] Enabled, LVDS 2.5 V OUT1: 31.25 MHz [312 + 1/2 MHz] Enabled, LVDS 2.5 V OUT1: 31.4375 GHz [13 + 7/16 GHz] Prod = 1.7857142857142857 MHz [1 + 11/14 MHz] Fma0 = 625 MHz P dividers: P 00 = 14 P1 = Dumed P2 = Dumed P2 = Dumed P3 = 1 WOXME = 279.9479188140707284 [279 + 50580/53359] M = 1505</pre>	Design ID:	<none></none>			
Pesign Rule Check Errors: - No errors Warnings: - No warnings Design Host Interface: I/O Fower Supply: VDD (Core) SFI Mode: 4-Wire IZC Address Range: 104d to 107d / 0x68 to 0x6B (selected via AO/Al pins) Internal Reference: 48 Mfz (XTAL - Crystal) Internal Reference: 48 Mfz (XTAL - Crystal) Internal Reference: 48 Mfz (XTAL - Crystal) Inturs: IN0: 25 MHz Standard IN1: Duused IN2: Duused IN3: Duused Outputs: OUT0: 156.25 MHz [156 + 1/4 MHz] Enabled, LVDS 2.5 V OUT1: 312.5 MHz [312 + 1/2 MHz] Enabled, LVDS 2.5 V Frequency Plan Froc = 13.4375 GHz [13 + 7/16 GHz] Prof = 1.78571428571428571 MHz [1 + 11/14 MHz] Frad = 625 MHz P dividers: P0 = 14 P1 = Duused P2 = Duused P3 = Duused P3 = Duused P3 = Duused P3 = Duused P4 = 1505 N dividers: NO:					
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<pre></pre>					
<pre>Host Interface: I/O Fower Supply: VDD (Core) SPI Mode: 4-Wire IZC Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/A1 pins) Internal Reference: 48 Mfz (XTAL - Crystal) Inputs: INO: 25 MHz Standard IN1: Unused IN3: Unused Outputs: OUTO: 156.25 MHz [156 + 1/4 MHz] Enabled, LVDS 2.5 V OUTI: 312.5 MHz [312 + 1/2 MHz] Enabled, LVDS 2.5 V Frequency Plan Fvoc = 13.4375 GHz [13 + 7/16 GHz] Prof = 1.78571428571428571 MHz [1 + 11/14 MHz] Fns0 = 625 MHz P dividers: P0 = 14 P1 = Unused P2 = Unused P2 = Unused P3 = Unused P3 = Unused Pxaxb = 1 MCMXMB = 279.9479188140707284 [279 + 50580/53359] M dividers: NO: No: Tree Content of the second of</pre>					
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<pre>SPI Mode: 4-#ire I2C Address Range: 104d to 107d / 0x68 to 0x6B (selected via A0/Al pins) Internal Reference: 48 MHz (XTAL - Crystal) Inputs: IN0: 25 MHz Standard IN1: Duneed IN2: Unused Outputs: OUTO: 156.25 MHz [156 + 1/4 MHz] Enabled, LVDS 2.5 V OUT1: 312.5 MHz [312 + 1/2 MHz] Enabled, LVDS 2.5 V OUT1: 31.4375 GHz [13 + 7/16 GHz] Frequency Plan From = 13.4375 GHz [13 + 7/16 GHz] Fpfd = 1.7857142857142857 MHz [1 + 11/14 MHz] Fma = 625 MHz P = 14 P1 = Unused P2 = Unused P2 = Unused P3 = Duneed P3 = Duneed Pxaxb = 1</pre>		: VDD (Core)			
<pre>Internal Reference: 48 MHz (XTAL - Crystal) Inputs: IN0: 25 MHz Standard TN1: Dunsed IN1: Dunsed IN2: Unused OUTputs: OUT0: 156.25 MHz [156 + 1/4 MHz] Enabled, LVD5 2.5 V OUT1: 312.5 MHz [152 + 1/2 MHz] Enabled, LVD5 2.5 V OUT1: 312.5 MHz [132 + 1/2 MHz] Enabled, LVD5 2.5 V Prequency Plan Fvco = 13.4375 GHz [13 + 7/16 GHz] Ppfd = 1.78571428571428571 MHz [1 + 11/14 MHz] Fma0 = 625 MHz P 0 = 14 P1 = Unused P2 = Unused P2 = Unused P2 = Unused Pxaxb = 1 NO: OUT1 = 00000000000000000000000000000000000</pre>					
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NO: ,					
	N0:				w
Copy to Clipboard Save Report Ask for Help Close	Copy to Clipboard	Save Report Ask for Help		Cla	~~

Figure 10.12. Design Report Window

10.4.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode.

10.5 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CBPro Wizard, click on Edit Configuration with Wizard:



Figure 10.13. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations.

515392 EVB Defau	It Configuration - ClockBuilder Pro	-		X
ClockBuild	er Pro v2.30.1 🍫	SILICON	LA	B
Step 1 of 14 - D	sign ID & Notes ▼	Configuring Si	392E R	ev .
Design ID The device has 8 r Design ID:	egisters, DESIGN_ID0 through DESIGN_ID7, that can be used to store a design/configuration/rev	ision identifier.		
	The string you enter here is stored as ASCII bytes in registers DESIGN_ID0 through DESIGN_IC	07.		
Padding Mode:	NULL Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padde character).	ed with 0x00 bytes (ak	a NULL	
	Space Padded If you do not enter the full 8 characters, the remaining bytes of DESIGN_IDx will be padde character).	ed with 0x20 bytes (sp	ace	
	u want here. The text is stored in your project file and included in design reports and custom par ord wrapped in reports, you can use newlines to start a new paragraph.	t number datasheet a	ddendum	s.

Figure 10.14. Design Wizard

Note you can click on the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. After making your desired changes, you can click on Write to EVB to update the DUT to reconfigure your device real-time. The Design Write status window will appear each time you make a change.

CB Si5392E Design Write	_	×
Writing Si5392E Design to EVB Address 0x023E		

Figure 10.15. Writing Design Status

10.6 Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CBPro Wizard by clicking on the icon on your desktop and then selecting Open Design Project File.



Figure 10.16. Open Design Project File

Locate your CBPro design file (*.slabtimeproj or *.sitproj file).design file in the Windows file browser.



Figure 10.17. Browse to Project File

Select Yes when the WRITE DESIGN to EVB popup appears:

Bi5392 EVB Default Configuration - ClockBuilder Pro	– 🗆 X
ClockBuilder Pro v2.30.1 🍫	SILICON LABS
Design Dashboard 🔻	Configuring Si5392E Rev A
Default plan for Si5392 EVB has been loaded. You can make edits to t	the EVB's configuration using the interactive Wizard.
Edit Configuration with Wizard Design ID & Notes · Host Interface · Application & Reference · Free Run · Inputs · Input Select · Outputs · I/O Skew · Hitless Switching Assistant · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5392E Rev A EVB Write Design to EVB Open EVB GUI
Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a design report (text) or create a draft datasheet addendum (PDF) for your design.	Documentation <u>Si5395/94/92 Reference Manual</u> <u>Si5395/94/92 Data Sheet</u>
Silicon Labs Cloud Services You can <u>create a custom part number</u> for your design, which can be used to order factory pre-programmed devices. Or <u>request a phase noise report</u> for this design.	Ask for Help Have a question about your design? Click here to get assistance.
Frequency Plan Valid 🕢 Design OK 🔅 Pd: 641 mW, Tj: 84 °C	Home Close

Figure 10.18. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

10.7 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting Export as shown below:



Figure 10.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

Si5392E Expo	n.					_	
ntroduction	Register File	Settings File	Multi-Project Regi	ister/Settings	Regmap		
About Regi	ster Export						
This export configuratio		e registers that	t need to be writte	en to the Si539	2E to achie	eve your desig	n/
	d line version o prompt to learr		vailable. Type CBPr	roProjectRegi	stersExport	t help from a	9
Options							
Export Type	2:						
Each		Values (CSV) Fi is an address,d	ile data pair in hexade	cimal format.	A comma s	eparates the a	address
The r used Include If check be prefi	directly in firm summary heac ed, an informa	equence is exp ware code. ler tional header v	oressed in C code v will be included at neader will contain	the top of the	e file. Each l	' line in the hea	der will
Certain This ens the dow	control registe ures the devic	e is stable duri	register writes itten before and af ing configuration o turn inclusion of th	download and	resumes n	ormal operation	on after

Figure 10.20. Export Settings

UG387: Si5392 Evaluation Board User's Guide • Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

11. Writing a New Frequency Plan or Device Configuration to Non-Volatile Memory (OTP)

Note: Writing to the device non-volatile memory (OTP) is NOT the same as writing a configuration into the Si5392 using ClockBuilder Pro on the Si5392 EVB. Writing a configuration into the EVB from ClockBuilder Pro is done using Si5392 RAM space and can be done virtually unlimited numbers of times. Writing to OTP is limited as described below.

Refer to the Si5395/4/2 Family Reference Manuals and device data sheets for information on how to write a configuration to the EVB DUT's non-volatile memory (OTP). The OTP can be programmed a maximum of two times only. Care must be taken to ensure the configuration desired is valid when choosing to write to OTP.

UG387: Si5392 Evaluation Board User's Guide • Serial Device Communications

12. Serial Device Communications

12.1 Onboard SPI Support

The MCU onboard the Si5392 EVB communicates with the Si5392 device through a 4-wire SPI (Serial Peripheral Interface) link. The MCU is the SPI master and the Si5392 device is the SPI slave. The Si5392 device can also support a 2-wire I²C serial interface, although the Si5392 EVB does NOT support the I²C mode of operation. SPI mode was chosen for the EVB because of the relatively higher speed transfers supported by SPI vs. I²C.

12.2 External I²C Support

I²C can be supported if driven from an external I²C controller. The serial interface signals between the MCU and Si5392 pass through shunts loaded on header J17. These jumper shunts must be installed in J17 for normal EVB operation using SPI with CBPro. If testing of I²C operation via external controller is desired, the shunts in J17 can be removed thereby isolating the on-board MCU from the Si5392 device. The shunt at JP1 (I2C_SEL) must also be removed to select I²C as Si5392 interface type. An external I²C controller connected to the Si5392 side of J17 can then communicate to the Si5392 device. (For more information on I²C signal protocol, please refer to the Si5392 data sheet.)

The figure below illustrates the J17 header schematic. J17 even numbered pins (2, 4, 6, etc.) connect to the Si5392 device and the odd numbered pins (1, 3, 5, etc.) connect to the MCU. Once the jumper shunts have been removed from J17 and JP1, I²C operation should use J17 pin 4 (DUT_SDA_SDIO) as the I2C SDA and J17 pin 8 (DUT_SCLK) as the I²C SCLK. Please note the external I²C controller will need to supply its own I²C signal pull-up resistors



Figure 12.1. Serial Communications Header J17

UG387: Si5392 Evaluation Board User's Guide • Si5392 EVB Schematic and Bill of Materials (BOM)

13. Si5392 EVB Schematic and Bill of Materials (BOM)

The Si5392 EVB Schematic and Bill of Materials (BOM) can be found at: www.silabs.com/documents/public/schematic-files/si539x-design-files.zip

Note: Please be aware that the Si5392 EVB schematic is in OrCad Capture hierarchical format and not in a typical "flat" schematic format.

This document supports the evaluation board silkscreened Si5392 EVB for the following configurations as described in the table below. The data sheet documents the different Si5392 grades.

Config #	Eval Board Label	Si5392		Notes
		Grade	Revision	
1	Si5392J-A-EB	J	A	No Crystal and related components installed.
2	Si5392E-A-EB	E	A	No Crystal and related components installed. Precision grade DUT and label also differ versus Si5392J-A-EB.

Note:

1. The Si5392J-A-EB should be used to evaluate Si5392J/K/L/M plans.

2. The Si5292E-A-EB should be used to evaluate the Si5392E plans.

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