MACRONIX INTERNATIONAL CO., LTD.

Product/Process Change Notice

PCN # P-1509-0001
Date: 2015/11/13

Dear Customer:

Please be informed that Macronix is going to add 2nd source assembly subcontractor to backup customer original approved assembly subcontractors for NAND Flash 48TSOP package products. The 2nd source assembly subcontractor is ChipMOS located in Taiwan.

The detailed information about this change is described in the following pages. This process change has passed Macronix' qualification based on JEDEC standard, and the qualification report is attached below.

If you have any questions, concerns, or requests about this change, please contact your local Macronix Sales Representatives within 30 days, otherwise Macronix will assume customer received the PCN with no comments and the change is acceptable to the customer. Macronix follows JEDEC standards, in JESD-46D, it stipulates: ".....Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change".

Thank you.

Macronix International Co., Ltd.
旺宏電子股份有限公司

(Note: For the customers who receive Macronix PCNs via distributors, Macronix will assist the distributors to convey the PCNs to the customers. It is each distributor's responsibility to communicate and track the responses of each customers and report back to Macronix, the distributor shall assume full responsibilities if failed to do so.)

PCN No.: P-1509-0001 **Issue Date :** 2015/11/13

Subject: Adding a new assembly vendor– ChipMOS for NAND Flash 48TSOP package products.

Affected Macronix Part No.:

MX30LF2G18AC-TI, MX30LF2G28AB-TI, MX30LF2GE8AB-TI, MX30LF4G18AC-TI, MX30LF4G28AB-TI, MX30LF4G28SB-TI, MX30LF4GE8AB-TI, MX30UF2G18AB-TI, MX30UF2G28AB-TI, MX30UF4G18AB-TI, MX30UF4G28AB-TI, MX60LF8G18AC-TI, MX60LF8G28AB-TI

Package type: NAND Flash 48TSOP package products

Change Category : New assembly vendor

Reason of Change: To increase NAND Flash 48TSOP package assembly capacity and flexibility.

Before Change :	**After Change :**
Assembly vendor:	Assembly vendors:
SPIL	SPIL
	ChipMOS

Product identification:

ChipMOS assembled IC marking vendor code: a

SPIL assembled IC marking vendor code: S

Assessment of Change:

1. No impact to Form, Fit, Function, Quality & Reliability.
2. ChipMOS assembled 48TSOP had passed internal Macronix’s qualification based on JEDEC MSL level 3 standards and it is also Halogen-Free, and meets RoHS compliance.
   * Attached is ChipMOS assembled 48TSOP package qualification report
3. ChipMOS has been one of Macronix’s high performing assembly vendors for other package types for a long time.

Schedule:

CS Sample available: 2015/09/30

Mass production: 2015/12/01.

MACRONIX INTERNATIONAL CO., LTD.
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ChipMOS 48L TSOP(I) Package Qualification Report

1. PURPOSE:

To qualify new assembly subcontractor “ChipMOS” for 48TSOP package.

2. PACKAGE PROFILE:

ASSEMBLY HOUSE	ChipMOS
PACKAGE	48L TSOP(I) (12 x 20 mm)
DIE SIZE	6898 x 7351 μm^2
DIE ATTACH	Nitto EM-710
LEAD FRAME	Copper
WIRE BOND MATERIAL	Au
MOLD COMPOUND	Hitachi 9740HF
LEAD FINISH	Matte Sn

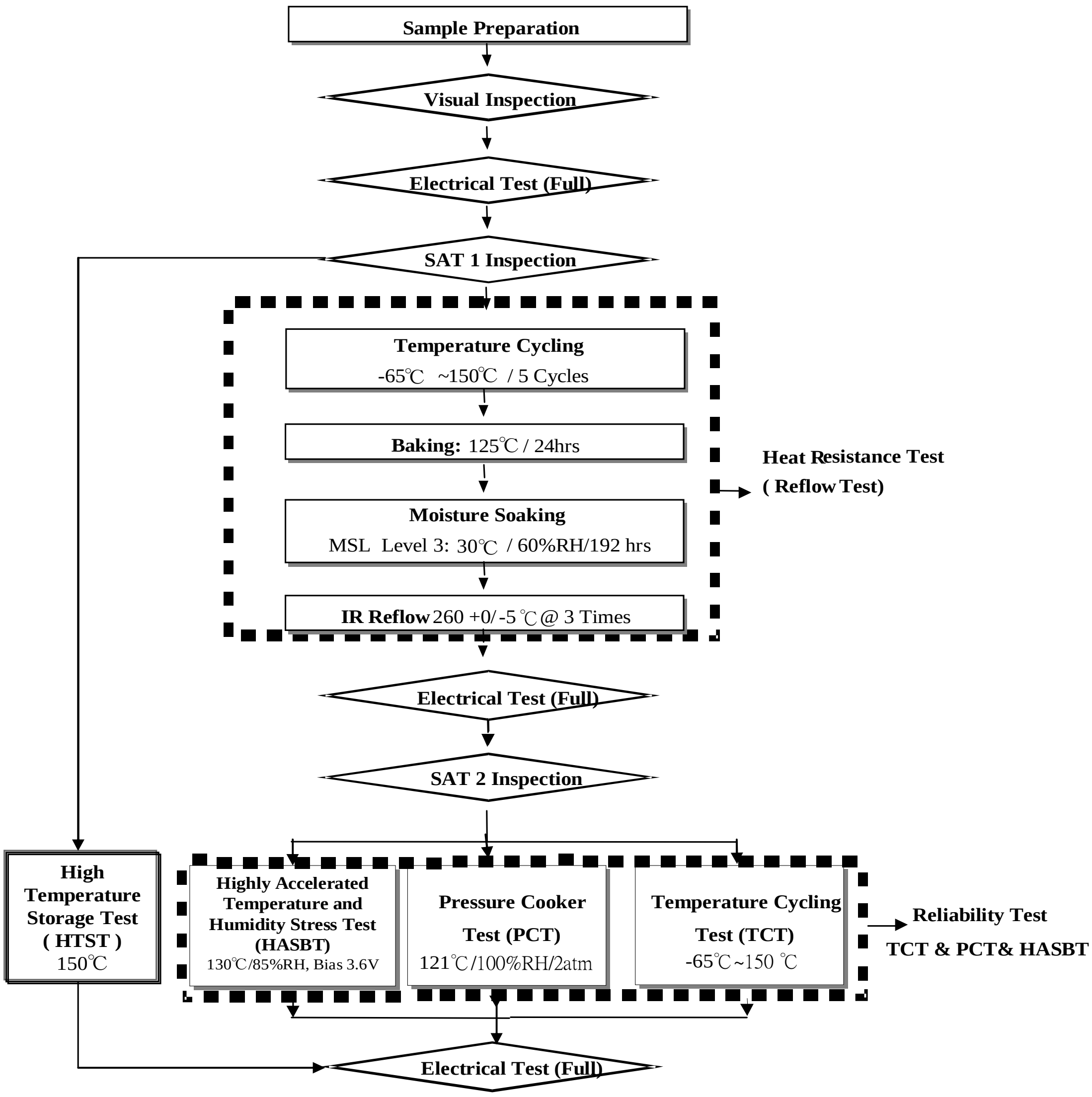
3. QUALIFICATION ITEMS, TEST CONDITIONS, AND TEST FLOW:

3-1. QUALIFICATION ITEMS:

Test Item	Reference	Test Condition
1. Heat Resistance Test: Reflow Test	JEDEC J-STD-020	MSL: Follow JEDEC MSL Level 3 (30℃/ 60%RH, 192hrs)
2. Pressure Cooker Test	JESD22-A102	121℃/ 100%RH/2 atm
3.Temperature Cycling Test	JESD22-A104	-65℃ ~150℃
4. Highly Accelerated Temperature and Humidity Stress Test	JESD22-A110	130℃/ 85% RH, Bias: 3.6V
5.High Temperature Storage Test	JESD22-A103	@150℃
6. Solderability Test	JESD22-B102	■ Steam aging 8hrs & Dipping Time≦5sec ■ Sn-Ag-Cu solder paste: 245℃ ■ Sn-Pb solder paste: 235℃

*Perform SAT examination before and after Preconditioning per JESD22-A112.

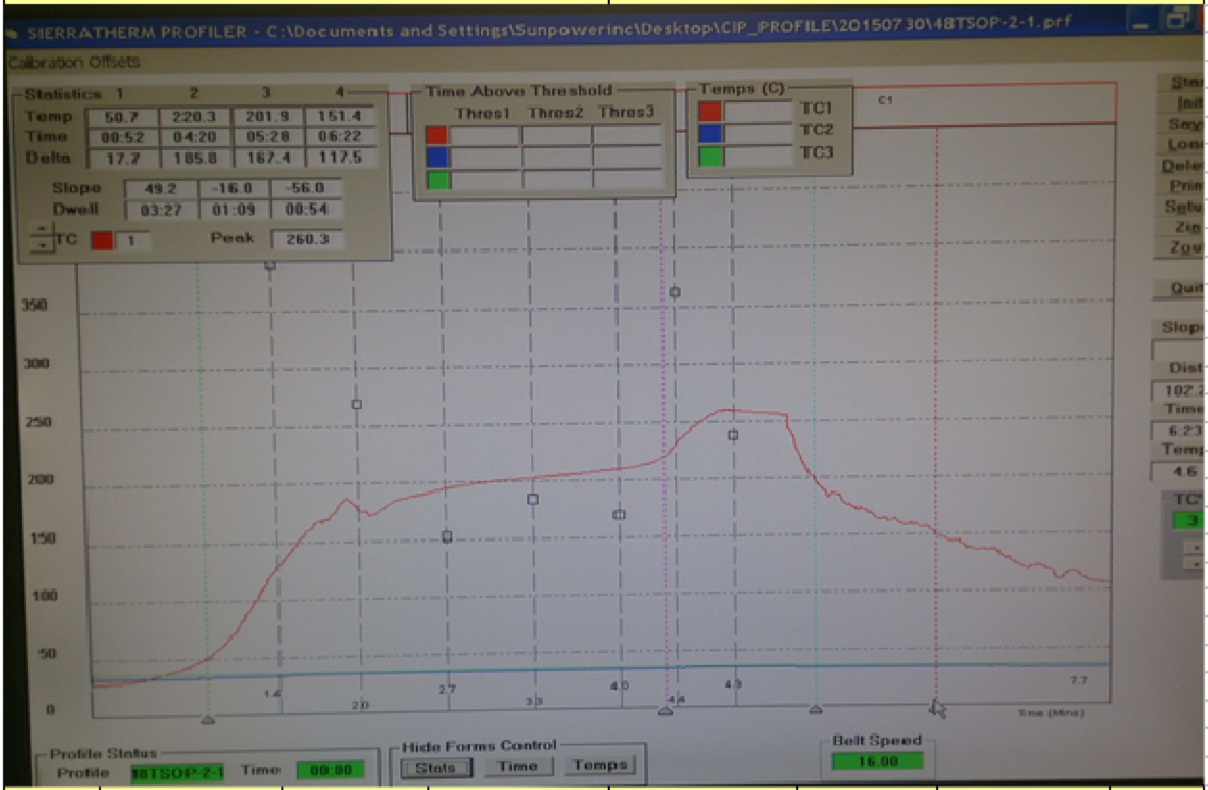
3-2. HEAT RESISTANT TEST (REFLOW TEST) AND RELIABILITY TEST FLOW



3-2-1. REFLOW PROFILE

Ra Lab Reflow Test Data

Equipment Name：	IR Reflow
Equipment Model：	SIERRA THERM/3K16-63C42-7AN
委託單號：	R-2015072189~91
Test Date：	2015.07/31



SIERRATHERM PROFILER - C:\Documents and Settings\Sunpowerinc\Desktop\CIP_PROFILE\20150730\48TSOP-2-1.prf

Statistics	1	2	3	4
Temp	50.7	220.3	201.9	151.4
Time	00:52	04:20	05:28	06:22
Delta	17.7	185.8	167.4	117.5
Slope	49.2	-16.0	-56.0	
Dwell	03:27	01:09	00:54	

TC 1 Peak 260.3

Profile Status: Profile 48TSOP-2-1 Time 00:00

Belt Speed 16.00

	Ramp-up rate(1)：	Pre-heat time：	Ramp-up rate(2)：	Peak Temperature：	Soldering Zone	Ramp-down rate：	結果判定
Temp rang	50~150℃	150~200℃	220~255℃	260-0 -5℃	220~220℃	200~150℃	Pass
Spec	1.5~3℃ Sec	60~120Sec	1.5~3℃ Sec	30~40Sec	60~150Sec	< 6℃ Sec	
Data	1.1	87	1.6	32	62	0.9	

Note 1: Subject the samples to 3 cycles of the above defined reflow conditions

Note 2: Time 25℃ to peak temperature: 8 minutes max.

Note 3: The time between reflows shall be 5 minutes minimum and 40 minutes maximum.

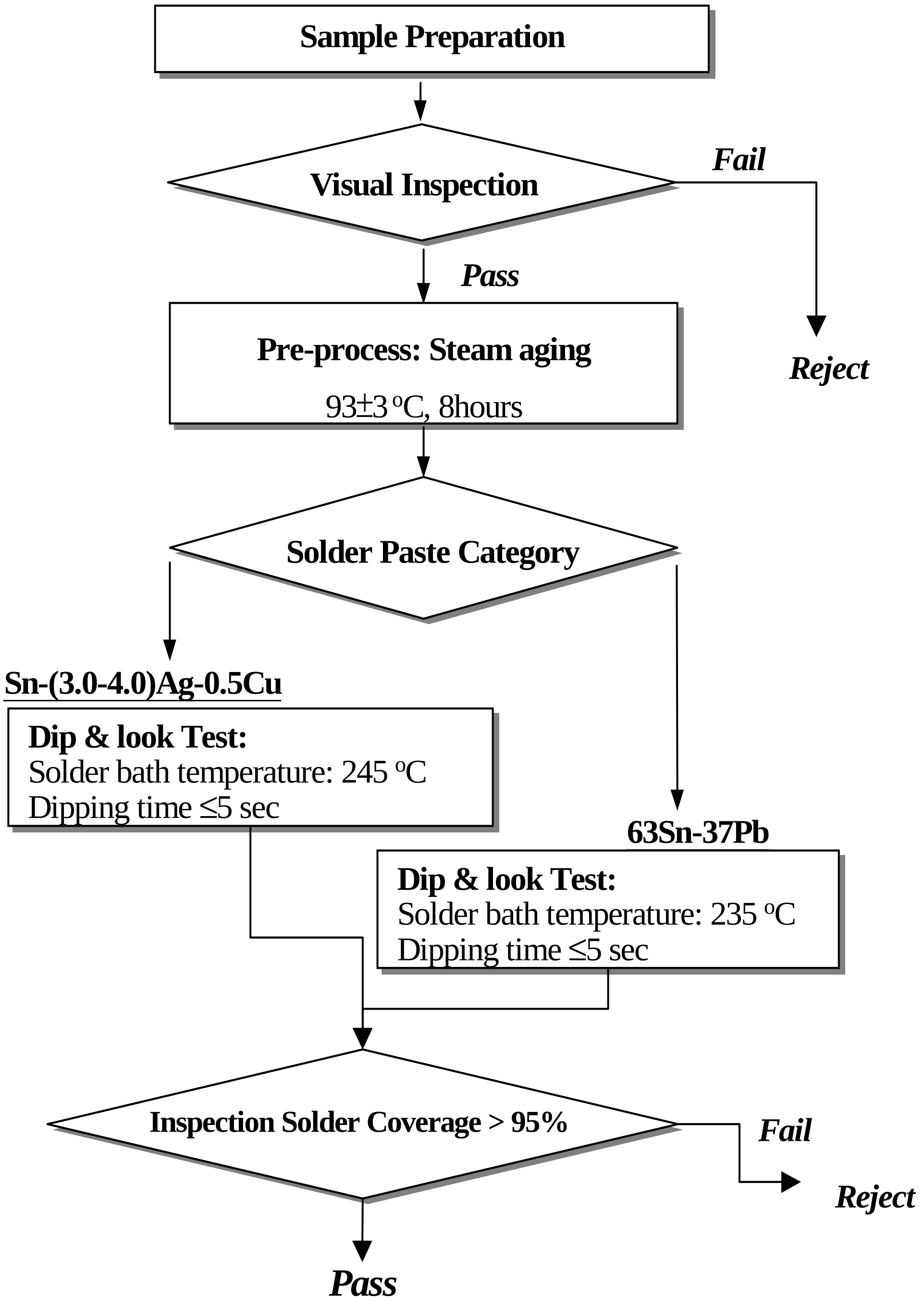
3-2-2. CRITERIA

LTPD= 3%, PCT 96 hours and TCT 500 cycles & HASBT 96 hours & HTST 500 hours.

3-2-3. REFERENCE SPECIFICATION

5650-0901: ASSEMBLY RELIABILITY QUALIFICATION SPEC

3-3. SOLDERABILITY TEST FLOW



4. RESULTS

4-1. HEAT RESISTANCE TEST and RELIABILITY TEST RESULTS

PRODUCT	6311		
LOT#	8B630800A6-1	8B630800A6-2	8B630800A6-3
DATE CODE	a1524	a1524	a1525
SAT 1	0/22	0/22	0/22
PRECON	0/250	0/250	0/250
SAT 2	0/22	0/22	0/22
PCT 96 HRS	0/77	0/77	0/77
TCT 500 CYC	0/77	0/77	0/77
HASBT 96 HRS	0/77	0/77	0/77
HTST 500 HRS	0/45	0/45	0/45

FAIL / SAMPLE SIZE

4-2. SOLDERABILITY TEST RESULTS

Matte Sn Plating

Plating Material	Matte Sn		
Solder Paste Material	Sn-(3.0-4.0)Ag-0.5Cu		
INSPECTION	0/5	0/5	0/5

FAIL / SAMPLE SIZE

Plating Material	Matte Sn		
Solder Paste Material	63Sn-37Pb		
INSPECTION	0/5	0/5	0/5

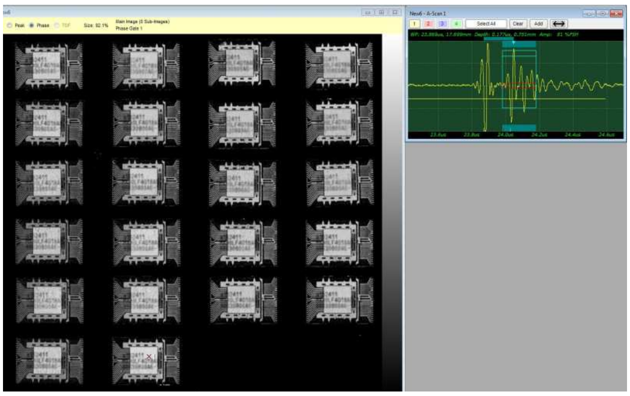
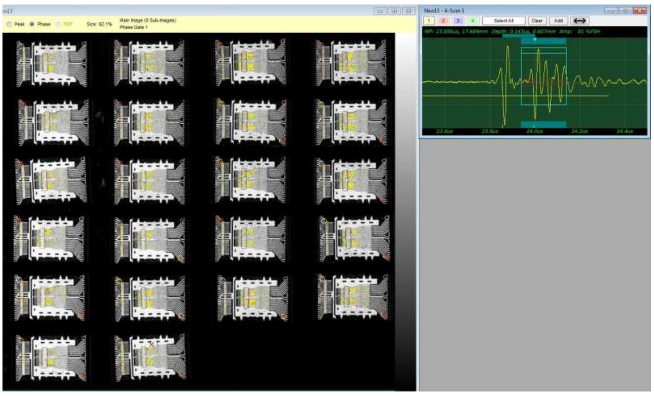
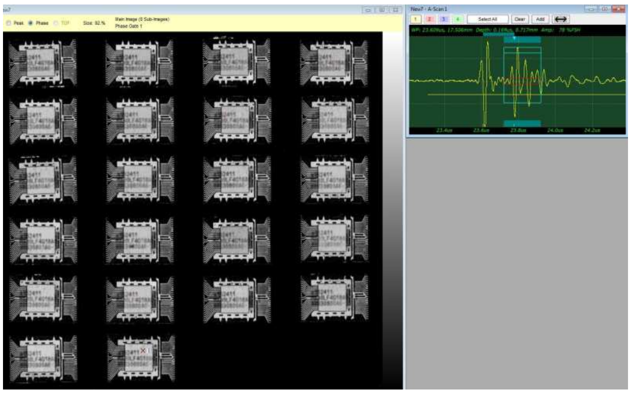
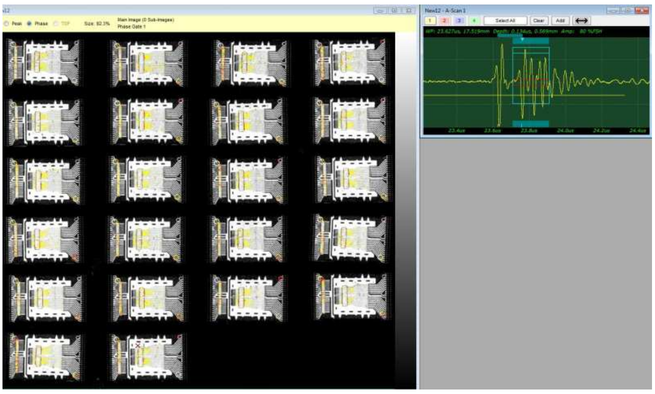
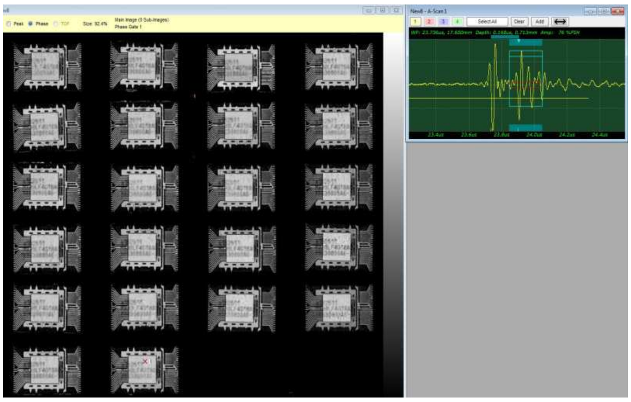
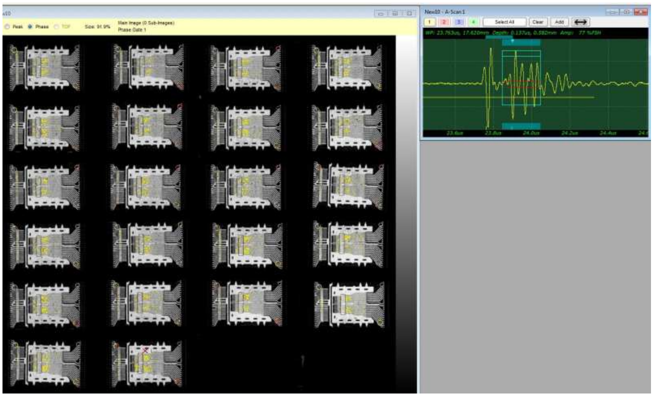
FAIL / SAMPLE SIZE

5. CONCLUSION: PASS

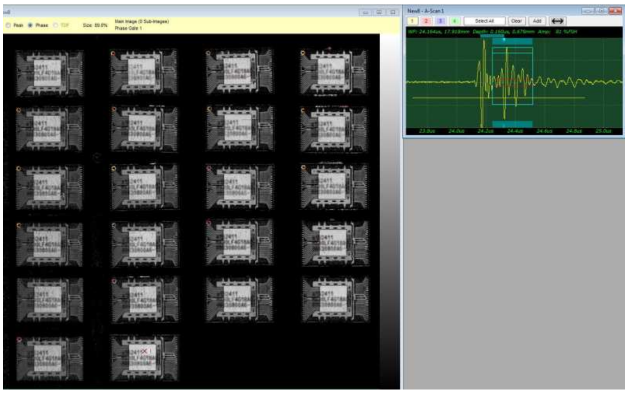
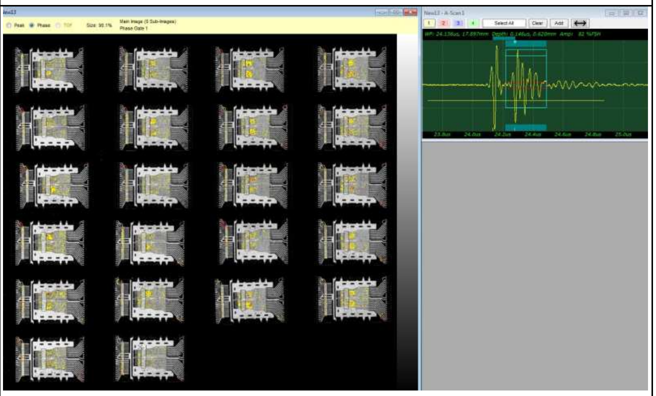
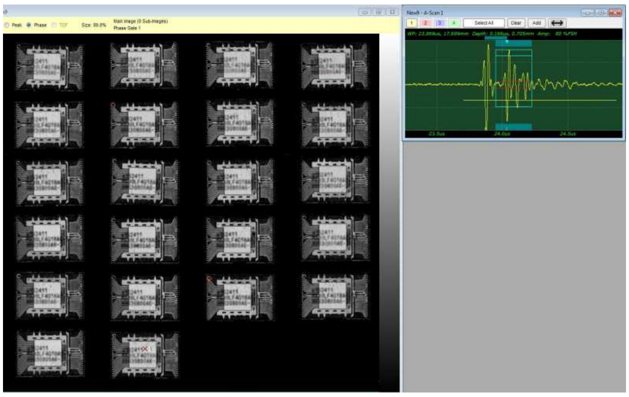
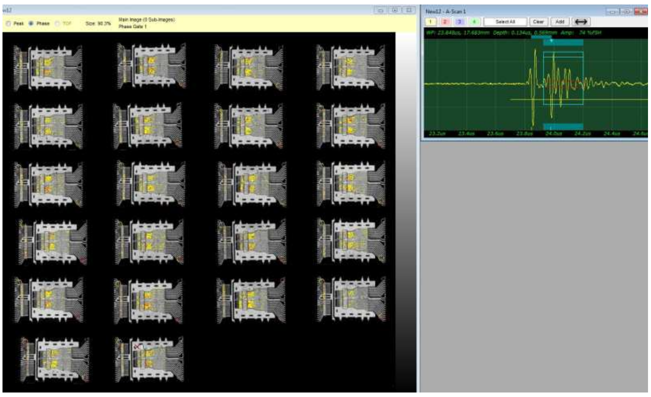
6. ATTACHED FILE

6-1. SAT PHOTO

6-1-1. BEFORE PRE-CONDITION

a1. Lot no#8B630800A6-1:Topside of package	a2. Lot no#8B630800A6-1:Backside of package
	
b1. Lot no#8B630800A6-2:Topside of package	b2. Lot no#8B630800A6-2:Backside of package
	
c1. Lot no#8B630800A6-3:Topside of package	c2. Lot no#8B630800A6-3:Backside of package
	

6-1-2. AFTER PRE-CONDITION

a1. Lot no#8B630800A6-1:Topside of package	a2. Lot no#8B630800A6-1:Backside of package
	
b1. Lot no#8B630800A6-2:Topside of package	b2. Lot no#8B630800A6-2:Backside of package
	
c1. Lot no#8B630800A6-3:Topside of package	c2. Lot no#8B630800A6-3:Backside of package