U_FPGA
FPGA.SchDoc

U_SODIMM
SODIMM.SchDoc

U_CLOCK
CLOCK.SchDoc

U_POWER
POWER.SchDoc

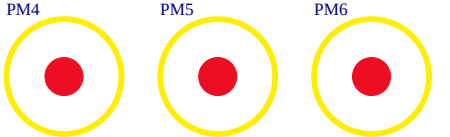
U_CONN
CONN.SchDoc

U_CPLD
CPLD.SchDoc

PM1 PM2 PM3

FIDU-DOT - small FIDU-DOT - small FIDU-DOT - small

PM4 PM5 PM6

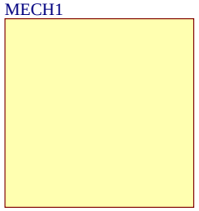


FIDU-DOT - small FIDU-DOT - small FIDU-DOT - small

Serial
Serial
Serialnumber 6,3 x 6.3mm

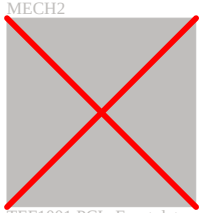
LOGO1
TE Logo PRINT Layer
LOGO PRINT

Front Bracket screw head on Top
MECH1



Slotblende Ndigo xTDC4 Lemo

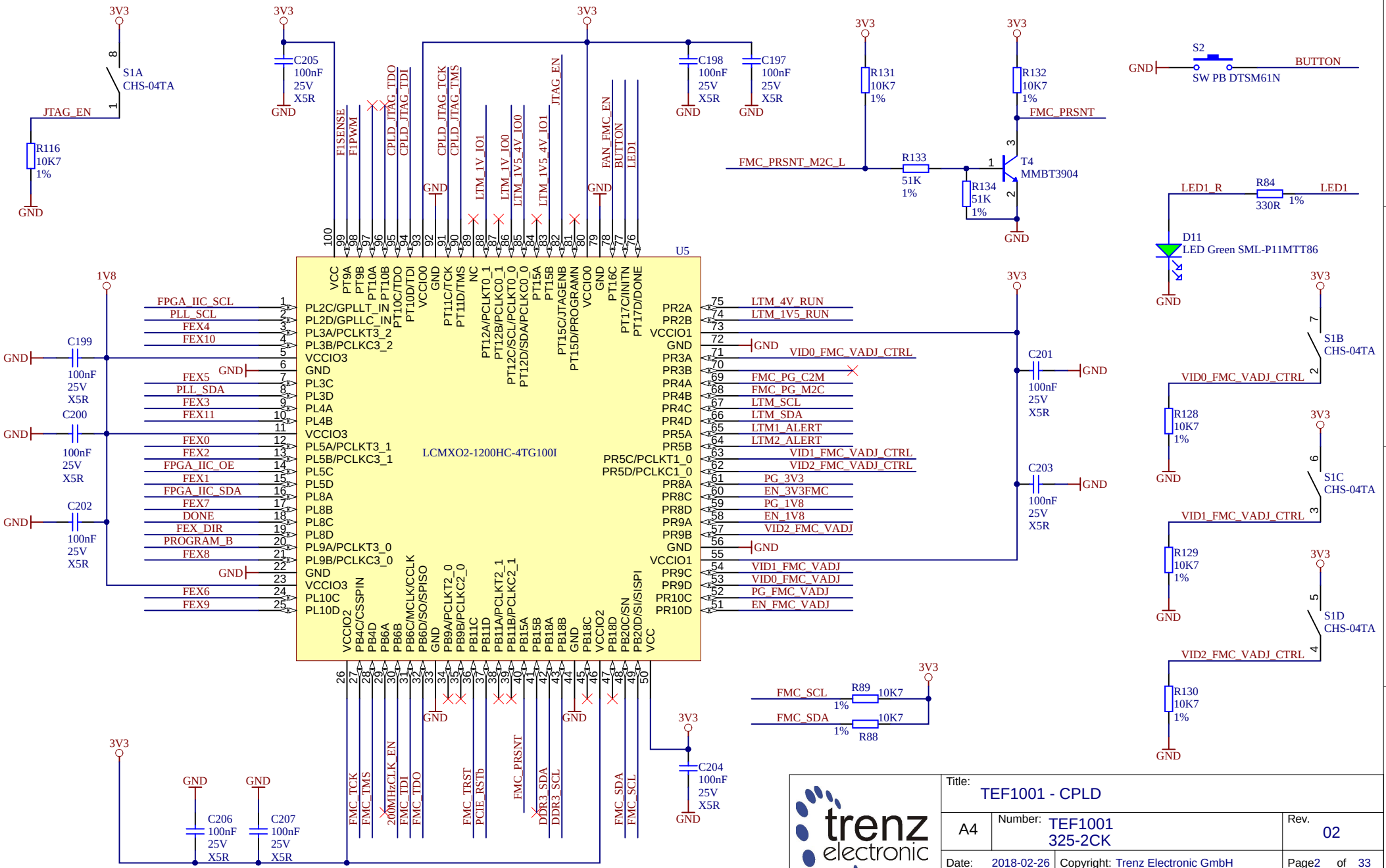
Front Bracket screw head on Bottom
MECH2



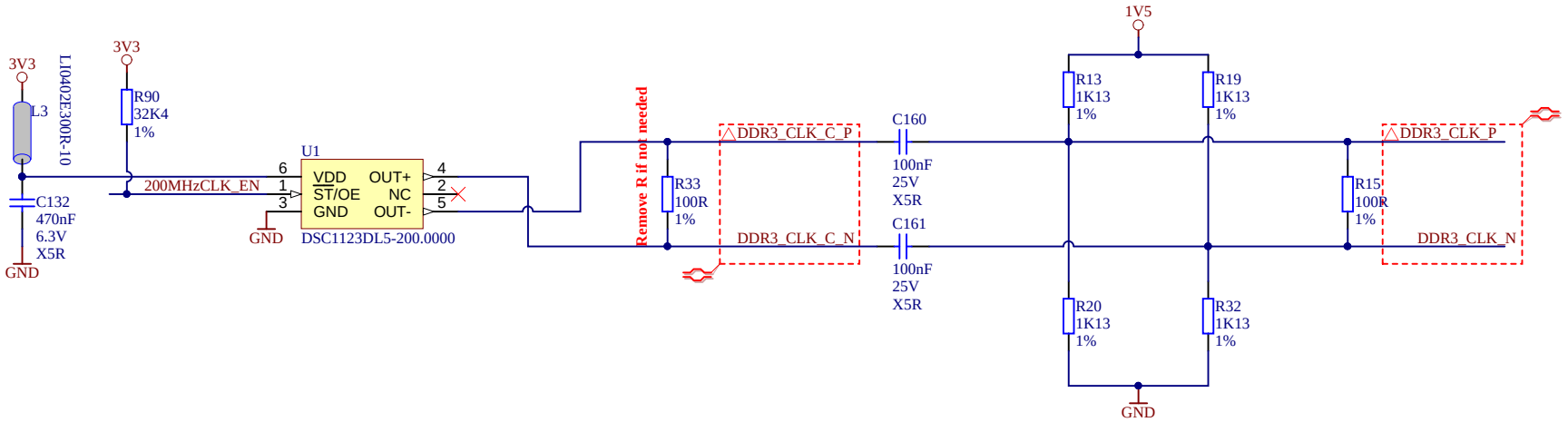
TEF1001 PCIe Frontplate

trenz electronic

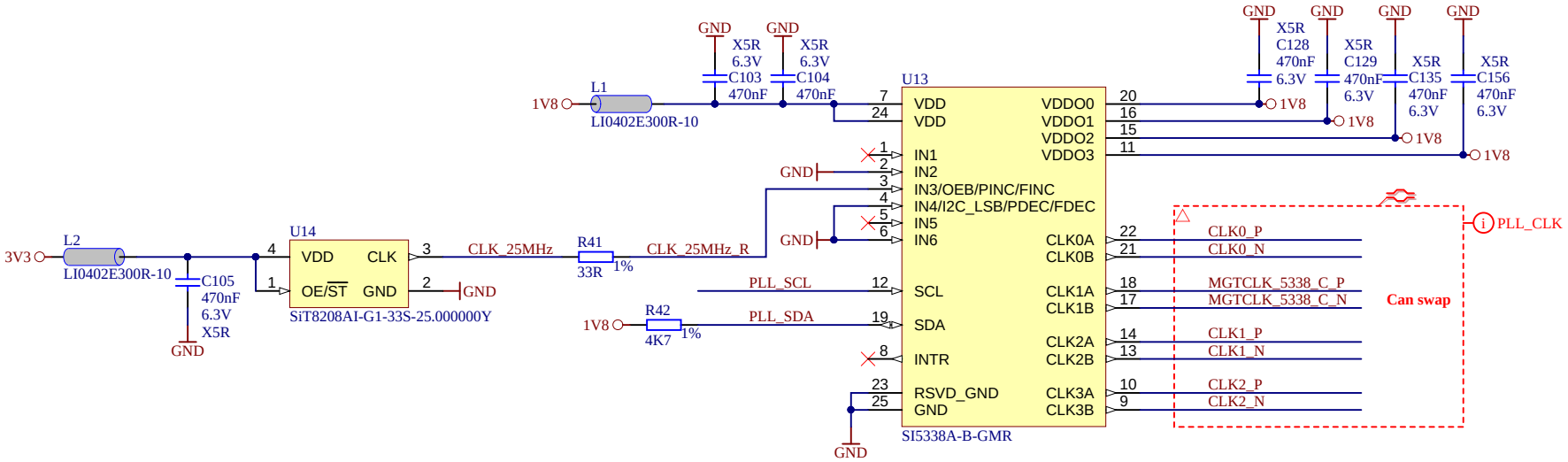
Title: TEF1001 - MAIN			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page1 of 33
Filename: TEF1001.SchDoc			

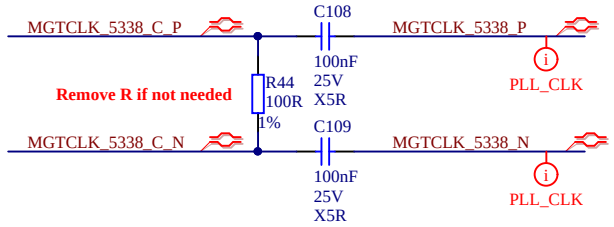

U5
LCMXO2-1200HC-4TG100I
S1A CHS-04TA
JTAG_EN
R116 10K7 1%
C205 100nF 25V X5R
C198 100nF 25V X5R
C197 100nF 25V X5R
R131 10K7 1%
R132 10K7 1%
FMC_PRSNT
FMC_PRSNT_M2C_L
R133 51K 1%
R134 51K 1%
T4 MMBT3904
S2 SW PB DTSM61N
BUTTON
LED1_R
R84 330R 1%
LED1
D11 LED Green SML-P11MTT86
S1B CHS-04TA
S1C CHS-04TA
S1D CHS-04TA
R128 10K7 1%
R129 10K7 1%
R130 10K7 1%
VID0_FMC_VADJ_CTRL
VID1_FMC_VADJ_CTRL
VID2_FMC_VADJ_CTRL
C199 100nF 25V X5R
C200 100nF 25V X5R
C202 100nF 25V X5R
C201 100nF 25V X5R
C203 100nF 25V X5R
C204 100nF 25V X5R
C206 100nF 25V X5R
C207 100nF 25V X5R
R89 10K7 1%
R88 10K7 1%
FMC_SCL
FMC_SDA
FPGA_IIC_SCL
PLL_SCL
FEX4
FEX10
FEX5
PLL_SDA
FEX3
FEX11
FEX0
FEX2
FPGA_IIC_OE
FEX1
FPGA_IIC_SDA
FEX7
DONE
FEX_DIR
PROGRAM_B
FEX8
FEX6
FEX9
LTM_4V_RUN
LTM_1V5_RUN
VID0_FMC_VADJ_CTRL
FMC_PG_C2M
FMC_PG_M2C
LTM_SCL
LTM_SDA
LTM1_ALERT
LTM2_ALERT
VID1_FMC_VADJ_CTRL
VID2_FMC_VADJ_CTRL
PG_3V3
EN_3V3FMC
PG_1V8
EN_1V8
VID2_FMC_VADJ
VID1_FMC_VADJ
VID0_FMC_VADJ
PG_FMC_VADJ
EN_FMC_VADJ
F1SENSE
F1PWM
CPLD_JTAG_TDO
CPLD_JTAG_TDI
CPLD_JTAG_TCK
CPLD_JTAG_TMS
LTM_1V_IO1
LTM_1V_IO0
LTM_1V5_4V_IO0
LTM_1V5_4V_IO1
JTAG_EN
FAN_FMC_EN
BUTTON
LED1
FMC_TCK
FMC_TMS
200MHzCLK_EN
FMC_TDI
FMC_TDO
FMC_TRST
PCIE_RSTb
FMC_PRSNT
DDR3_SDA
DDR3_SCL
FMC_SDA
FMC_SCL
Title: TEF1001 - CPLD
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page2 of 33
Filename: CPLD.SchDoc
trenz electronic

U_CLK-SI5338
CLK-SI5338.SchDoc



trenz electronic	Title: TEF1001 - CLOCK		
	A4	Number: TEF1001 325-2CK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page3 of 33
	Filename: CLOCK.SchDoc		

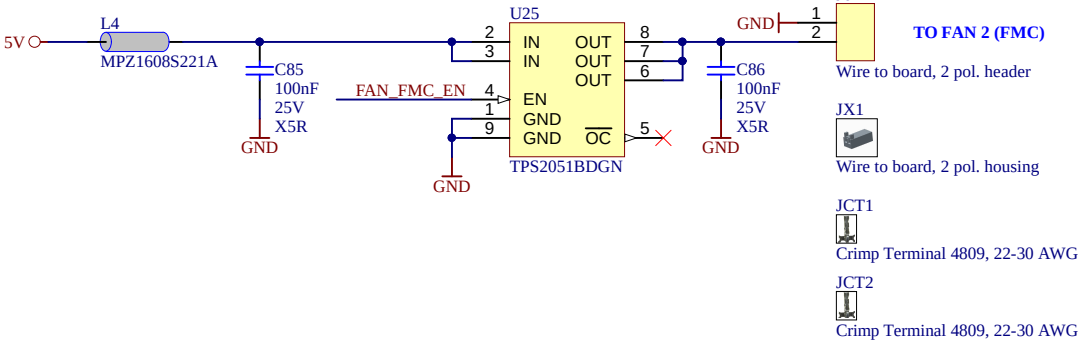


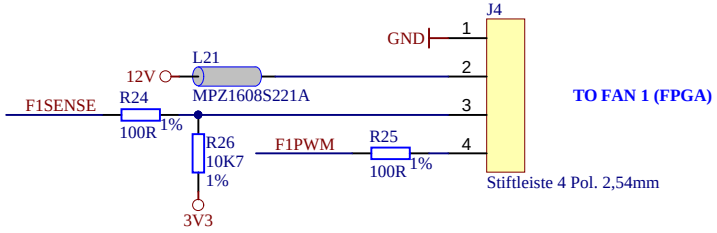


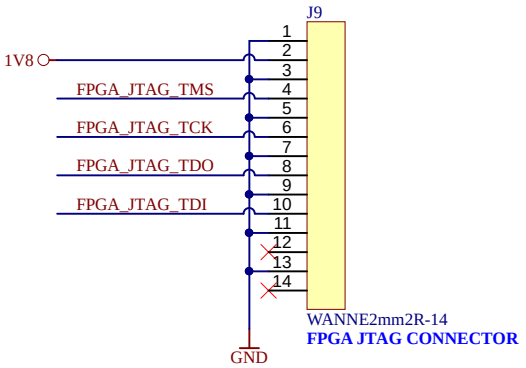
Title: TEF1001 - CLK-SI5338			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page4 of 33
Filename: CLK-SI5338.SchDoc			

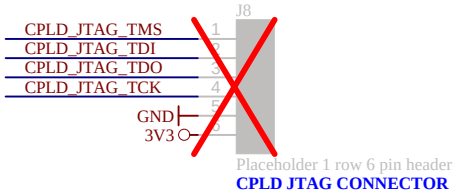
U_FMC
FMC.SchDoc

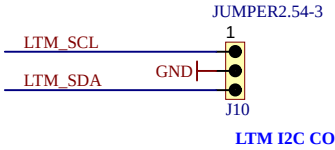
U_PCIE_CONN
PCIE_CONN.SchDoc





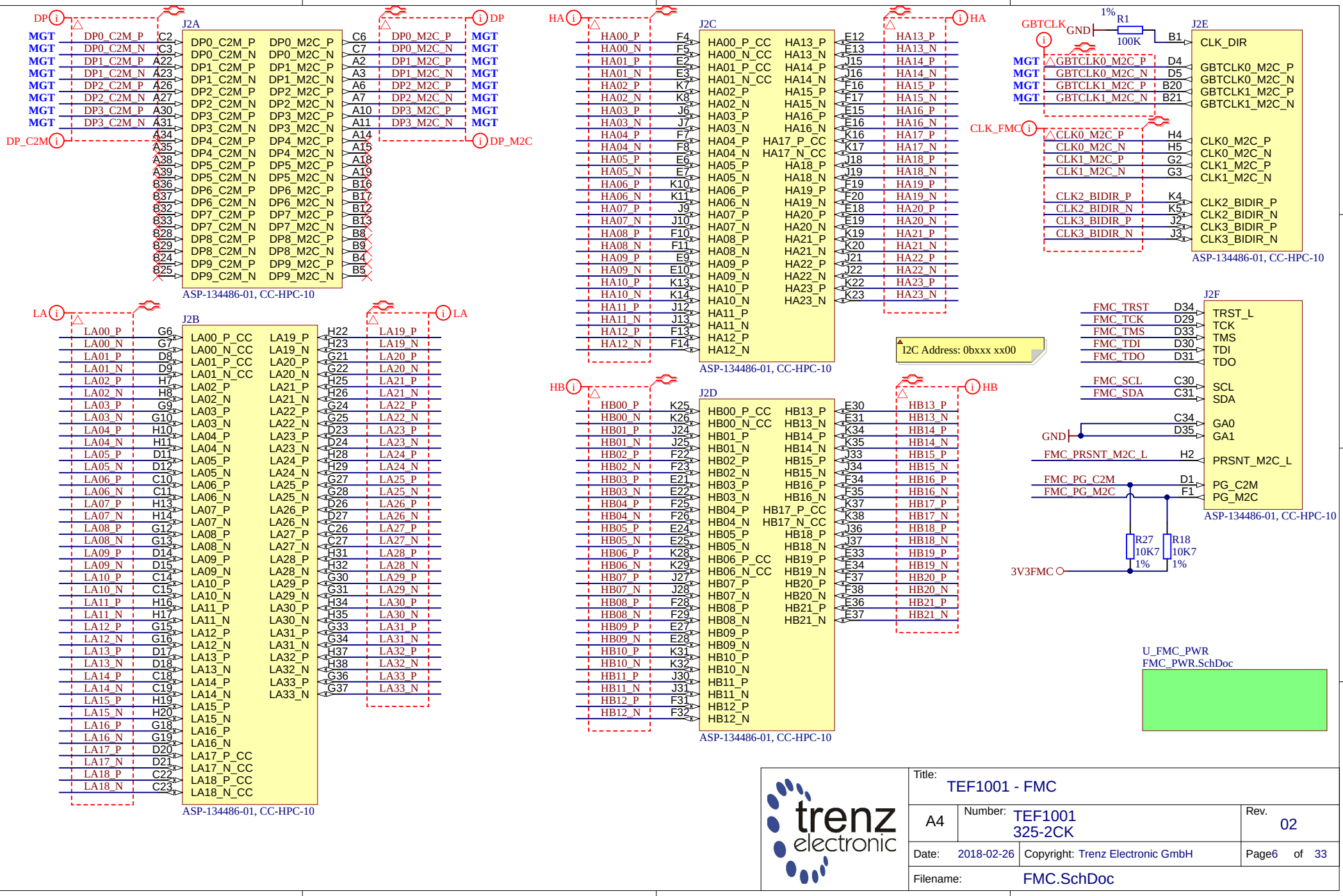


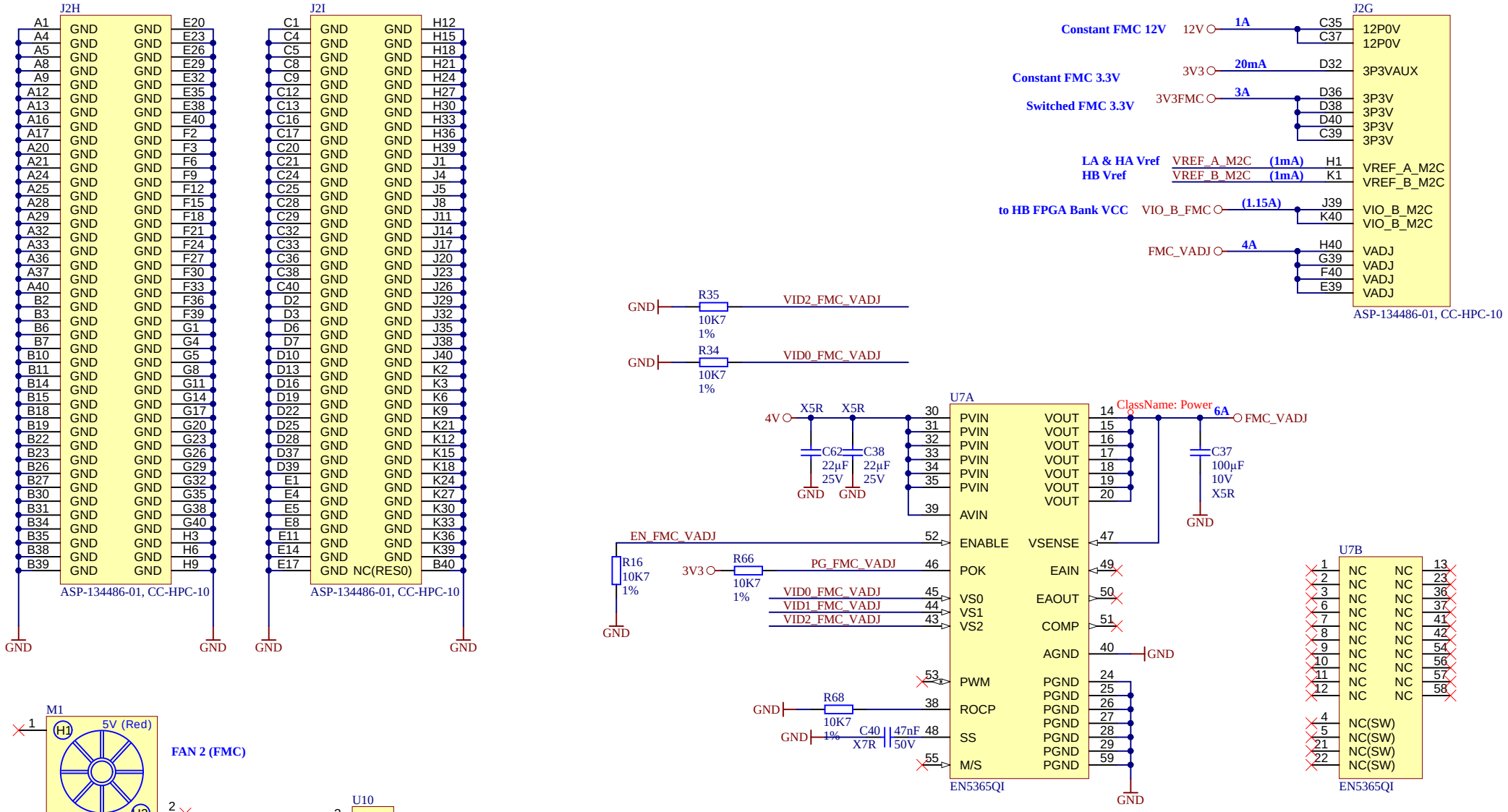


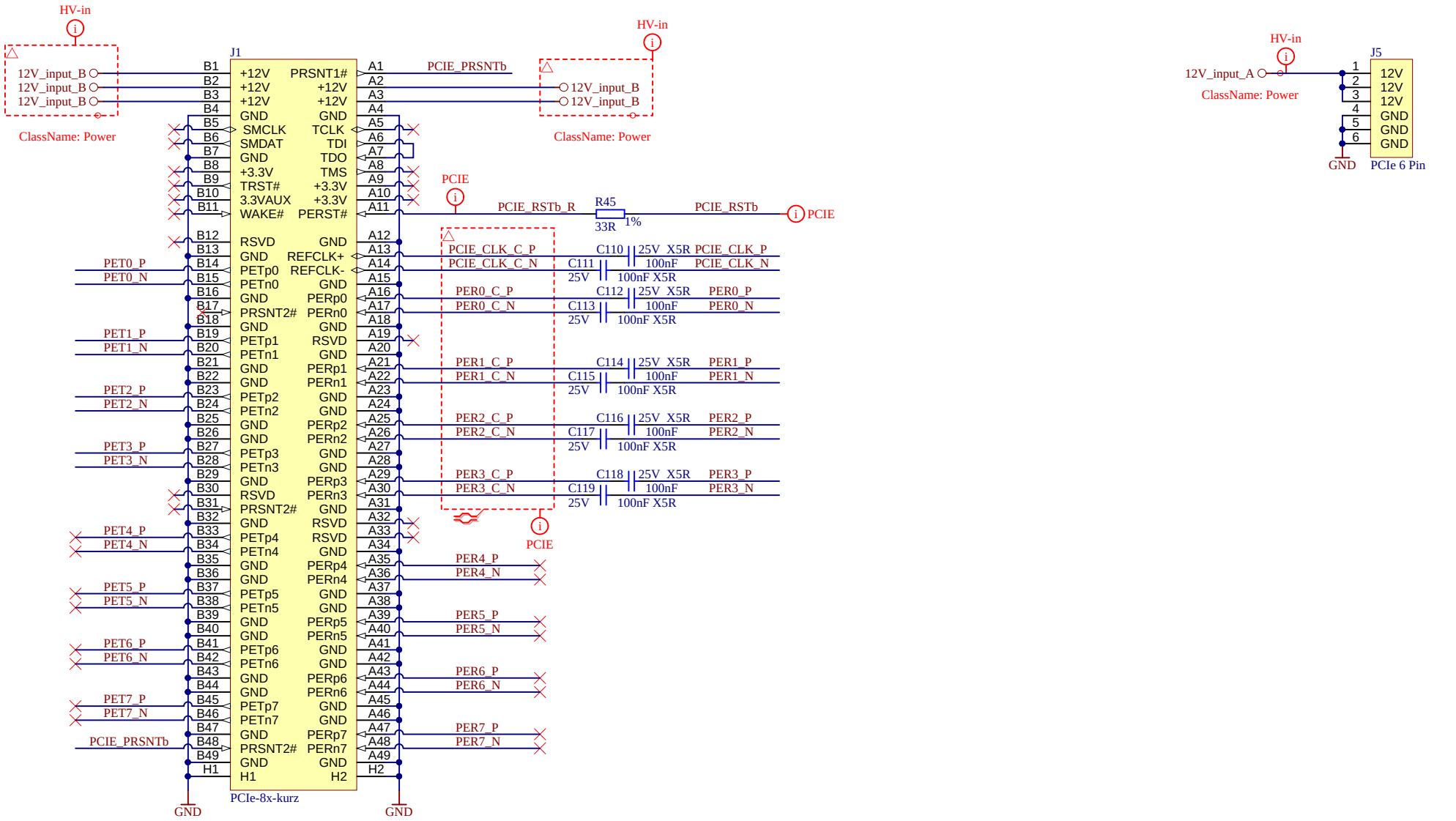


trenz electronic

Title: TEF1001 - CONN			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page5 of 33
Filename: CONN.SchDoc			


J2A
ASP-134486-01, CC-HPC-10
J2B
ASP-134486-01, CC-HPC-10
J2C
ASP-134486-01, CC-HPC-10
J2D
ASP-134486-01, CC-HPC-10
J2E
ASP-134486-01, CC-HPC-10
J2F
ASP-134486-01, CC-HPC-10
I2C Address: 0bxxx xx00
U_FMC_PWR
FMC_PWR.SchDoc
trenz electronic
Title: TEF1001 - FMC
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page6 of 33
Filename: FMC.SchDoc


J2H
J2I
J2G
ASP-134486-01, CC-HPC-10
Constant FMC 12V
Constant FMC 3.3V
Switched FMC 3.3V
LA & HA Vref
HB Vref
to HB FPGA Bank VCC
VID2_FMC_VADJ
VID0_FMC_VADJ
U7A
EN5365QI
EN_FMC_VADJ
PG_FMC_VADJ
VID0_FMC_VADJ
VID1_FMC_VADJ
VID2_FMC_VADJ
FMC_VADJ
U7B
M1
FAN 2 (FMC)
5V (Red)
GND (Black)
FAN 5VDC 45X5MM .7W 1.06CFM
U10
Single FMC Con. Cooled BB Snap
Type: Set as Standard (No BOM)
VS2 | VS1 | VS0 | Output Voltage
0 | 0 | 0 | 3.3V
0 | 0 | 1 | 2.5V
0 | 1 | 0 | 1.8V
0 | 1 | 1 | 1.5V
1 | 0 | 0 | 1.25V
1 | 0 | 1 | 1.2V
trenz electronic
Title: TEF1001 - FMC_PWR
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page7 of 33
Filename: FMC_PWR.SchDoc



trenz electronic	Title: TEF1001 - PCIE CONNECTOR		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page8 of 33
Filename: PCIE_CONN.SchDoc			

U_FPGA_BANK_12
FPGA_BANK_12.SchDoc

U_FPGA_BANK_13
FPGA_BANK_13.SchDoc

U_FPGA_BANK_14
FPGA_BANK_14.SchDoc

U_FPGA_BANK_15
FPGA_BANK_15.SchDoc

U_FPGA_BANK_16
FPGA_BANK_16.SchDoc

U_FPGA_MGT_BANKS
FPGA_MGT_BANKS.SchDoc

U_FPGA_CFG
FPGA_CFG.SchDoc

U_DDR_Banks
DDR_Banks.SchDoc

U_FPGA_POWER
FPGA_POWER.SchDoc

HEATSINK TYPE 2 (FPGA)

KK2
GND H1 GND
GND H2 GND
GND H3 GND
GND H4 GND

ATS-FPS058061011-40-C2-R0

HEATSINK TYPE 1 (FPGA)

KK1
GND H1
GND H2
GND H3
GND H4
T1SA-APBX-D125D

J3 ATS-HK76-R0
J7 ATS-HK76-R0

Hardware for HEATSINK TYPE 2 (FPGA)

R96 330R 1% FPGA_LED1
D1 LED Green SML-P11MTT86 GND

R100 330R 1% FPGA_LED2
D2 LED Green SML-P11MTT86 GND

R101 330R 1% FPGA_LED3
D3 LED Green SML-P11MTT86 GND

R102 330R 1% FPGA_LED4
D4 LED Green SML-P11MTT86 GND

3V3 C63 100nF 25V X5R GND
FMC_VADJ C64 100nF 25V X5R GND

U11 SN74AVC4T774RSVR
VCCA 14, VCCB 13
A1 1, A2 2, A3 3, A4 4
B1 12, B2 11, B3 10, B4 9
OE 7, GND 8
DIR1 15, DIR2 16, DIR3 5, DIR4 6
FPGA_LED1_VT
FPGA_LED2_VT
FPGA_LED3_VT
FPGA_LED4_VT

R107 330R 1% FPGA_LED9
D9 LED Green SML-P11MTT86 GND

R106 330R 1% FPGA_LED8
D8 LED Green SML-P11MTT86 GND

R105 330R 1% FPGA_LED7
D7 LED Green SML-P11MTT86 GND

R104 330R 1% FPGA_LED6
D6 LED Green SML-P11MTT86 GND

3V3 C65 100nF 25V X5R GND
1V8 C66 100nF 25V X5R GND

U21 SN74AVC4T774RSVR
VCCA 14, VCCB 13
A1 1, A2 2, A3 3, A4 4
B1 12, B2 11, B3 10, B4 9
OE 7, GND 8
DIR1 15, DIR2 16, DIR3 5, DIR4 6
FPGA_LED9_VT
FPGA_LED8_VT
FPGA_LED7_VT
FPGA_LED6_VT

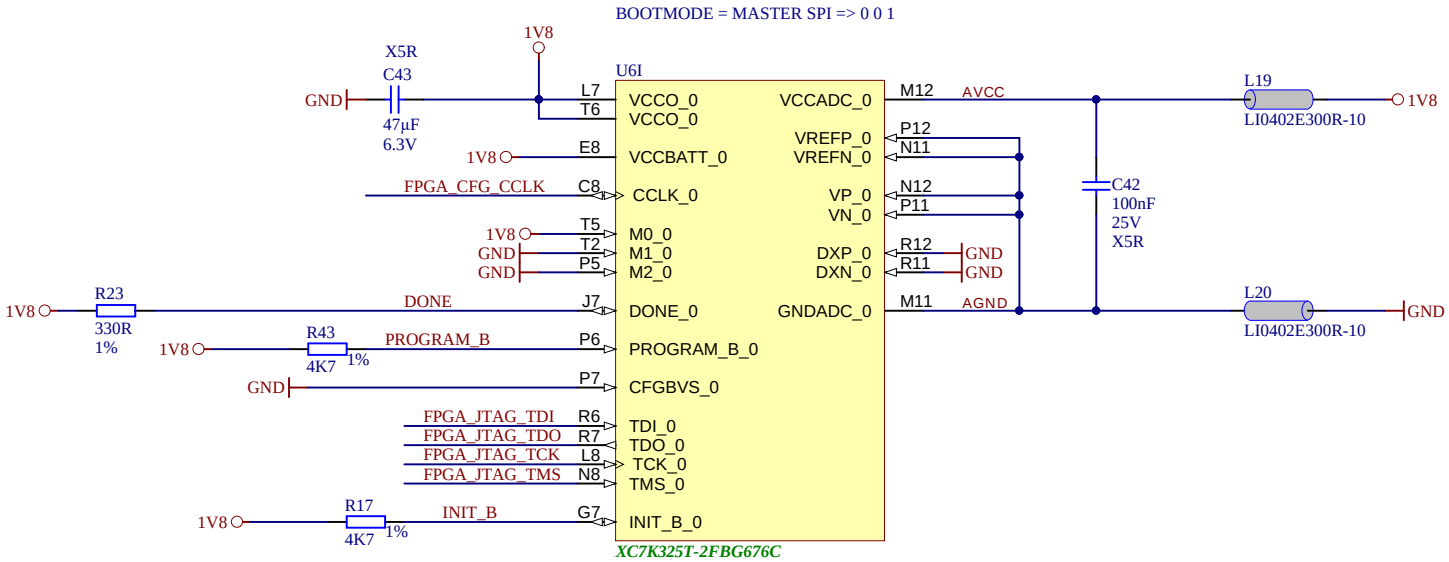
C74 100nF 25V X5R GND
3V3
C75 100nF 25V X5R GND
FMC_VADJ

U22 SN74AVC4T774RSVR
VCCA 14, VCCB 13
A1 1, A2 2, A3 3, A4 4
B1 12, B2 11, B3 10, B4 9
OE 7, GND 8
DIR1 15, DIR2 16, DIR3 5, DIR4 6
FPGA_LED5
FPGA_LED10
FPGA_LED5_VT
FPGA_LED10_VT

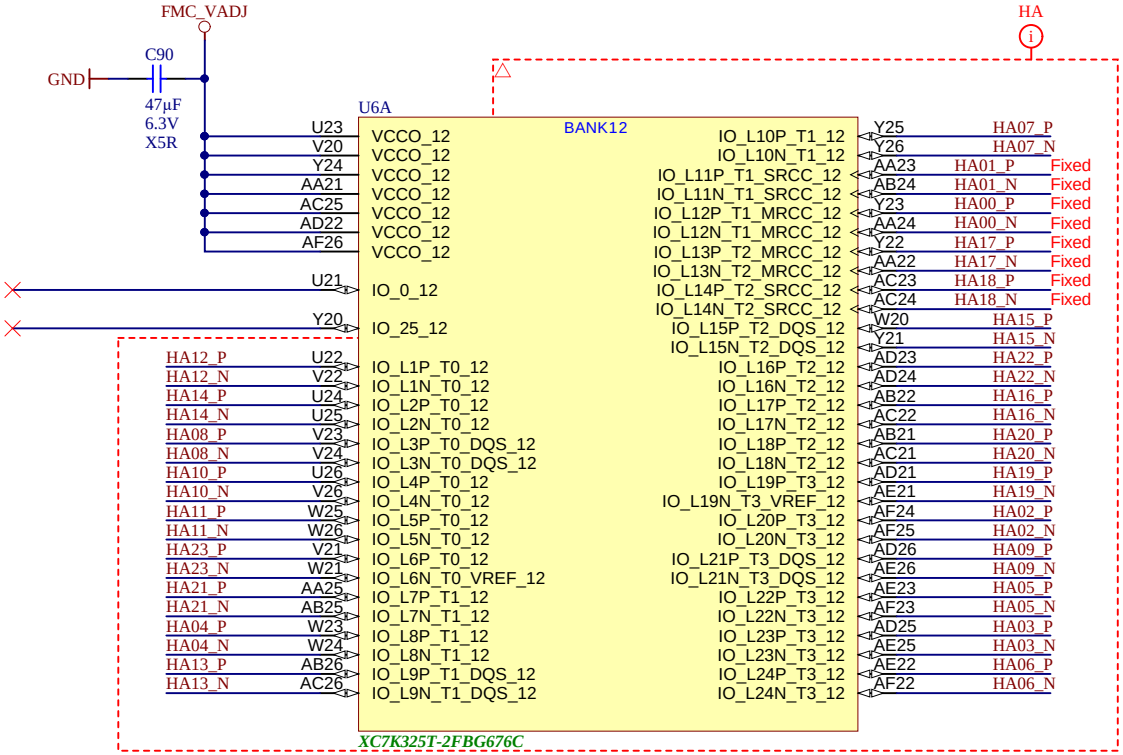
R103 330R 1% D5 LED Green SML-P11MTT86 GND
R108 330R 1% D10 LED Green SML-P11MTT86 GND

trenz electronic

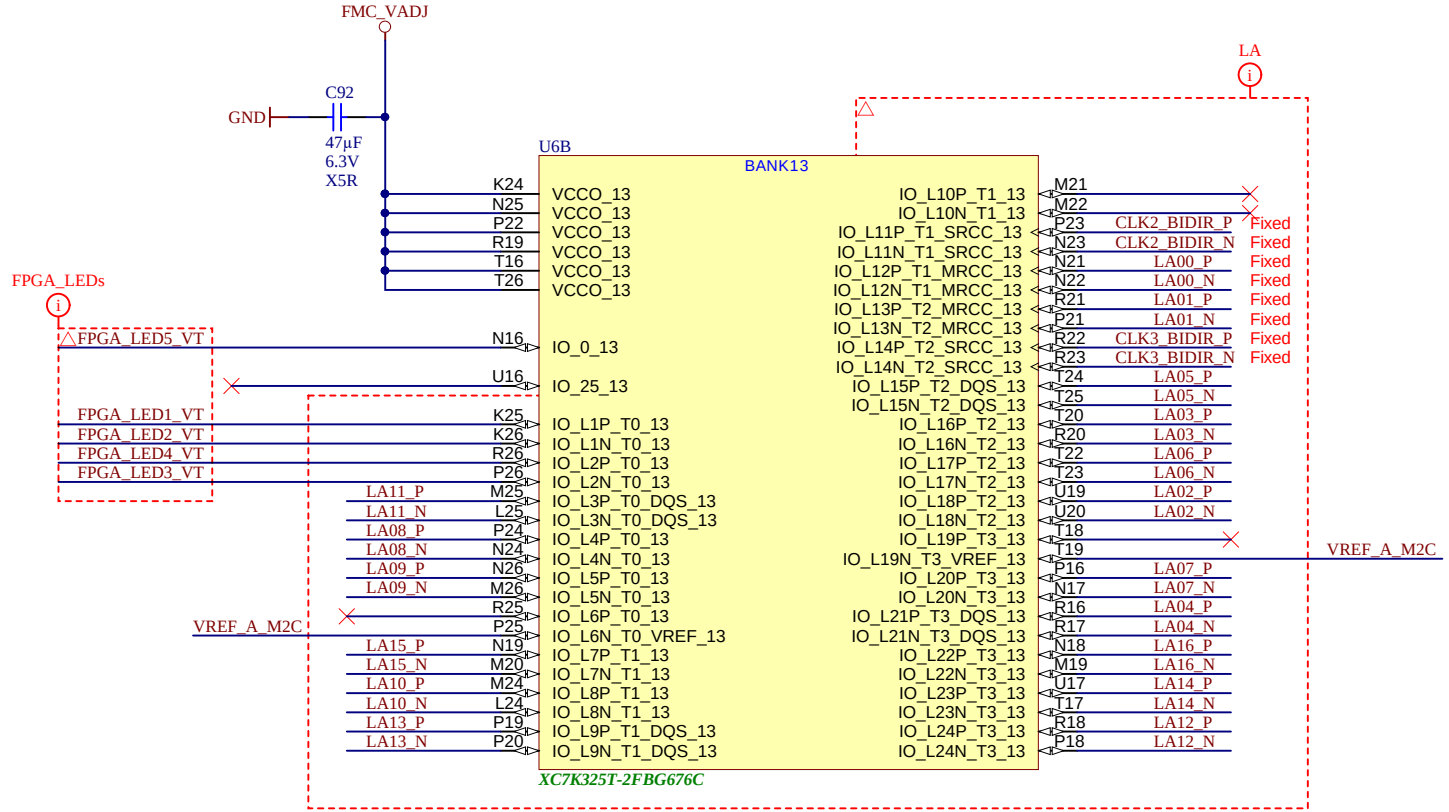
Title: TEF1001 - FPGA			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page9 of 33
Filename: FPGA.SchDoc			



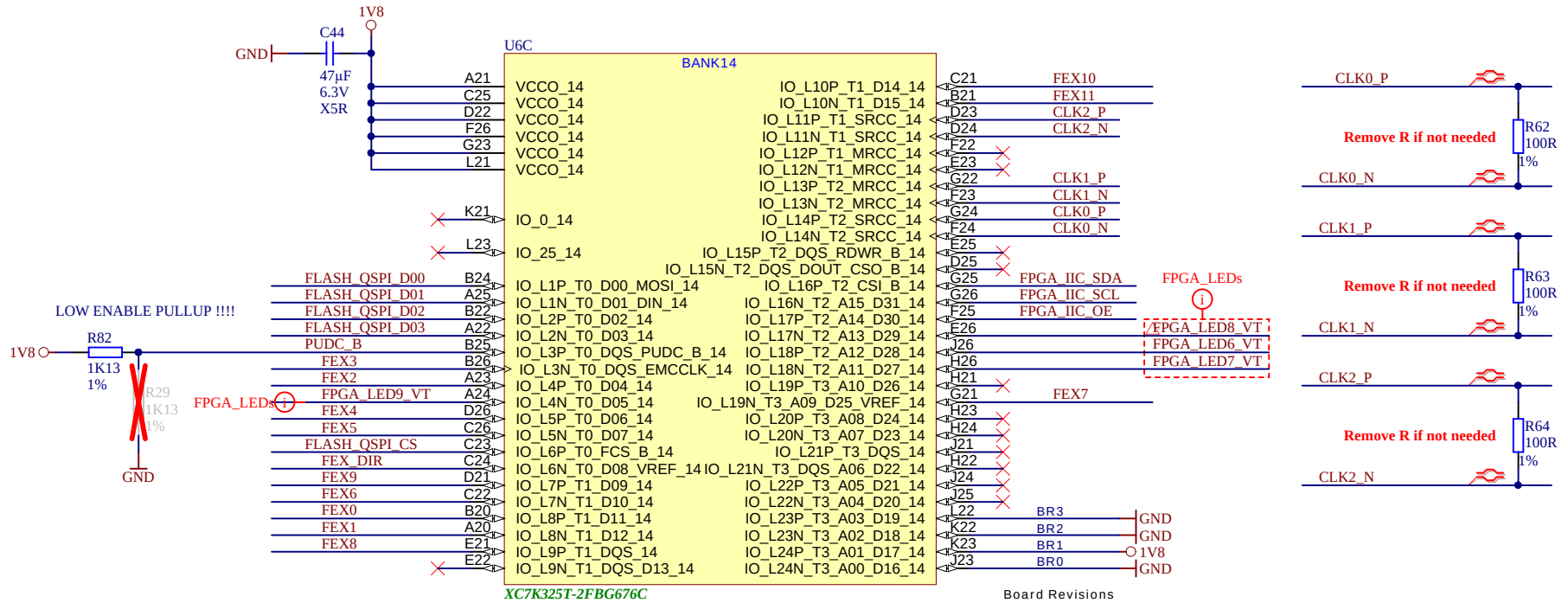
trenz electronic	Title: TEF1001 - FPGA_CFG		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page10 of 33
Filename: FPGA_CFG.SchDoc			



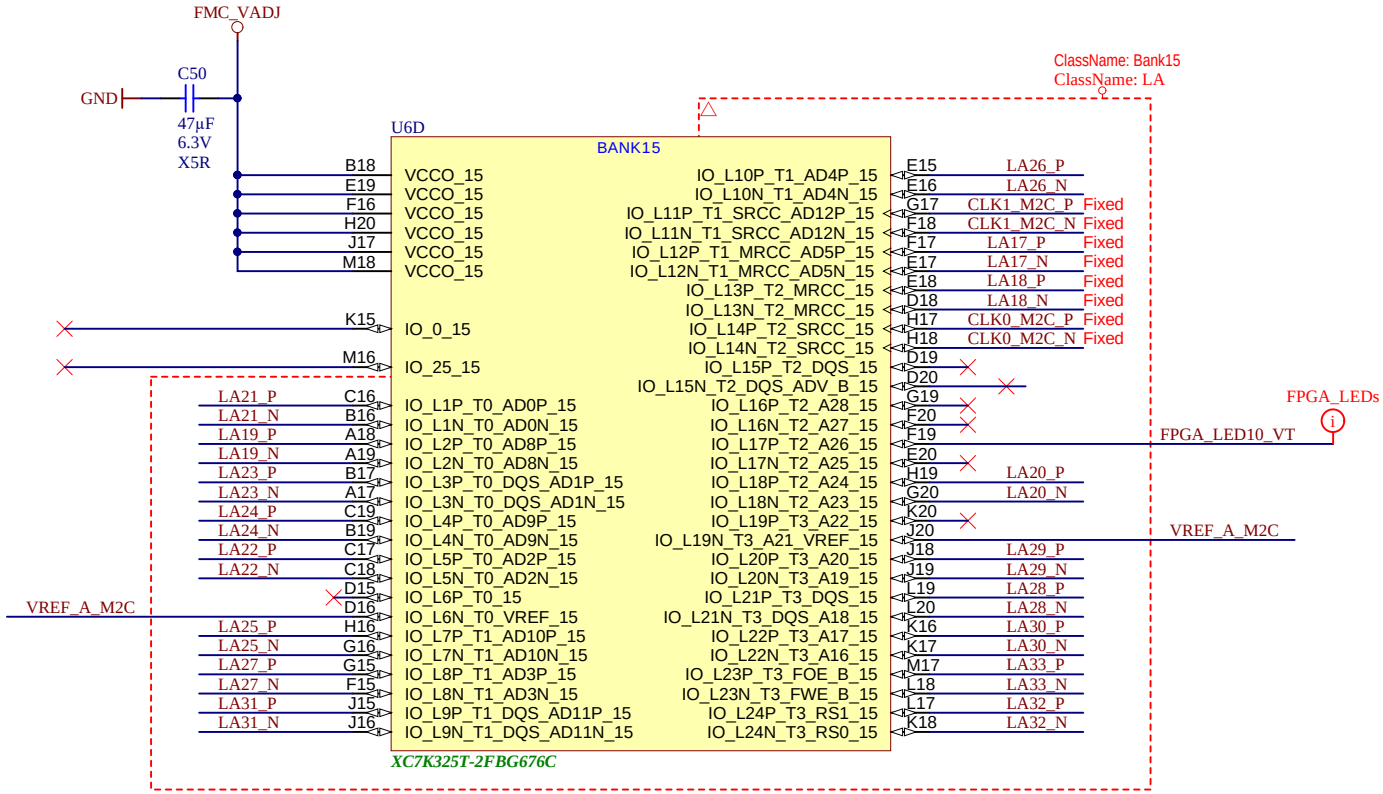
trenz electronic	Title: TEF1001 - FPGA_BANK_12		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page11 of 33
Filename: FPGA_BANK_12.SchDoc			



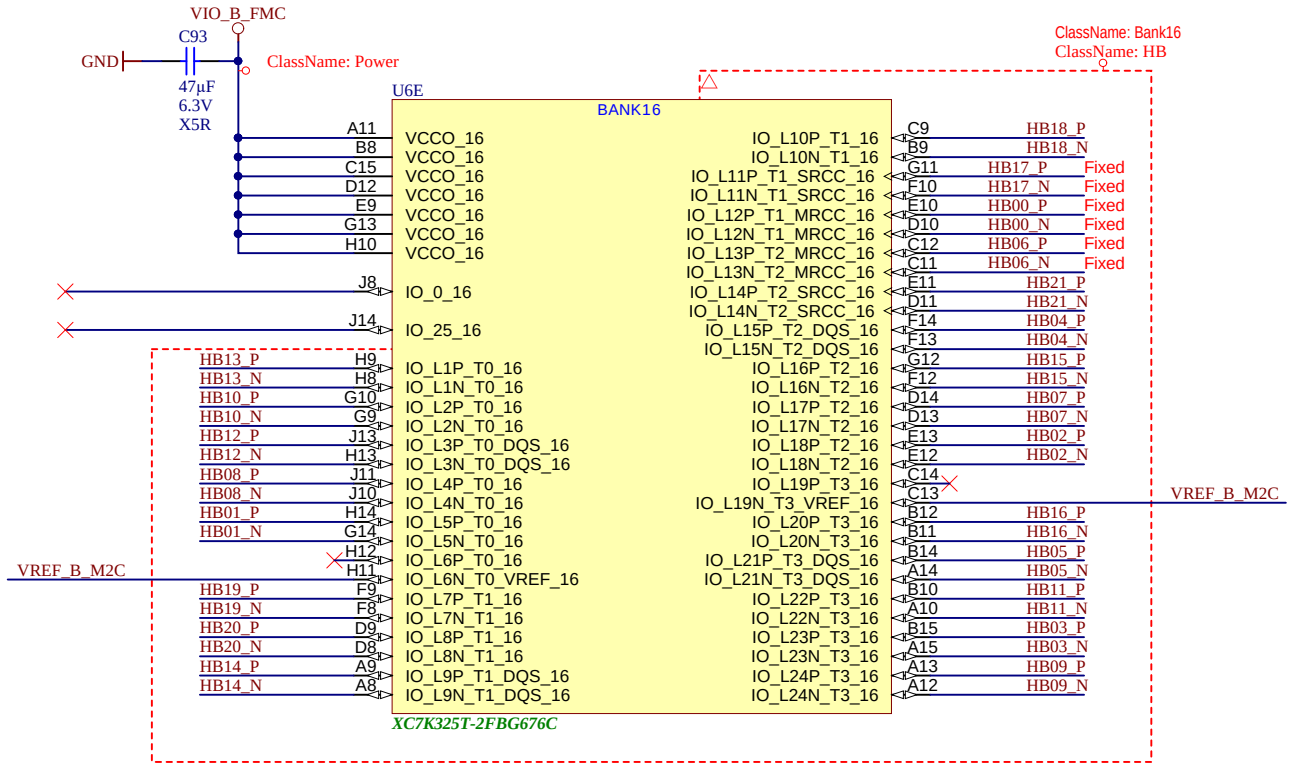
Title: TEF1001 - FPGA_BANK_13			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page12 of 33
Filename: FPGA_BANK_13.SchDoc			



	Title: TEF1001 - FPGA_BANK_14		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page13 of 33
Filename: FPGA_BANK_14.SchDoc			

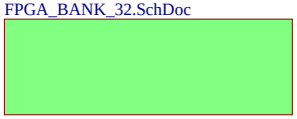


Title: TEF1001 - FPGA_BANK_15			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page14 of 33
Filename: FPGA_BANK_15.SchDoc			

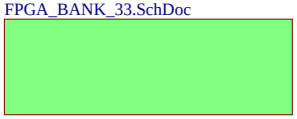


trenz electronic	Title: TEF1001 - FPGA_BANK_16		
	A4	Number: TEF1001 325-2CK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page15 of 33
	Filename: FPGA_BANK_16.SchDoc		

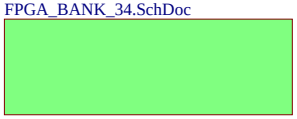
U_FPGA_BANK_32
FPGA_BANK_32.SchDoc



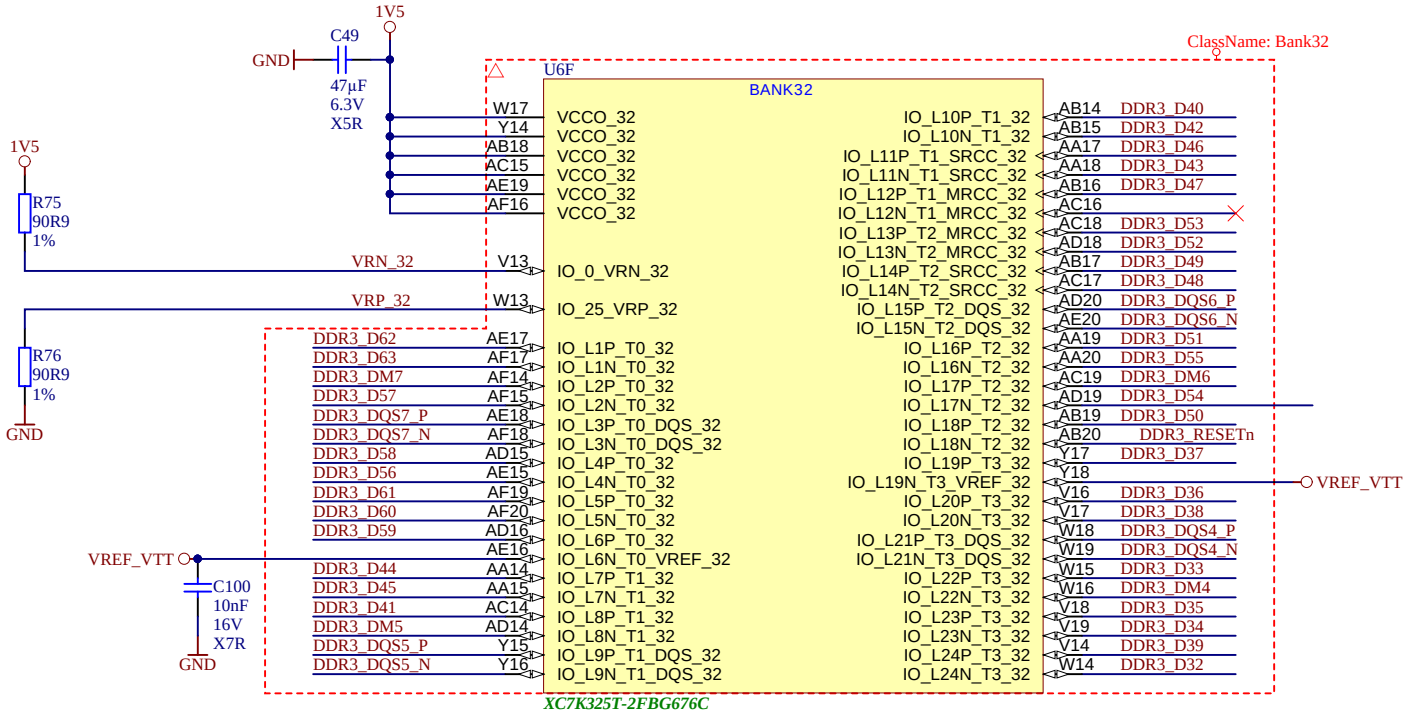
U_FPGA_BANK_33
FPGA_BANK_33.SchDoc



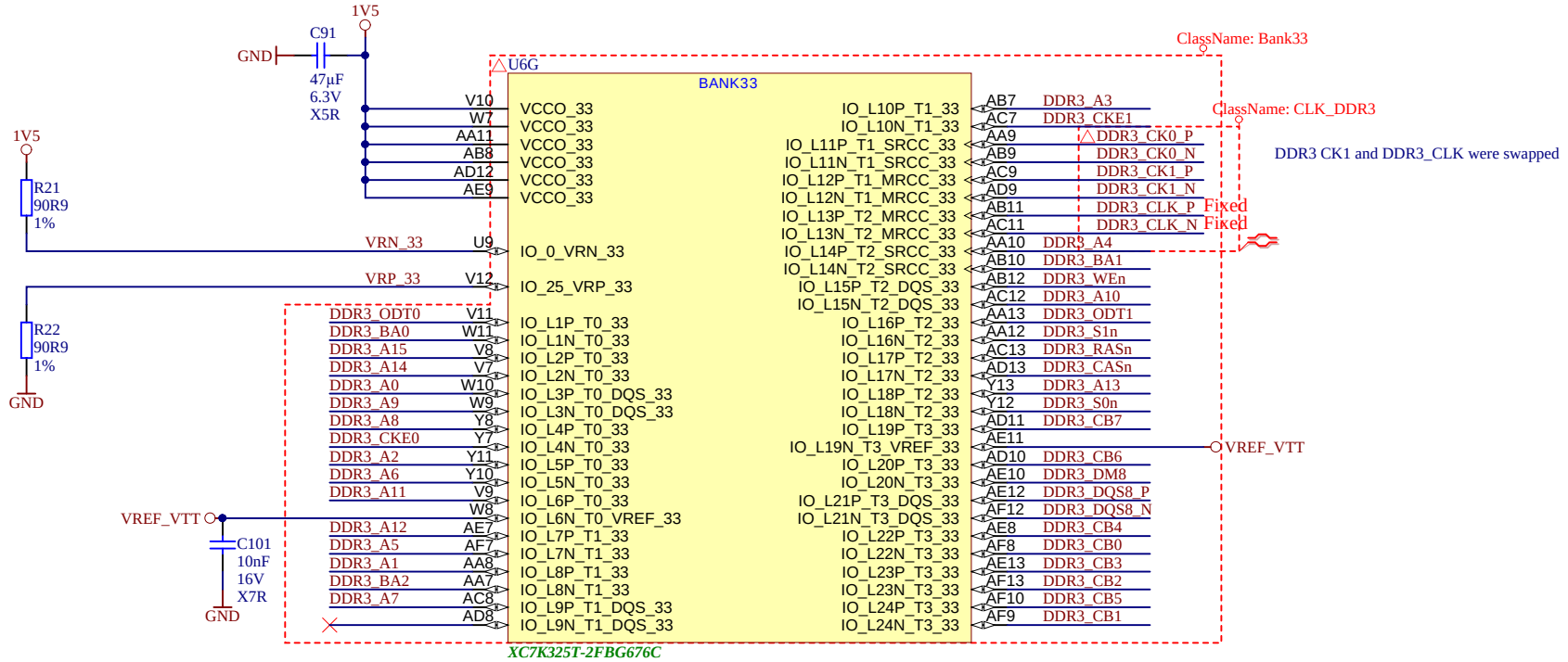
U_FPGA_BANK_34
FPGA_BANK_34.SchDoc



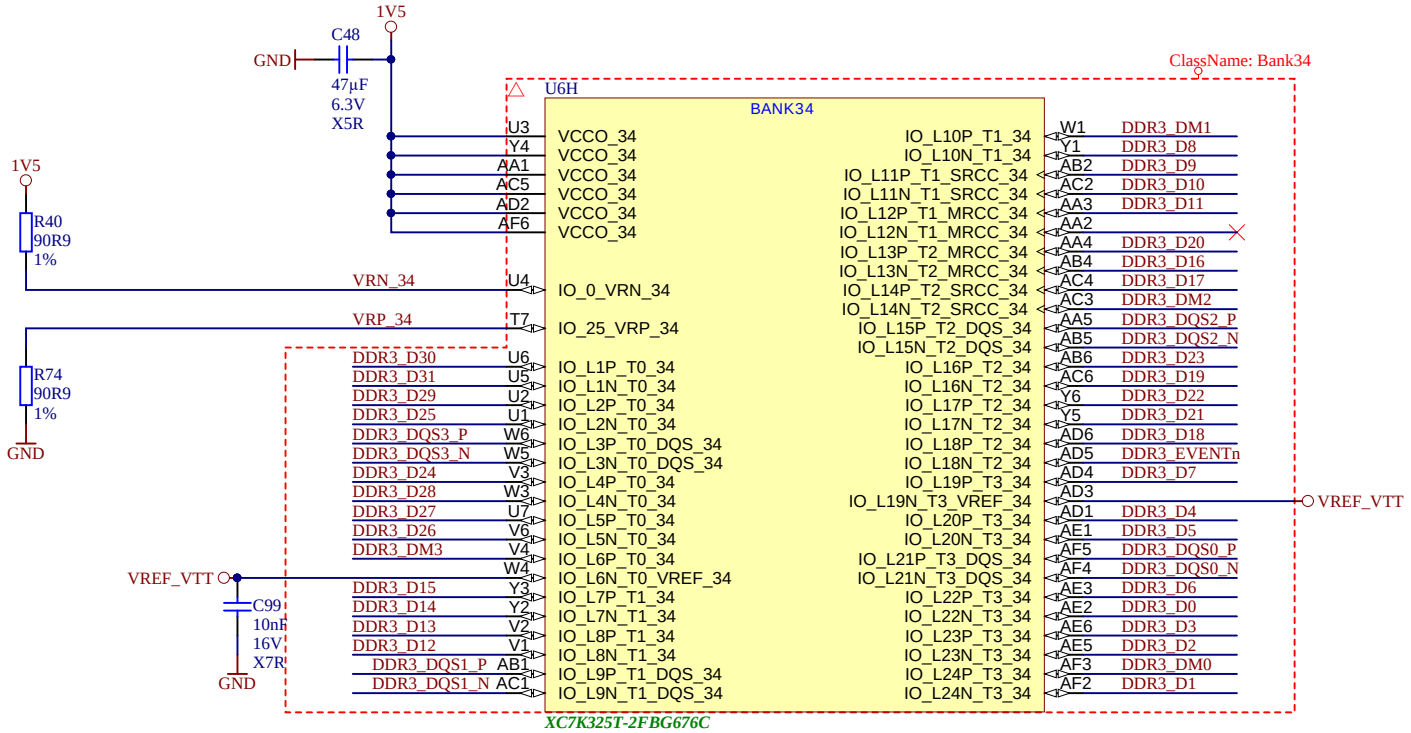
trenz electronic	Title: TEF1001 - DDR_BANKS		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page16 of 33
Filename: DDR_Banks.SchDoc			



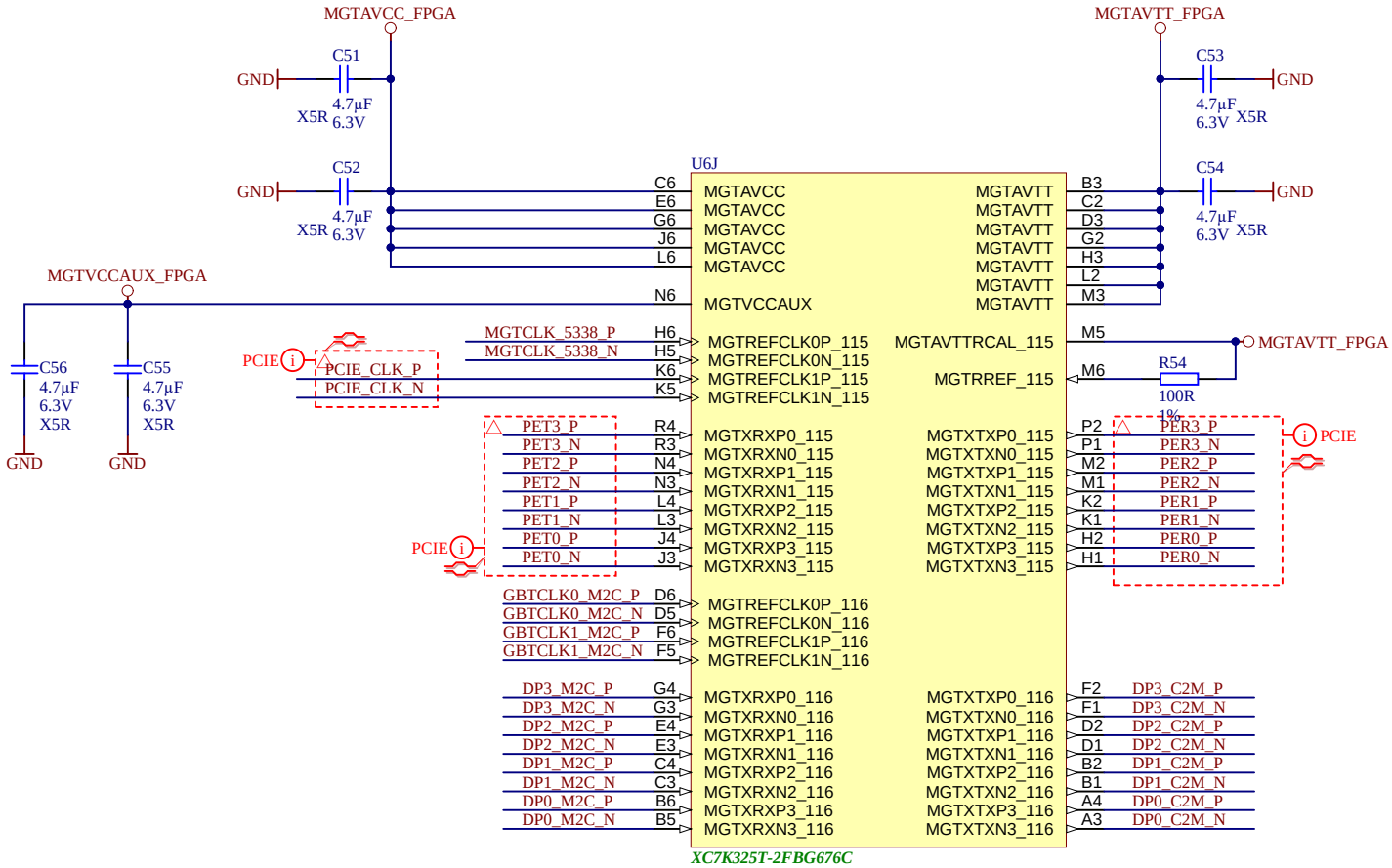
trenz electronic	Title: TEF1001 - FPGA_BANK_32		
	A4	Number: TEF1001 325-2CK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page17 of 33
	Filename: FPGA_BANK_32.SchDoc		



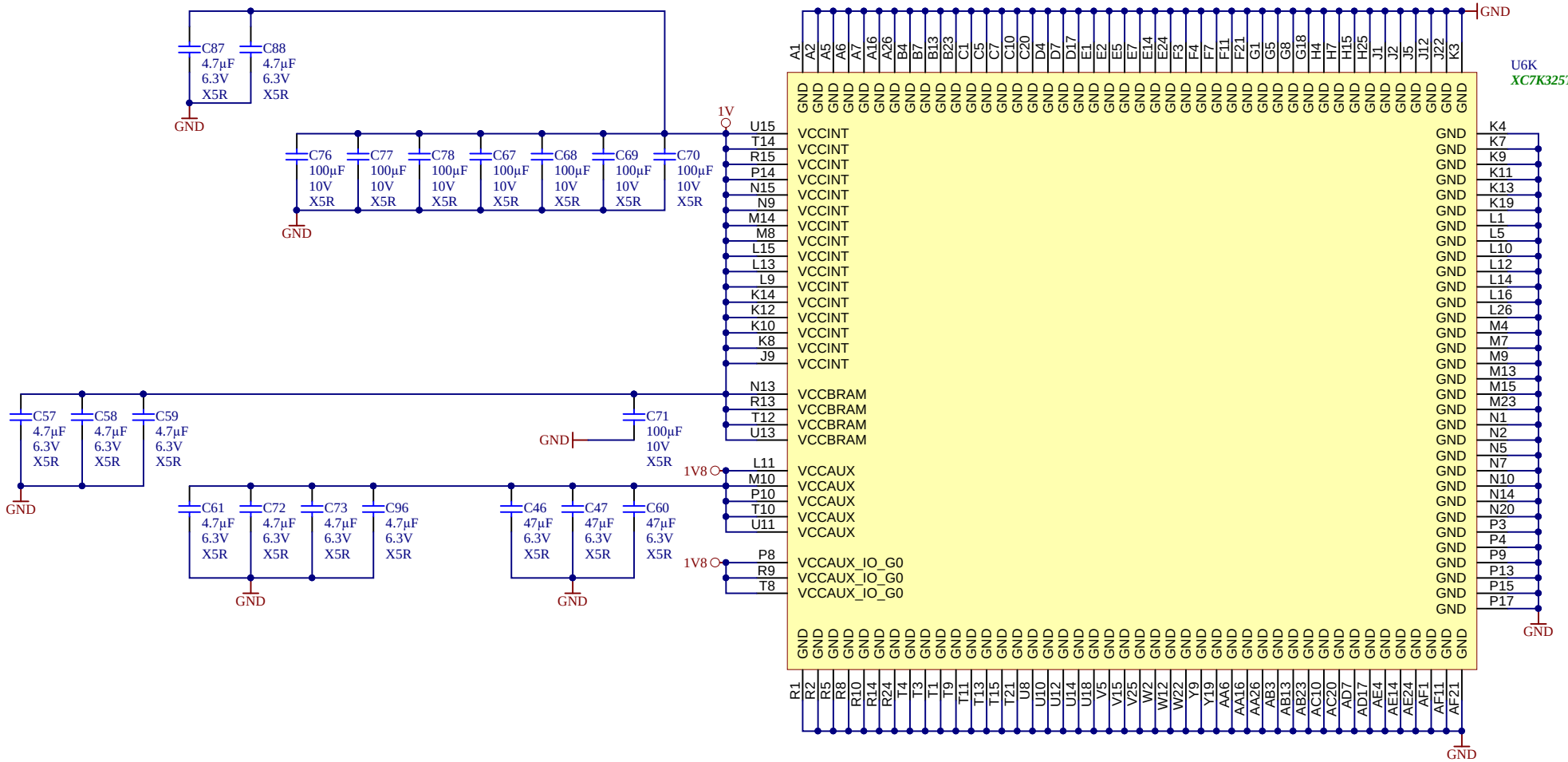
trenz electronic	Title: TEF1001 - FPGA_BANK_33		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page18 of 33
Filename: FPGA_BANK_33.SchDoc			



trenz electronic	Title: TEF1001 - FPGA_BANK_34		
	A4	Number: TEF1001 325-2CK	Rev. 02
	Date: 2018-02-26	Copyright: Trenz Electronic GmbH	Page19 of 33
	Filename: FPGA_BANK_34.SchDoc		

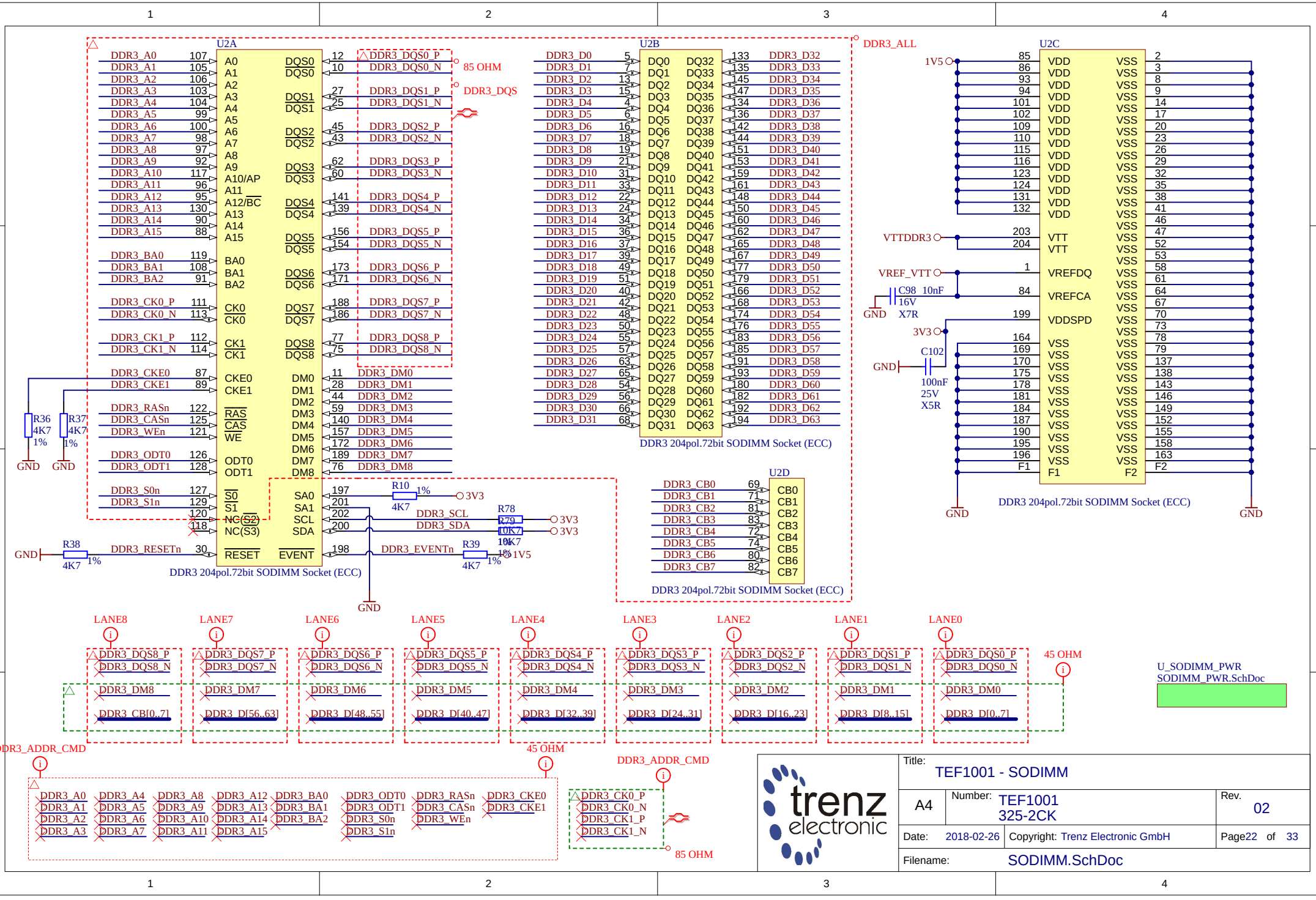


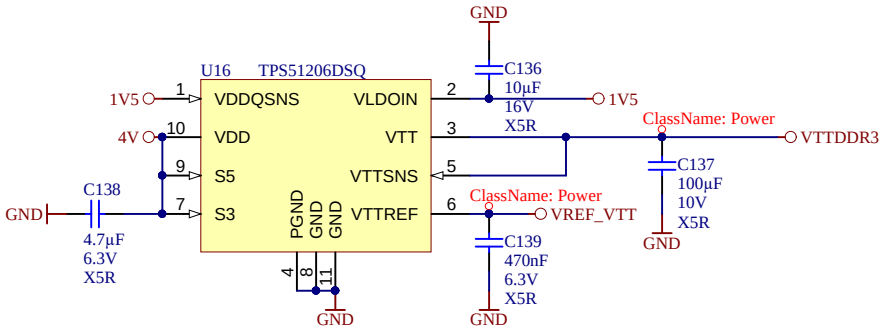
trenz electronic	Title: TEF1001_FPGA_MGT_BANKS		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page20 of 33
Filename: FPGA_MGT_BANKS.SchDoc			

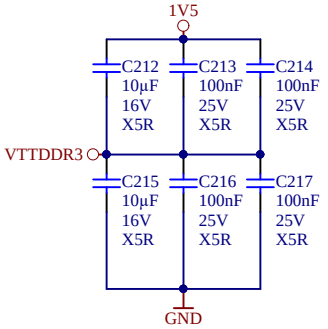


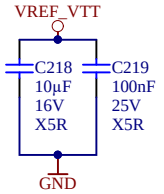
trenz electronic

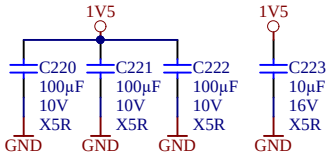
Title: TEF1001 - FPGA_POWER			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page21 of 33
Filename: FPGA_POWER.SchDoc			

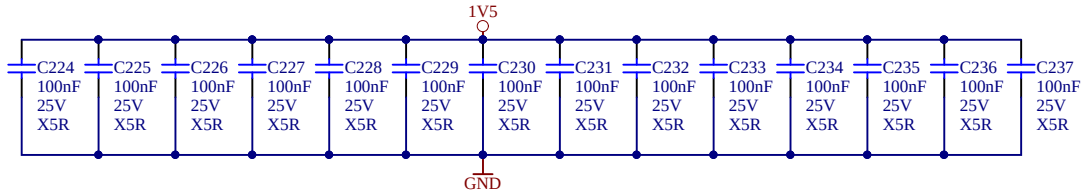

U2A
U2B
U2C
U2D
DDR3_ALL
85 OHM
DDR3_DQS
DDR3 204pol.72bit SODIMM Socket (ECC)
R36 4K7 1%
R37 4K7 1%
R38 4K7 1%
R10 4K7 1%
R39 4K7 1%
R78 10K7 1%
R79 10K7 1%
C98 10nF 16V X7R
C102 100nF 25V X5R
3V3
1V5
GND
VTTDDR3
VREF_VTT
LANE8
LANE7
LANE6
LANE5
LANE4
LANE3
LANE2
LANE1
LANE0
45 OHM
U_SODIMM_PWR
SODIMM_PWR.SchDoc
DDR3_ADDR_CMD
Title: TEF1001 - SODIMM
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page22 of 33
Filename: SODIMM.SchDoc











trenz electronic	Title: TEF1001 - SODIMM_PWR		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page23 of 33
Filename: SODIMM_PWR.SchDoc			

U_PWR_4V_1V5
PWR_4V_1V5.SchDoc

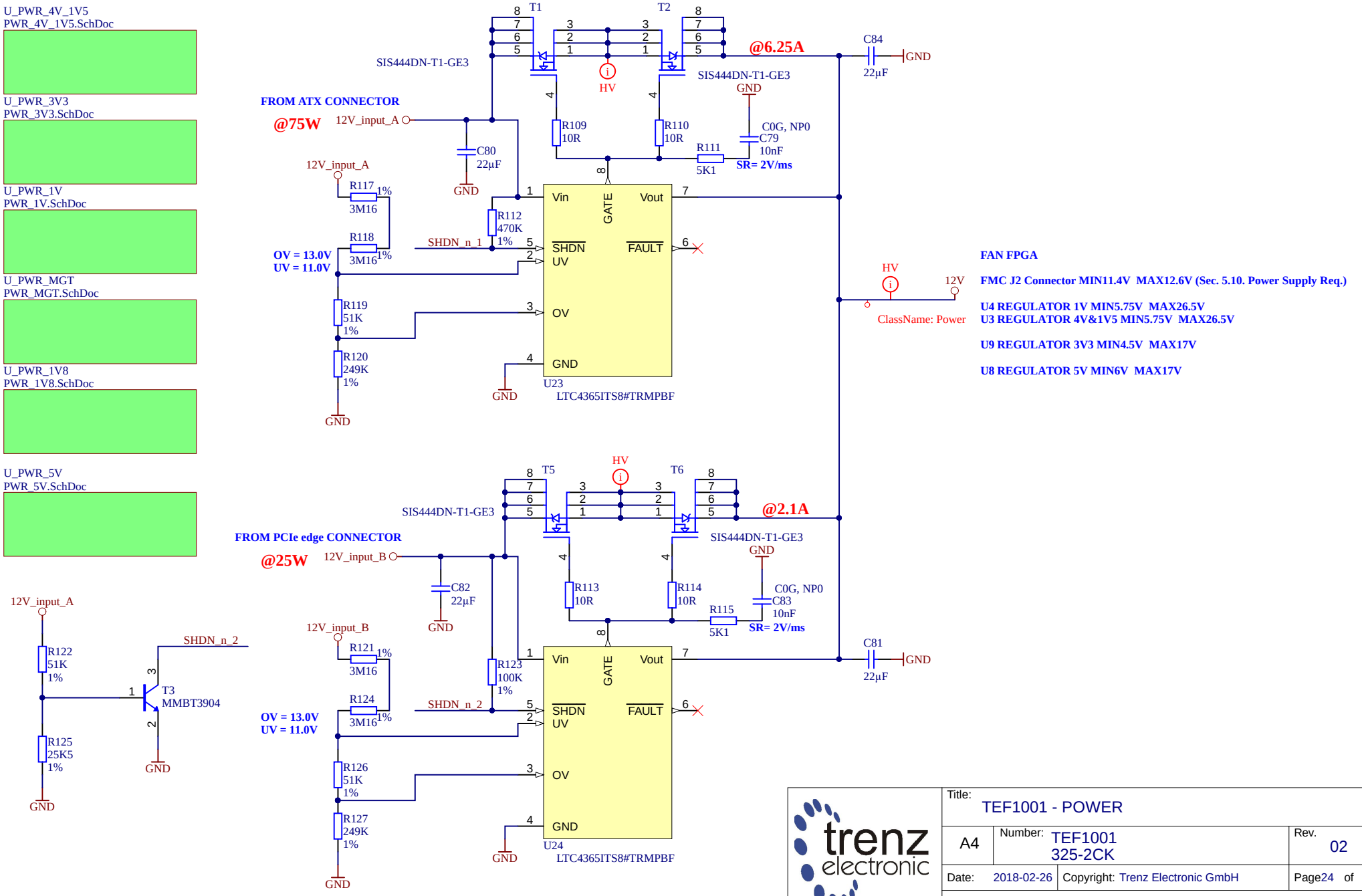
U_PWR_3V3
PWR_3V3.SchDoc

U_PWR_1V
PWR_1V.SchDoc

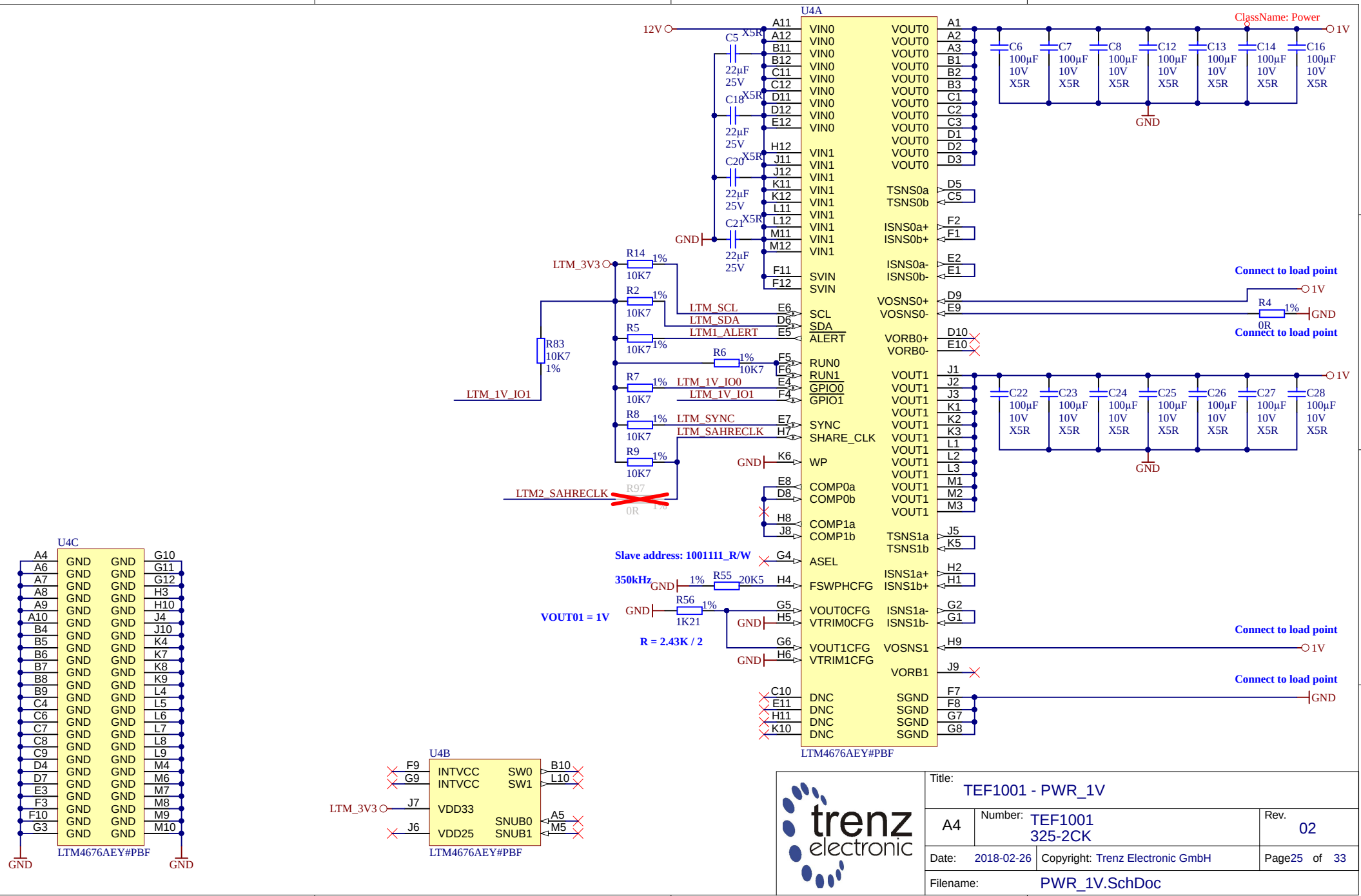
U_PWR_MGT
PWR_MGT.SchDoc

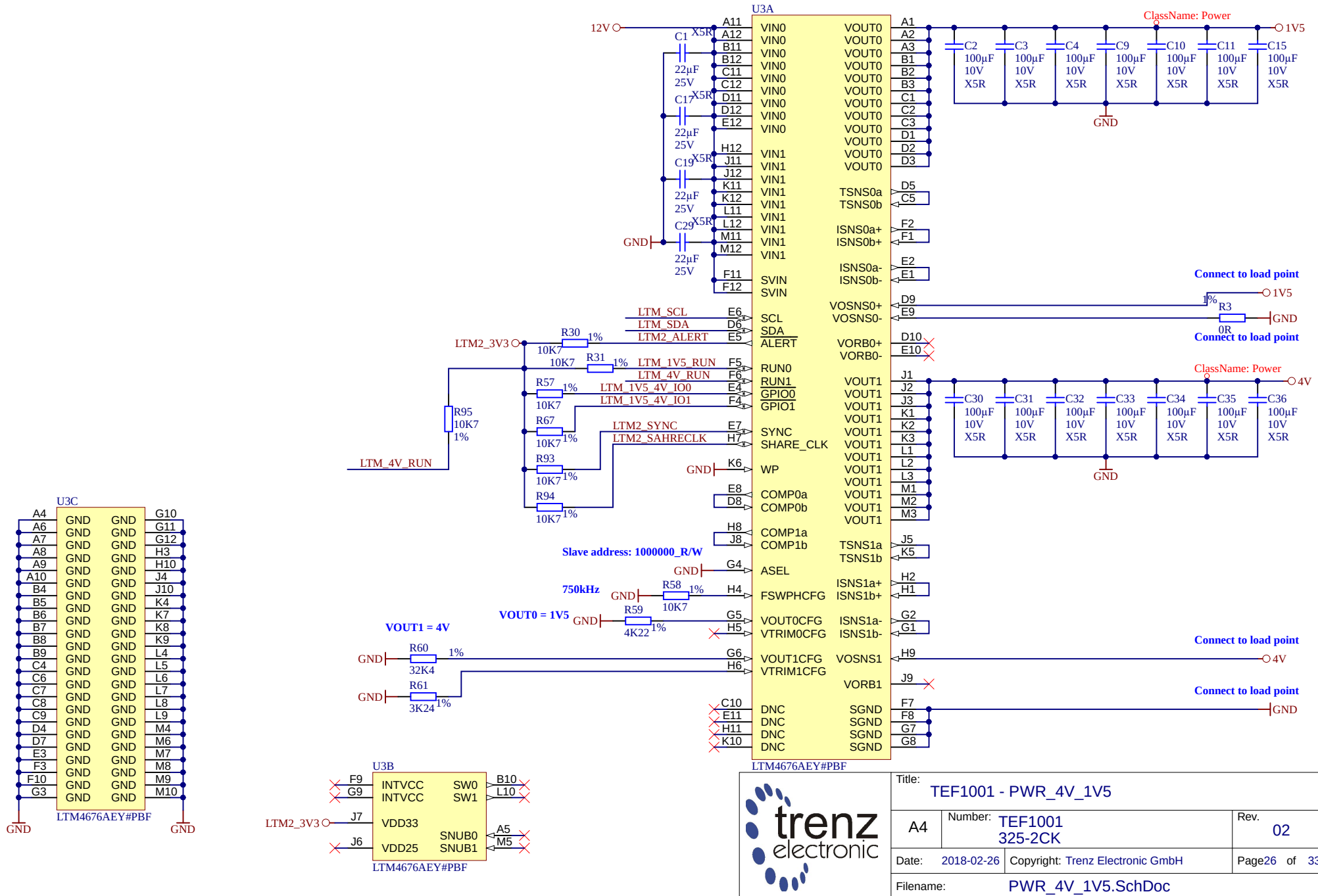
U_PWR_1V8
PWR_1V8.SchDoc

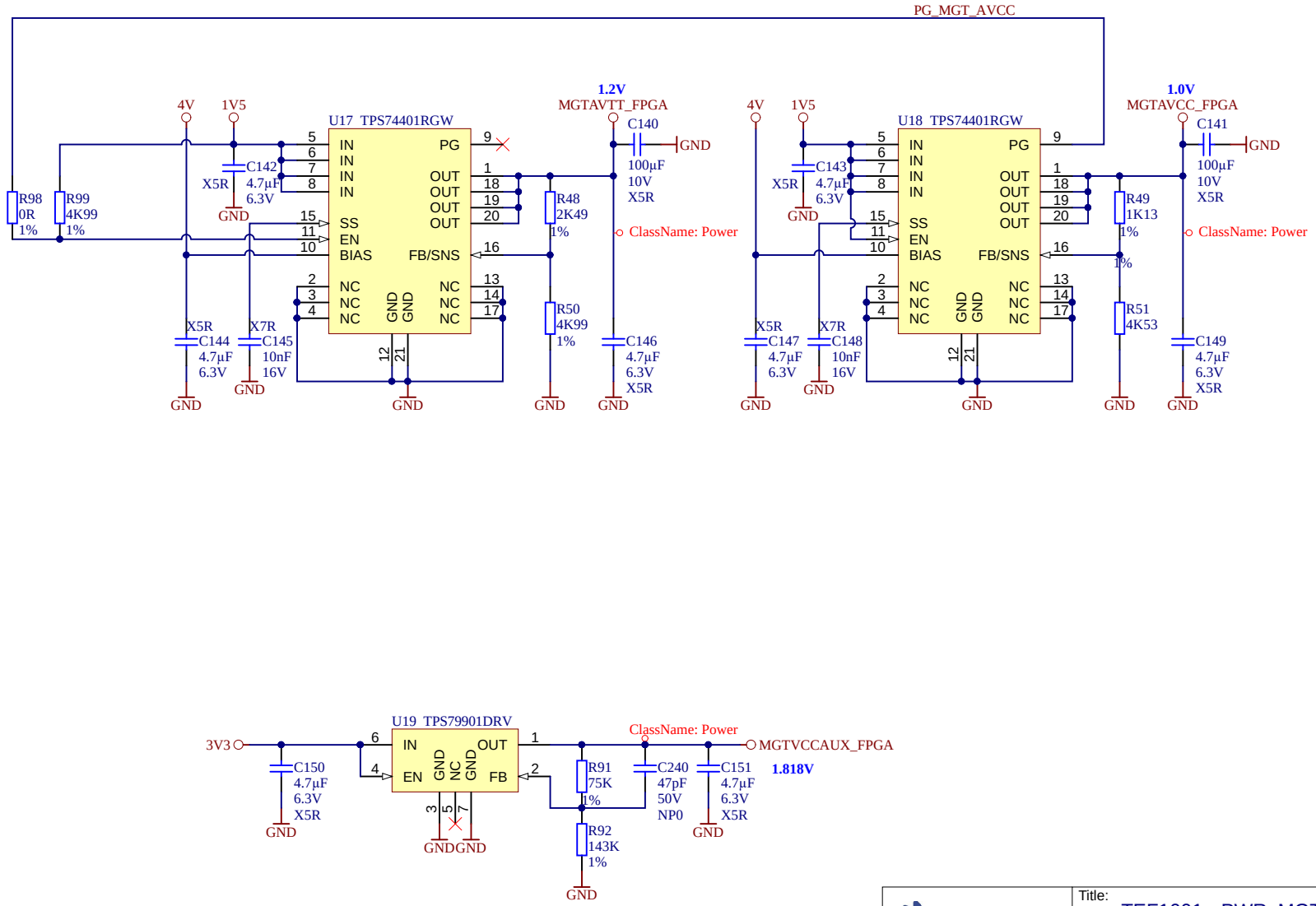
U_PWR_5V
PWR_5V.SchDoc



Title: TEF1001 - POWER			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page24 of 33
Filename: POWER.SchDoc			

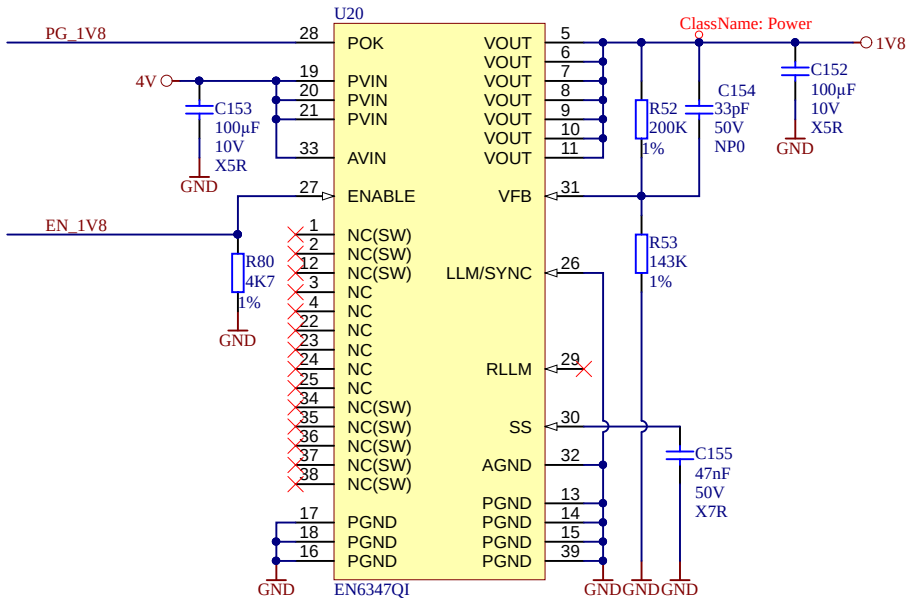

U4A
LTM4676AEY#PBF
U4C
LTM4676AEY#PBF
U4B
LTM4676AEY#PBF
12V
1V
GND
LTM_3V3
LTM_1V_IO1
LTM2_SAHRECLK
LTM_SCL
LTM_SDA
LTM1_ALERT
LTM_1V_IO0
LTM_SYNC
LTM_SAHRECLK
Slave address: 1001111_R/W
350kHz
VOUT01 = 1V
R = 2.43K / 2
ClassName: Power
Connect to load point
Title: TEF1001 - PWR_1V
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page25 of 33
Filename: PWR_1V.SchDoc


U3A
LTM4676AEY#PBF
U3C
LTM4676AEY#PBF
U3B
LTM4676AEY#PBF
12V
GND
LTM2_3V3
LTM_4V_RUN
LTM_SCL
LTM_SDA
LTM2_ALERT
LTM_1V5_RUN
LTM_4V_RUN
LTM_1V5_4V_IO0
LTM_1V5_4V_IO1
LTM2_SYNC
LTM2_SAHRECLK
Slave address: 1000000_R/W
750kHz
VOUT0 = 1V5
VOUT1 = 4V
ClassName: Power
1V5
4V
Connect to load point
Title: TEF1001 - PWR_4V_1V5
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page26 of 33
Filename: PWR_4V_1V5.SchDoc

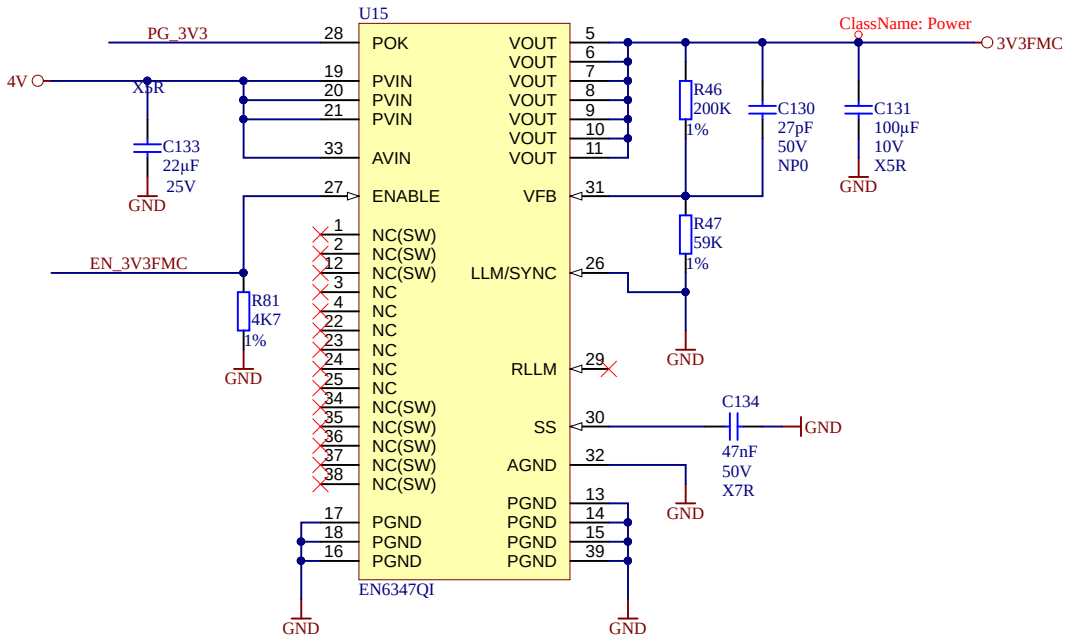


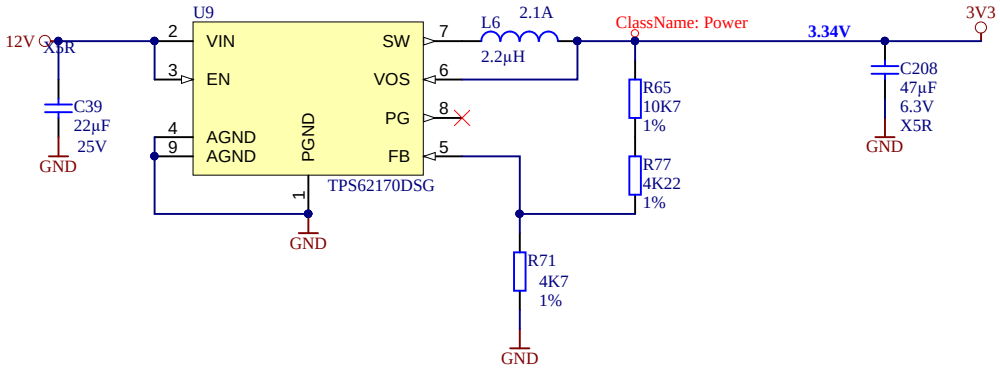
trenz electronic

Title: TEF1001 - PWR_MGT			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page27 of 33
Filename: PWR_MGT.SchDoc			

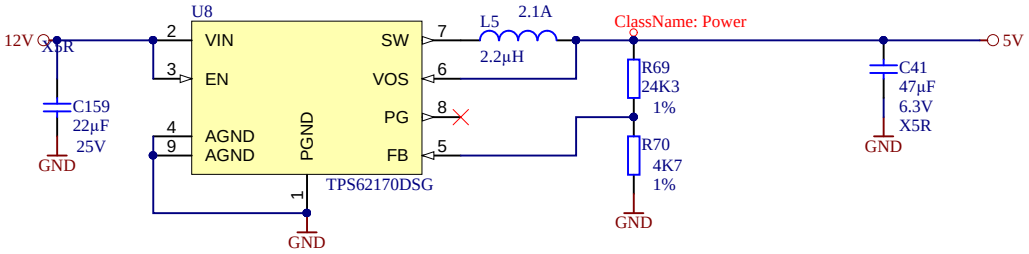


trenz electronic	Title: TEF1001 - PWR_1V8		
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page28 of 33
Filename: PWR_1V8.SchDoc			

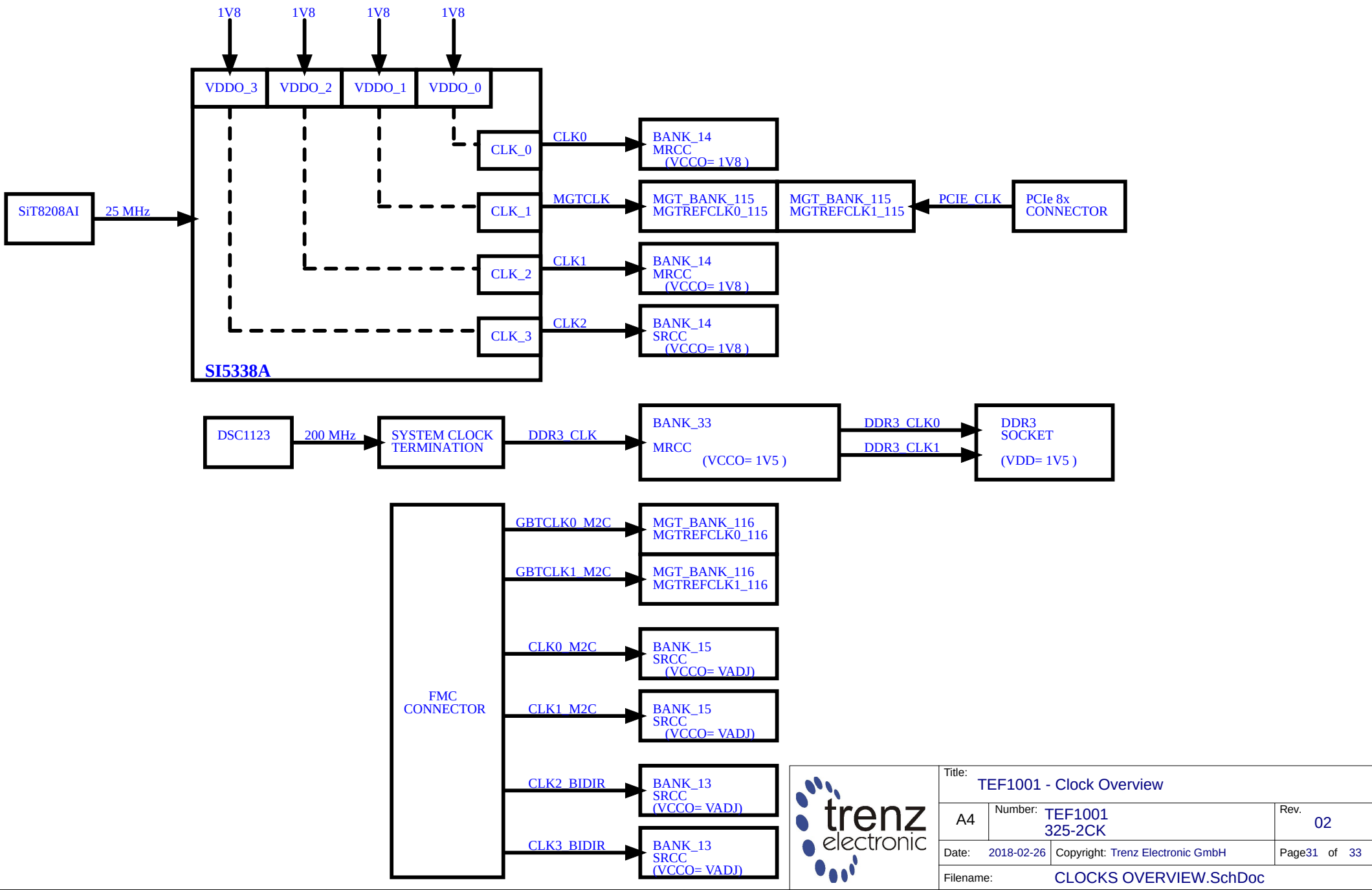




Title: TEF1001 - PWR_3V3			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page29 of 33
Filename: PWR_3V3.SchDoc			

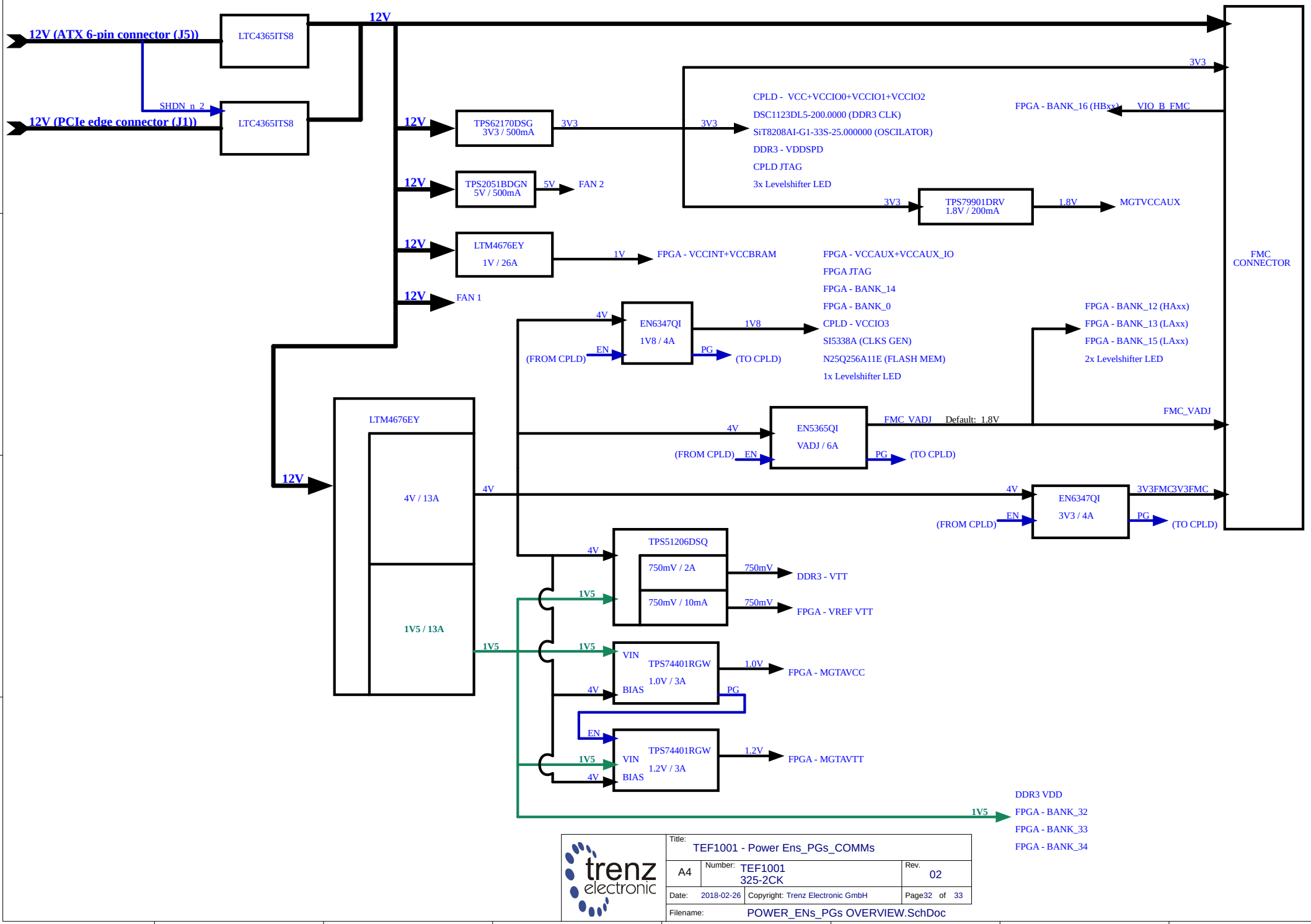


Title: TEF1001 - PWR_5V			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page30 of 33
Filename: PWR_5V.SchDoc			



trenz electronic

Title: TEF1001 - Clock Overview			
A4	Number: TEF1001 325-2CK		Rev. 02
Date: 2018-02-26	Copyright: Trenz Electronic GmbH		Page31 of 33
Filename: CLOCKS OVERVIEW.SchDoc			


12V (ATX 6-pin connector (J5))
12V (PCIe edge connector (J1))
LTC4365ITS8
LTC4365ITS8
SHDN_n_2
12V
12V
TPS62170DSG
3V3 / 500mA
3V3
3V3
CPLD - VCC+VCCIO0+VCCIO1+VCCIO2
DSC1123DL5-200.0000 (DDR3 CLK)
SiT8208AI-G1-33S-25.000000 (OSCILATOR)
DDR3 - VDDSPD
CPLD JTAG
3x Levelshifter LED
FPGA - BANK_16 (HBxx)
VIO_B_FMC
12V
TPS2051BDGN
5V / 500mA
5V
FAN 2
3V3
TPS79901DRV
1.8V / 200mA
1.8V
MGTVCCAUX
12V
LTM4676EY
1V / 26A
1V
FPGA - VCCINT+VCCBRAM
FPGA - VCCAUX+VCCAUX_IO
FPGA JTAG
FPGA - BANK_14
FPGA - BANK_0
CPLD - VCCIO3
SI5338A (CLKS GEN)
N25Q256A11E (FLASH MEM)
1x Levelshifter LED
FMC CONNECTOR
12V
FAN 1
4V
EN6347QI
1V8 / 4A
1V8
(FROM CPLD)
EN
PG
(TO CPLD)
FPGA - BANK_12 (HAxx)
FPGA - BANK_13 (LAxx)
FPGA - BANK_15 (LAxx)
2x Levelshifter LED
LTM4676EY
4V / 13A
1V5 / 13A
12V
4V
4V
EN5365QI
VADJ / 6A
FMC_VADJ
Default: 1.8V
FMC_VADJ
(FROM CPLD)
EN
PG
(TO CPLD)
4V
EN6347QI
3V3 / 4A
3V3FMC3V3FMC
(FROM CPLD)
EN
PG
(TO CPLD)
4V
TPS51206DSQ
750mV / 2A
750mV
DDR3 - VTT
1V5
750mV / 10mA
750mV
FPGA - VREF VTT
1V5
1V5
VIN
TPS74401RGW
1.0V / 3A
1.0V
FPGA - MGTAVCC
4V
BIAS
PG
EN
1V5
VIN
TPS74401RGW
1.2V / 3A
1.2V
FPGA - MGTAVTT
4V
BIAS
DDR3 VDD
1V5
FPGA - BANK_32
FPGA - BANK_33
FPGA - BANK_34
trenz electronic
Title: TEF1001 - Power Ens_PGs_COMMs
A4
Number: TEF1001 325-2CK
Rev. 02
Date: 2018-02-26
Copyright: Trenz Electronic GmbH
Page32 of 33
Filename: POWER_ENs_PGs OVERVIEW.SchDoc

Revision 02:
---
1) added C87, C88 4.7µF
2) C154 incremented from 27pF to 33pF
3) route 12V input from PCIe edge connector, added input power protection circuits for ATX 12V and PCIe edge connector (U23 with T1, T2 and U24 with T5, T6, resistors and capacitors), power priority switch T3, (priority for ATX)
4) added S1 (FMC_VADJ value, and JTAG_EN)
5) T4 and resistors added for reading the FMC_PRSNT_M2C value
6) U25 and capacitors added (FMC FAN)
7) added screws for bracket
8) added 10 x FPGA LEDs D1-D10 via levelshifter (U11, U21, U22)

Revision 02a (2020-04-15):
---
1) VY: New FAN M1, F455B-05MD replaced by F455B-05LD

trenz electronic

Title: TEF1001 - Revision history		
A4	Number: TEF1001 325-2CK	Rev. 02
Date: 2018-11-19	Copyright: Trenz Electronic GmbH	Page33 of 33
Filename: Revision_Changes.SchDoc		