

Evaluating the ADL9005 Wideband, Low Noise Amplifier, Single Positive Supply, 0.01 GHz to 26.5 GHz

FEATURES

2-layer Rogers 4350B evaluation board with heat spreader
End launch, 2.9 mm RF connectors
Through calibration path (depopulated)

EVALUATION KIT CONTENTS

ADL9005-EVALZ evaluation board

EQUIPMENT NEEDED

RF signal generator
RF spectrum analyzer
RF network analyzer
5 V, 200 mA power supply
External dc block
Wideband, bias tee (Marki Microwave BT2-0040)

GENERAL DESCRIPTION

The ADL9005-EVALZ consists of a 2-layer printed circuit board (PCB) fabricated from 10 mil thick, Rogers 4350B, copper clad, mounted to an aluminum heat spreader. The heat spreader assists in providing thermal relief to the device as well as mechanical support to the PCB. Mounting holes on the heat spreader allow attachment to larger heat sinks for improved thermal management.

The RFIN and RFOUT ports on the ADL9005-EVALZ are populated with 2.9 mm, female coaxial connectors, and the respective RF traces have a 50 Ω characteristic impedance. The ADL9005-EVALZ is populated with components suitable for use over the entire -40°C to $+85^{\circ}\text{C}$ operating temperature range of the ADL9005.

To calibrate out board trace losses, a through calibration path, THRU CAL, is provided between the RFINTHRU and THRUCAL connectors. RFINTHRU and THRUCAL must be populated with RF connectors to use the through calibration path. The power voltages and ground path are accessed through surface-mounted technology (SMT) test points.

An external wideband bias tee must be connected to RFOUT to provide bias current and ac coupling on RFOUT. The BT2-0040 from Marki Microwave is recommended.

Alternatively, dc bias can be provided by connecting the dc supply voltage to the VDDOPT SMT test point.

EVALUATION BOARD PHOTOGRAPHS

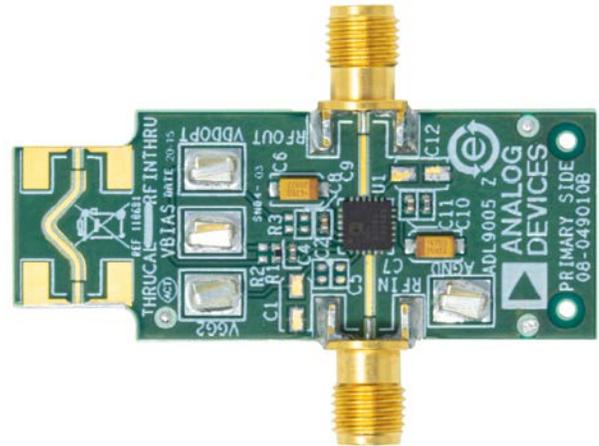


Figure 1. ADL9005-EVALZ Top Side

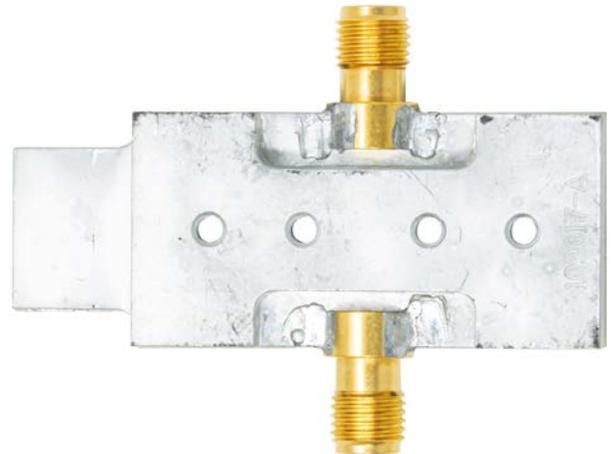


Figure 2. ADL9005-EVALZ Bottom Side

The RF traces are 50 Ω , grounded, coplanar waveguide. The package ground leads and the exposed pad directly connect to the ground plane. Multiple vias are used to connect the top and bottom ground planes with particular focus on the area directly beneath the ground pad to provide adequate electrical conduction and thermal conduction to the heat spreader.

For full details on the ADL9005, see the ADL9005 data sheet, which must be consulted in conjunction with this user guide when using the ADL9005-EVALZ.

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REVISION HISTORY

2/2021—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

PROVIDING DC BIAS THROUGH A CONNECTORIZED BIAS TEE

A 5 V, 200 mA supply is required to provide the bias to the ADL9005 when using the ADL9005-EVALZ. Connect the 5 V supply through an external bias tee, such as the Marki Microwave BT2-0040, to the RFOUT port (see Figure 3). Connect the same 5 V supply to the VBIAS SMT test point. A connectorized dc blocking capacitor must be connected to the RFIN port because there is not an ac coupling capacitor on the RF input trace on the ADL9005-EVALZ. The R1 value (default value is 300 Ω) sets the total current (I_{DQ}) to 80 mA.

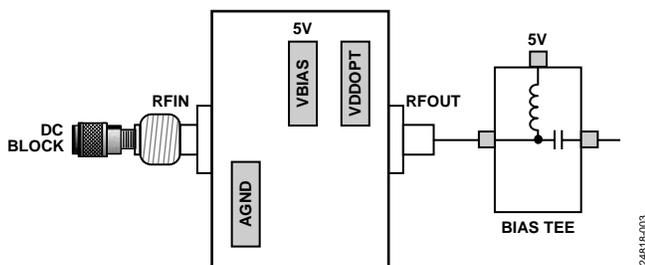


Figure 3. ADL9005-EVALZ Operation Using a Connectorized Bias Tee

Recommended Bias Sequencing

To avoid damaging the device, careful attention must be paid to the sequencing of the RF input, the bias voltage, and the drain bias voltage. The following power-up sequencing is recommended:

1. Connect GND.
2. Increase the voltage on the VBIAS SMT test point and the external bias tee to 5 V.
3. Apply the RF signal.

The following power-down sequencing is recommended:

1. Turn off the RF signal.
2. Reduce the voltage on the VBIAS SMT test point and the external bias tee to 0 V.

PROVIDING DC BIAS THROUGH THE ACG4/ V_{DD2} PIN

An alternative way to bias the ADL9005 when using the ADL9005-EVALZ is by applying 8.5 V to the ACG4/ V_{DD2} pin through the VDDOPT SMT test point and by applying 5 V to the R_{BIAS} pin through the VBIAS SMT test point.

The VDDOPT SMT test point connects directly to the ACG4/ V_{DD2} pin on the ADL9005. The higher 8.5 V supply is required to make up for the voltage drop across an internal resistor so that the internal drain bias voltage is still equal to 5 V.

Applying this 8.5 V supply voltage to the VDDOPT SMT test point removes the need for an external bias tee, which must be replaced with a connectorized dc block on the RFOUT port (see Figure 4).

With 5 V applied to the VBIAS SMT test point and the default value of R1 at 300 Ω , the resulting I_{DQ} is 80 mA. The VBIAS SMT test point can also be connected directly to the 8.5 V supply. However, to do this, the R1 value must be increased to 850 Ω to maintain an I_{DQ} of 80 mA.

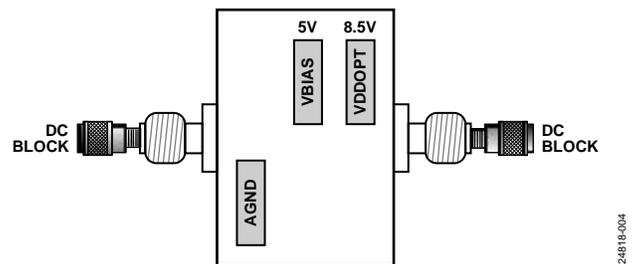


Figure 4. ADL9005-EVALZ Operation with V_{DD} Applied Through the VDDOPT SMT Test Point

Recommended Bias Sequencing when Providing Bias Through the VDDOPT SMT Test Point

The following sequencing is recommended for power-up when providing bias through the VDDOPT SMT test point:

1. Connect GND.
2. Increase the voltage on the VDDOPT SMT test point to 8.5 V.
3. Increase the voltage on the VBIAS SMT test point to 5 V.
4. Apply the RF signal.

The following sequencing is recommended for power-down when providing bias through the VDDOPT SMT test point:

1. Remove the RF signal.
2. Decrease the voltage on the VBIAS SMT test point to 0 V.
3. Decrease the voltage on the VDDOPT SMT test point to 0 V.

THROUGH CALIBRATION PATH

The ADL9005-EVALZ includes a calibration path (see the evaluation board schematic in Figure 6). RFINTHRU and THRUICAL must be populated with RF connectors to use the through calibration path. Figure 5 shows the insertion loss, input return loss and output return loss of the through calibration path. Table 1 lists the insertion loss of the through calibration path.

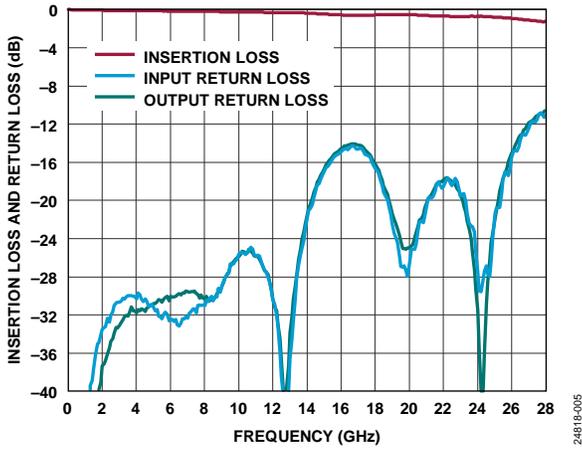


Figure 5. Insertion Loss and Return Loss (Input and Output) of the Through Calibration Path

Table 1. Insertion Loss of the Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
0.01	+0.04
0.25	-0.013
0.5	-0.02
0.75	-0.023
1	-0.04
3	-0.1
5	-0.1
7	-0.2
9	-0.2
11	-0.3
13	-0.3
15	-0.5
17	-0.6
19	-0.5
21	-0.6
23	-0.7
25	-0.8
27	-1.1

EVALUATION BOARD SCHEMATIC AND ARTWORK

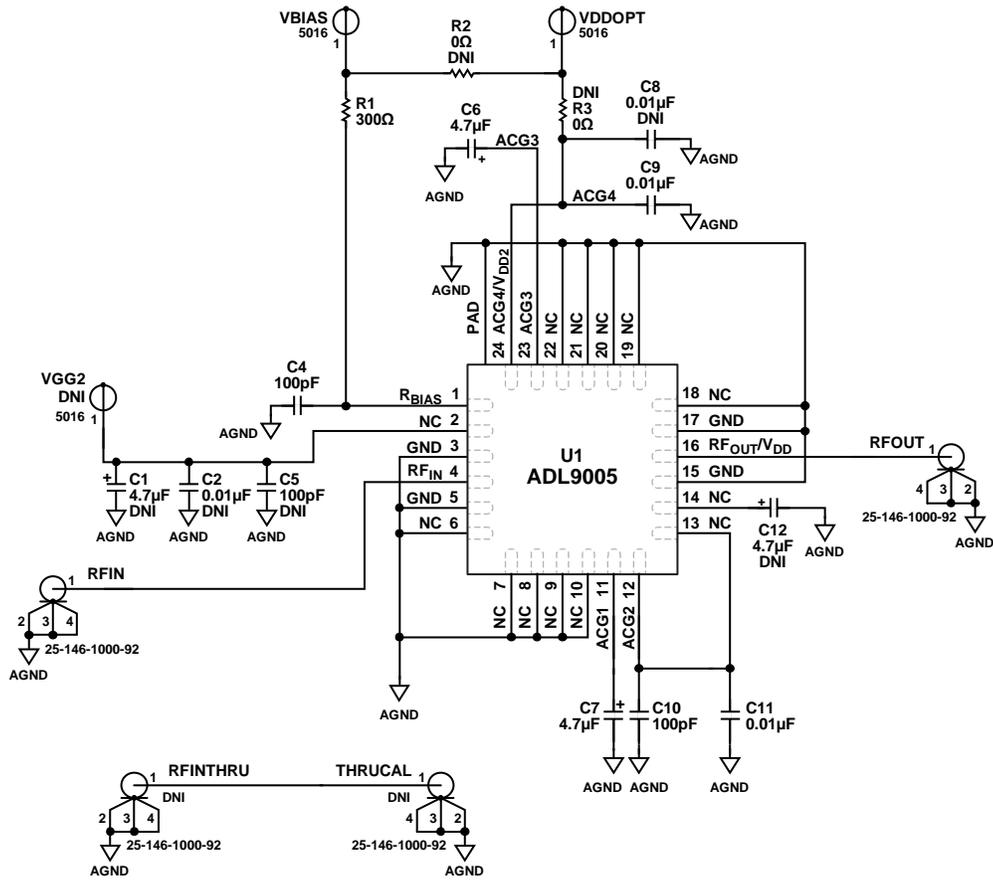


Figure 6. ADL9005-EVALZ Schematic

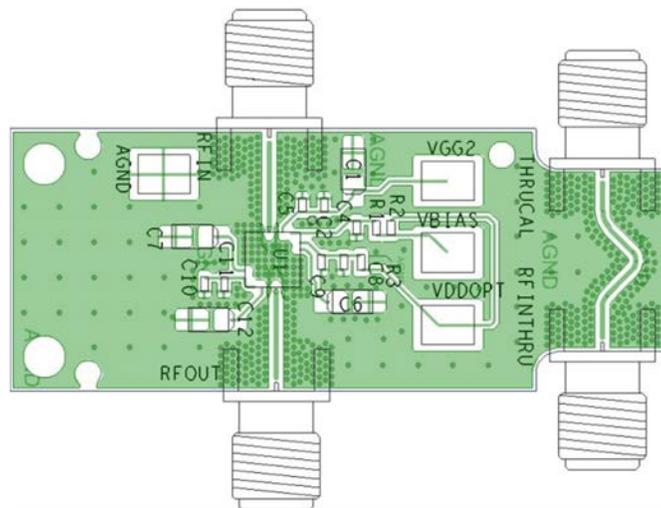


Figure 7. ADL9005-EVALZ Assembly Drawing (RFINTHRU and THRUCAL Not Installed)

ORDERING INFORMATION

BILL OF MATERIALS

Table 2.

Reference Designator	Description	Manufacturer	Manufacturer Number
C1, C12	4.7 μ F capacitors, tantalum, do not install (DNI)	AVX	TAJA475K020RNJ
C2, C8	0.01 μ F capacitors, ceramic, 0402, DNI	KEMET	C0402C103J3RACTU
C4, C10	100 pF capacitors, ceramic, 0402	Samsung	CL05C101JB5NNNC
C5	100 pF capacitors, ceramic, 0402, DNI	Samsung	CL05C101JB5NNNC
C6, C7	4.7 μ F capacitors, tantalum	AVX	TAJA475K020RNJ
C9, C11	0.01 μ F capacitors, ceramic, 0402	KEMET	C0402C103J3RACTU
R1	300 Ω resistor, surface-mounted device (SMD), 0402	MULTICOMP (SPC)	0402WGF3000TCE
R2, R3	0 Ω resistors, SMD, 0402, DNI	Panasonic	ERJ-2GE0R00X
RFINTHRU, THRUCAL	Connectors, K jack edge, DNI	SRI Connector Gage Co.	25-146-1000-92
VBIAS, VDDOPT, AGND	Connectors, SMT test points	Keystone Electronics	5016
RFIN, RFOUT	Connectors, K jack edge	SRI Connector Gage Co.	25-146-1000-92
VGG2	Connectors, SMT test points, DNI	Keystone Electronics	5016
U1	Wideband, low noise amplifier, single positive supply, 0.01 GHz to 26.5 GHz	Analog Devices, Inc.	ADL9005

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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