

# BQ25601D I<sup>2</sup>C Controlled 3-A Single-Cell Battery Charger With USB Charger Detection for High Input Voltage and Narrow Voltage DC (NVDC) Power Path Management

## 1 Features

- High-efficiency, 1.5-MHz, synchronous switch-mode buck charger
  - 92% Charge efficiency at 2 A from 5-V input
  - Optimized for USB voltage input (5 V)
  - Selectable low power Pulse Frequency Modulation (PFM) Mode for light load operations
- Supports USB On-The-Go (OTG)
  - Boost converter with up to 1.2-A output
  - 92% Boost efficiency at 1-A output
  - Accurate Constant Current (CC) limit
  - Soft-start up to 500- $\mu$ F capacitive load
  - Output short circuit protection
  - Selectable low power PFM Mode for light load operations
- Single input to support USB input and high voltage adapters
  - Support 3.9-V to 13.5-V input voltage range with 22-V absolute maximum input voltage rating
  - Programmable input current limit (100 mA to 3.2 a with 100-mA Resolution) to support USB 2.0, USB 3.0 standards and high voltage adapters (IINDPM)
  - Maximum power tracking by input voltage limit up to 5.4 V (VINDPM)
  - VINDPM Threshold automatically tracks battery voltage
  - Auto detect USB BC1.2, SDP, CDP, DCP and non-standard adapters
- High battery discharge efficiency with 19.5-m $\Omega$  battery discharge MOSFET
- Narrow VDC (NVDC) power path management
  - Instant-on works with no battery or deeply discharged battery
  - Ideal diode operation in Battery Supplement Mode
- BATFET Control to support ship mode, wake up and full system reset
- Flexible autonomous and I<sup>2</sup>C Mode for optimal system performance
- High integration includes all MOSFETs, current sensing and loop compensation
- 17- $\mu$ A Low battery leakage current
- High accuracy
  - $\pm$ 0.5% Charge voltage regulation
  - $\pm$ 5% at 1.5-A Charge current regulation

- $\pm$ 10% at 0.9-A Input current regulation
- Safety-Related Certifications:
  - TUV IEC 62368 Certification

## 2 Applications

- Smart phones
- Portable internet devices and accessory

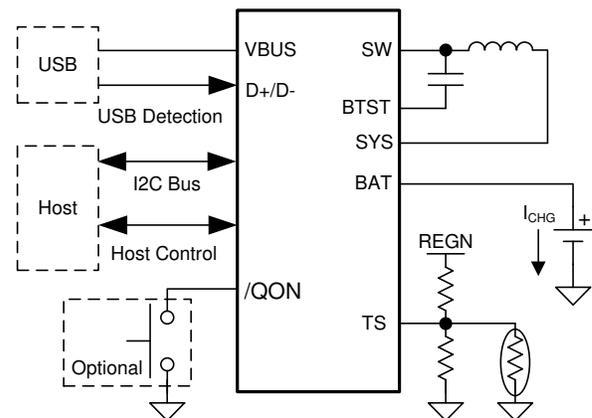
## 3 Description

The BQ25601D device is a highly-integrated 3-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. The I<sup>2</sup>C serial interface with charging and system settings makes the device a truly flexible solution.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ25601D	WQFN (24)	4.00 mm $\times$ 4.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Application**



## Table of Contents

<b>1 Features</b> .....	1	9.2 Functional Block Diagram.....	17
<b>2 Applications</b> .....	1	9.3 Feature Description.....	18
<b>3 Description</b> .....	1	9.4 Device Functional Modes.....	25
<b>4 Revision History</b> .....	2	9.5 Protections.....	29
<b>5 Description (continued)</b> .....	3	9.6 Programming.....	31
<b>6 Device Comparison Table</b> .....	4	9.7 Register Maps.....	34
<b>7 Pin Configuration and Functions</b> .....	5	<b>10 Layout</b> .....	54
<b>8 Specifications</b> .....	7	10.1 Layout Guidelines.....	54
8.1 Absolute Maximum Ratings.....	7	10.2 Layout Example.....	54
8.2 ESD Ratings.....	7	<b>11 Device and Documentation Support</b> .....	56
8.3 Recommended Operating Conditions.....	7	11.1 Device Support.....	56
8.4 Thermal information.....	8	11.2 Documentation Support.....	56
8.5 Electrical Characteristics.....	8	11.3 Receiving Notification of Documentation Updates..	56
8.6 Timing Requirements.....	13	11.4 Support Resources.....	56
8.7 Typical Characteristics.....	14	11.5 Trademarks.....	56
<b>9 Detailed Description</b> .....	16	11.6 Electrostatic Discharge Caution.....	56
9.1 Overview.....	16	11.7 Glossary.....	56

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (December 2020) to Revision B (February 2022)</b>	<b>Page</b>
• Deleted MAX values for $V_{REGN}$ in <a href="#">Section 8.5</a> .....	8

<b>Changes from Revision * (July 2018) to Revision A (December 2020)</b>	<b>Page</b>
• Added Safety-Related Certifications Feature .....	1
• Deleted WEBENCH throughout data sheet.....	1
• Deleted OVPFET_DIS-1 from $I_{BAT}$ and $I_{VBUS\_HIZ}$ test conditions.....	8
• Added text to the end of last paragraph in Converter Power-Up.....	19
• Added text to the end of third paragraph in JEITA Guideline Compliance During Charging Mode.....	23
• Added TS Resistor Network figure in JEITA Guideline Compliance During Charging Mode.....	23
• Changed fault to timer in fourth paragraph in Charging Safety Timer.....	25
• Changed 0111 to 0010 in PN[3:0] in REG0B Field Descriptions.....	45
• Changed $>20\mu\text{F}$ to $\leq 20\mu\text{F}$ in last paragraph in Output Capacitor.....	48

## 5 Description (continued)

The BQ25601D is a highly-integrated 3.0-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer battery. It features fast charging with high input voltage support for a wide range of smart phones, tablets and portable devices. Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery life during discharging phase. Its input voltage and current regulation deliver maximum charging power to battery. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The I<sup>2</sup>C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant high voltage adapter. The device sets default input current limit based on the built-in USB interface. To set the default input current limit, the device uses the built-in USB interface, or takes the result from detection circuit in the system, such as USB PHY device. The device is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device also meets USB On-the-Go (OTG) operation power rating specification by supplying 5.15 V on VBUS with constant current limit up to 1.2A.

The power path management regulates the system slightly above battery voltage but does not drop below 3.5 V minimum system voltage (programmable). With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the power path management automatically reduces the charge current to zero. As the system load continues to increase, the power path discharges the battery until the system power requirement is met. This Supplement Mode prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and overcurrent protections. The thermal regulation reduces charge current when the junction temperature exceeds 110°C (programmable). The STAT output reports the charging status and any fault conditions. Other safety features include battery temperature sensing for charge and boost mode, thermal regulation and thermal shutdown and input UVLO and overvoltage protection. The VBUS\_GD bit indicates if a good power source is present. The INT output immediately notifies host when fault occurs.

The device also provides  $\overline{\text{QON}}$  pin for BATFET enable and reset control to exit low power ship mode or full system reset function.

The device is available in 24-pin, 4 mm × 4 mm × 0.75 mm thin WQFN package.

## 6 Device Comparison Table

	BQ25600(D)	BQ25601(D)	BQ25606
Number of Series Cells	1	1	1
Cell Chemistry	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer
Operation Input Voltage Range (V)	3.9 - 13.5	3.9 - 13.5	3.9 - 13.5
Absolute Max Rating, VBUS (V)	22	22	22
Charge Voltage (V)	3.85 - 4.62	3.85 - 4.62	4.2/4.35/4.4
Charge Current ICHG (A)	3	3	3
Power Path	Yes	Yes	Yes
Discharge Current Rating (A)	6	6	6
I2C / Standalone (I2C Address)	I2C (6BH)	I2C (6BH)	Standalone
USB Detection	BQ25600: PSEL; BQ25600D: D+/D-	BQ25601: PSEL; BQ25601D: D+/D-	D+/D-
BAT Remote Sense	Yes	No	No
Termination Current (A)	60 - 780	60 - 780	5% of ICHG
Precharge Current (A)	60 -780	60 -780	5% of ICHG
Package	WCSP30 - 2x2.4	QFN24 - 4x4	QFN24 - 4x4

## 7 Pin Configuration and Functions

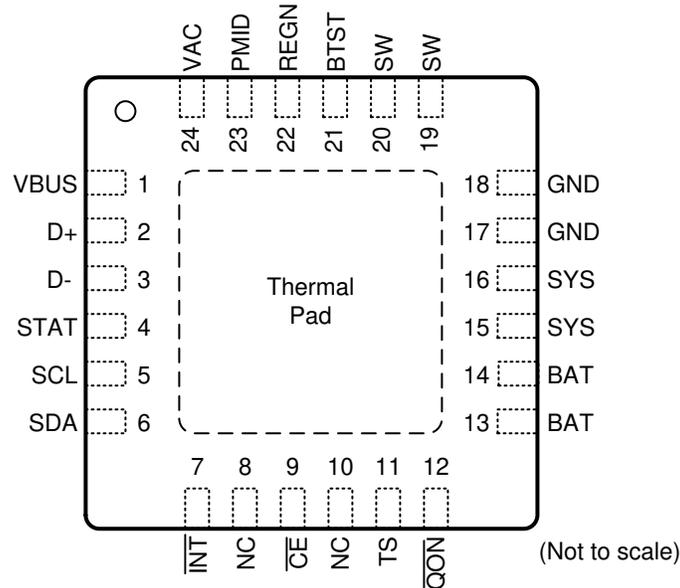


Figure 7-1. RTW Package 24-Pin WQFN Top View

Table 7-1. Pin Functions

Pin		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
BAT	13	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. Connect a 10 $\mu$ F close to the BAT pin.
	14		
BTST	21	P	PWM high side driver positive supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect the 0.047- $\mu$ F bootstrap capacitor from SW to BTST.
CE	9	DI	Charge enable pin. When this pin is driven low, battery charging is enabled.
GND	17	—	Ground pins.
	18		
INT	7	DO	Open-drain interrupt Output. Connect the INT to a logic rail through 10-k $\Omega$ resistor. The $\overline{\text{INT}}$ pin sends an active low, 256- $\mu$ s pulse to host to report charger device status and fault.
NC	8	—	No Connect. Keep the pins float.
	10		
D-	3	AIO	Negative line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
PMID	23	DO	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 $\mu$ F ceramic capacitor on PMID to GND.
D+	2	AIO	Positive line of the USB data line pair. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors
QON	12	DI	BATFET enable/reset control input. When BATFET is in ship mode, a logic low of $t_{\text{SHIPMODE}}$ duration turns on BATFET to exit shipping mode. When VBUS is not plugged-in, a logic low of $t_{\text{QON_RST}}$ (minimum 8 s) duration resets SYS (system power) by turning BATFET off for $t_{\text{BATFET_RST}}$ (minimum 250 ms) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic.
REGN	22	P	LSFET driver and internal supply output. Internally, REGN is connected to the anode of the boost-strap diode. Connect a 4.7- $\mu$ F (10-V rating) ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
SCL	5	DI	I <sup>2</sup> C interface clock. Connect SCL to the logic rail through a 10-k $\Omega$ resistor.
SDA	6	DIO	I <sup>2</sup> C interface data. Connect SDA to the logic rail through a 10-k $\Omega$ resistor.
STAT	4	DO	Open-drain charge status output. Connect the STAT pin to a logic rail via 10-k $\Omega$ resistor. The STAT pin indicates charger status. Collect a current limit resistor and a LED from a rail to this pin. Charge in progress: LOW Charge complete or charger in SLEEP mode: HIGH Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses This pin can be disabled via EN_ICHG_MON[1:0] register bits.

**Table 7-1. Pin Functions (continued)**

Pin		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
SW	19	P	Switching node output. Connected to output inductor. Connect the 0.047- $\mu$ F bootstrap capacitor from SW to BTST.
	20		
SYS	15	P	Converter output connection point. The internal current sensing network is connected between SYS and BAT. Connect a 20 $\mu$ F capacitor close to the SYS pin.
	16		
TS	11	AI	Temperature qualification voltage input to support JEITA profile. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. When TS pin is not used, connect a 10-k $\Omega$ resistor from REGN to TS and connect a 10-k $\Omega$ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
VAC	24	AI	Charge input voltage sense. This pin must be connected to VBUS pin.
VBUS	1	P	Charger input. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID pins. Place a 1- $\mu$ F ceramic capacitor from VBUS to GND close to device.
Thermal Pad	—	P	Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VAC, VBUS (converter not switching) <sup>(2)</sup>	-2	22	V
Voltage Range (with respect to GND)	BTST, PMID (converter not switching) <sup>(2)</sup>	-0.3	22	V
Voltage Range (with respect to GND)	SW	-2	16	V
Voltage Range (with respect to GND)	BTST to SW	-0.3	7	V
Voltage Range (with respect to GND)	D+, D-	-0.3	7	V
Voltage Range (with respect to GND)	REGN, TS, $\overline{CE}$ , BAT, SYS (converter not switching)	-0.3	7	V
Output Sink Current	STAT		6	mA
Voltage Range (with respect to GND)	SDA, SCL, INT, /QON, STAT	-0.3	7	V
Voltage Range (with respect to GND)	PGND to GND (QFN package only)	-0.3	0.3	V
Output Sink Current	INT		6	mA
Operating junction temperature, T <sub>J</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
- (2) VBUS is specified up to 22 V for a maximum of one hour at room temperature

### 8.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>BUS</sub>	Input voltage	3.9		13.5 <sup>(1)</sup>	V
I <sub>in</sub>	Input current (VBUS)			3.25	A
I <sub>SWOP</sub>	Output current (SW)			3.25	A
V <sub>BATOP</sub>	Battery voltage			4.615	V
I <sub>BATOP</sub>	Fast charging current			3.0	A
I <sub>BATOP</sub>	Discharging current (continuous)			6	A
T <sub>A</sub>	Operating ambient temperature	-40		85	°C

- (1) The inherent switching noise voltage spikes should not exceed the absolute maximum voltage rating on either the BTST or SW pins. A tight layout minimizes switching noise.

## 8.4 Thermal information

THERMAL METRIC <sup>(1)</sup>		BQ25601D	UNIT
		RTW (WQFN)	
		24 PinS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	35.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	22.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	11.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	12	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 8.5 Electrical Characteristics

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$  and  $V_{VAC} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>QUIESCENT CURRENTS</b>						
I <sub>BAT</sub>	Battery discharge current (BAT, SW, SYS) in buck mode	V <sub>BAT</sub> = 4.5 V, V <sub>BUS</sub> < V <sub>VAC-UVLOZ</sub> , leakage between BAT and VBUS, T <sub>J</sub> < 85°C		5	μA	
I <sub>BAT</sub>	Battery discharge current (BAT) in buck mode	V <sub>BAT</sub> = 4.5 V, HIZ Mode and No VBUS, I2C disabled, BATFET Disabled. T <sub>J</sub> < 85°C	17	33	μA	
I <sub>BAT</sub>	Battery discharge current (BAT, SW, SYS)	V <sub>BAT</sub> = 4.5 V, HIZ Mode and No VBUS, I2C Disabled, BATFET Enabled. T <sub>J</sub> < 85°C	58	85	μA	
I <sub>VBUS_HIZ</sub>	Input supply current (VBUS) in buck mode	V <sub>VBUS</sub> = 5 V, High-Z Mode, No battery	37	55	μA	
I <sub>VBUS_HIZ</sub>	Input supply current (VBUS) in buck mode	V <sub>VBUS</sub> = 12 V, High-Z Mode, No battery	68	93	μA	
I <sub>VBUS</sub>	Input supply current (VBUS) in buck mode	V <sub>VBUS</sub> = 12 V, V <sub>VBUS</sub> > V <sub>VBAT</sub> , converter not switching	1.5	3	mA	
I <sub>VBUS</sub>	Input supply current (VBUS) in buck mode	V <sub>VBUS</sub> > V <sub>UVLO</sub> , V <sub>VBUS</sub> > V <sub>VBAT</sub> , converter switching, V <sub>BAT</sub> = 3.8V, I <sub>SYS</sub> = 0A	3		mA	
I <sub>BOOST</sub>	Battery Discharge Current in boost mode	V <sub>BAT</sub> = 4.2 V, boost mode, I <sub>VBUS</sub> = 0 A, converter switching	3		mA	
<b>VBUS, VAC AND BAT PIN POWER-UP</b>						
V <sub>BUS_OP</sub>	VBUS operating range	V <sub>VBUS</sub> rising	3.9	13.5	V	
V <sub>VAC_UVLOZ</sub>	VBUS for active I <sup>2</sup> C, no battery Sense VAC pin voltage	V <sub>VAC</sub> rising	3.3	3.6	V	
V <sub>VAC_UVLOZ_HYS</sub>	I <sup>2</sup> C active hysteresis	V <sub>VAC</sub> falling from above V <sub>VAC_UVLOZ</sub>	300		mV	
V <sub>VAC_PRESENT</sub>	One of the conditions to turn on REGN	V <sub>VAC</sub> rising	3.65	3.9	V	
V <sub>VAC_PRESENT_HYS</sub>	One of the conditions to turn on REGN	V <sub>VAC</sub> falling	500		mV	
V <sub>SLEEP</sub>	Sleep mode falling threshold	(V <sub>VAC</sub> - V <sub>VBAT</sub> ), V <sub>BUSMIN_FALL</sub> ≤ V <sub>BAT</sub> ≤ V <sub>REG</sub> , V <sub>VAC</sub> falling	15	60	131	mV
V <sub>SLEEPZ</sub>	Sleep mode rising threshold	(V <sub>VAC</sub> - V <sub>VBAT</sub> ), V <sub>BUSMIN_FALL</sub> ≤ V <sub>BAT</sub> ≤ V <sub>REG</sub> , V <sub>VAC</sub> rising	115	220	340	mV

## 8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$  and  $V_{VAC} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}C$  to  $125^{\circ}C$  and  $T_J = 25^{\circ}C$  for typical values (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VAC\_OV\_RISE}$	VAC 6.5-V Overvoltage rising threshold	VAC rising; OVP (REG06[7:6]) = '01'	6.1	6.4	6.7	V
$V_{VAC\_OV\_RISE}$	VAC 10.5-V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) = '10'	10.35	10.9	11.5	V
$V_{VAC\_OV\_RISE}$	VAC 14-V Overvoltage rising threshold	VAC rising, OVP (REG06[7:6]) = '11'	13.5	14.2	14.85	V
$V_{VAC\_OV\_HYS}$	VAC 6.5-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '01'		320		mV
$V_{VAC\_OV\_HYS}$	VAC 10.5-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '10'		250		mV
$V_{VAC\_OV\_HYS}$	VAC 14-V Overvoltage hysteresis	VAC falling, OVP (REG06[7:6]) = '11'		300		mV
$V_{BAT\_UVLOZ}$	BAT for active I <sup>2</sup> C, no adapter	$V_{BAT}$ rising	2.5			V
$V_{BAT\_DPL\_FALL}$	Battery Depletion Threshold	$V_{BAT}$ falling	2.2		2.6	V
$V_{BAT\_DPL\_RISE}$	Battery Depletion Threshold	$V_{BAT}$ rising	2.34		2.86	V
$V_{BAT\_DPL\_HYST}$	Battery Depletion rising hysteresis	$V_{BAT}$ rising		180		mV
$V_{BUSMIN\_FALL}$	Bad adapter detection falling threshold	$V_{BUS}$ falling	3.75	3.9	4.0	V
$V_{BUSMIN\_HYST}$	Bad adapter detection hysteresis			80		mV
$I_{BADSRC}$	Bad adapter detection current source	Sink current from VBUS to GND		30		mA
<b>POWER-PATH</b>						
$V_{SYS\_MIN}$	System regulation voltage	$V_{VBAT} < SYS\_MIN[2:0] = 101$ , BATFET Disabled (REG07[5] = 1)	3.5	3.68		V
$V_{SYS}$	System Regulation Voltage	$I_{SYS} = 0$ A, $V_{VBAT} > V_{SYSMIN}$ , $V_{VBAT} = 4.400$ V, BATFET disabled (REG07[5] = 1)		$V_{BAT} + 50$ mV		V
$V_{SYS\_MAX}$	Maximum DC system voltage output	$I_{SYS} = 0$ A, Q4 off, $V_{VBAT} \leq 4.400$ V, $V_{VBAT} > V_{SYSMIN} = 3.5$ V	4.4	4.45	4.48	V
$R_{ON(RBFET)}$	Top reverse blocking MOSFET on-resistance between VBUS and PMID - Q1	$-40^{\circ}C \leq T_A \leq 125^{\circ}C$		45		m $\Omega$
$R_{ON(HSFET)}$	Top switching MOSFET on-resistance between PMID and SW - Q2	$V_{REGN} = 5$ V, $-40^{\circ}C \leq T_A \leq 125^{\circ}C$		62		m $\Omega$
$R_{ON(LSFET)}$	Bottom switching MOSFET on-resistance between SW and GND - Q3	$V_{REGN} = 5$ V, $-40^{\circ}C \leq T_A \leq 125^{\circ}C$		71		m $\Omega$
$V_{FWD}$	BATFET forward voltage in supplement mode			30		mV
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, $V_{BAT} = 4.2$ V, $T_J = 25^{\circ}C$		19.5	24	m $\Omega$
$R_{ON(BAT-SYS)}$	SYS-BAT MOSFET on-resistance	QFN package, Measured from BAT to SYS, $V_{BAT} = 4.2$ V, $T_J = -40 - 125^{\circ}C$		19.5	30	m $\Omega$
<b>BATTERY CHARGER</b>						
$V_{BATREG\_RANGE}$	Charge voltage program range		3.847		4.615	V
$V_{BATREG\_STEP}$	Charge voltage step			32		mV

## 8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$  and  $V_{VAC} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V <sub>BATREG</sub>	Charge voltage setting	VREG (REG04[7:3]) = 4.20 V (01011), V, $-40 \leq T_J \leq 85^{\circ}\text{C}$	4.178	4.200	4.220	
		VREG (REG04[7:3]) = 4.343 V (01111), V, $-40 \leq T_J \leq 85^{\circ}\text{C}$	4.321	4.343	4.365	V
		VREG (REG04[7:3]) = 4.391 V (10001), V, $-40 \leq T_J \leq 85^{\circ}\text{C}$	4.373	4.391	4.407	V
I <sub>CHG_REG_RANGE</sub>	Charge current regulation range	0		3000	mA	
I <sub>CHG_REG_STEP</sub>	Charge current regulation step		60		mA	
I <sub>CHG_REG</sub>	Charge current regulation setting	I <sub>CHG</sub> = 240 mA, V <sub>BAT</sub> = 3.1V or V <sub>BAT</sub> = 3.8 V	0.216	0.24	0.264	A
I <sub>CHG_REG_ACC</sub>	Charge current regulation accuracy	I <sub>CHG</sub> = 240 mA, V <sub>BAT</sub> = 3.1 V or V <sub>BAT</sub> = 3.8 V	-10%		10%	
I <sub>CHG_REG</sub>	Charge current regulation setting	I <sub>CHG</sub> = 720 mA, V <sub>BAT</sub> = 3.1 V or V <sub>BAT</sub> = 3.8 V	0.685	0.720	0.761	A
I <sub>CHG_REG</sub>	Charge current regulation accuracy	I <sub>CHG_REG</sub> = 720 mA, V <sub>BAT</sub> = 3.1 V or V <sub>BAT</sub> = 3.8 V	-5%		6%	
I <sub>CHG_REG</sub>	Charge current regulation setting	I <sub>CHG</sub> = 1.38 A, V <sub>BAT</sub> = 3.1 V or V <sub>BAT</sub> = 3.8 V	1.311	1.380	1.449	A
I <sub>CHG_REG_ACC</sub>	Charge current regulation accuracy	I <sub>CHG</sub> = 720 mA or I <sub>CHG</sub> = 1.38 A, V <sub>BAT</sub> = 3.1 V or V <sub>BAT</sub> = 3.8 V	-5%		5%	
V <sub>BATLOWV_FALL</sub>	Battery LOWV falling threshold	I <sub>CHG</sub> = 240 mA	2.7	2.8	2.9	V
V <sub>BATLOWV_RISE</sub>	Battery LOWV rising threshold	Pre-charge to fast charge	3.0	3.12	3.24	V
I <sub>PRECHG</sub>	Precharge current regulation	IPRECHG[3:0] = '0010' = 180 mA	153	171	189	mA
I <sub>PRECHG_ACC</sub>	Precharge current regulation accuracy	IPRECHG[3:0] = '0010' = 180 mA	-15%		5%	
I <sub>TERM</sub>	Termination current regulation	I <sub>CHG</sub> > 780 mA, I <sub>TERM</sub> [3:0] = '0010' = 180 mA, V <sub>BAT</sub> = 4.208 V	150	180	216	mA
I <sub>TERM_ACC</sub>	Termination current regulation accuracy	I <sub>CHG</sub> > 780 mA, I <sub>TERM</sub> [3:0] = '0010' = 180 mA, V <sub>BAT</sub> = 4.208 V	-16.7%		20%	
I <sub>TERM</sub>	Termination current regulation	I <sub>CHG</sub> ≤ 780 mA, I <sub>TERM</sub> [3:0] = '0010' = 180 mA	162	180	192	mA
I <sub>TERM_ACC</sub>	Termination current regulation accuracy	I <sub>CHG</sub> ≤ 780 mA, I <sub>TERM</sub> [3:0] = '0010' = 180 mA	-10%		10%	
I <sub>TERM</sub>	Termination current regulation	I <sub>CHG</sub> = 600 mA, I <sub>TERM</sub> [3:0] = '0000' = 60 mA, V <sub>BAT</sub> = 4.208 V	45	60	85	mA
I <sub>TERM_ACC</sub>	Termination current regulation accuracy	I <sub>CHG</sub> = 600 mA, I <sub>TERM</sub> [3:0] = '0000' = 60 mA, V <sub>BAT</sub> = 4.208 V	-25%		42%	
V <sub>SHORT</sub>	Battery short voltage	V <sub>BAT</sub> falling	1.85	2	2.15	V
V <sub>SHORTZ</sub>	Battery short voltage	V <sub>BAT</sub> rising	2.15	2.25	2.35	V
I <sub>SHORT</sub>	Battery short current	V <sub>BAT</sub> < V <sub>SHORTZ</sub>	70	90	110	mA
V <sub>RECHG</sub>	Recharge Threshold below V <sub>BAT_REG</sub>	V <sub>BAT</sub> falling, REG04[0] = 0	90	120	150	mV
V <sub>RECHG</sub>	Recharge Threshold below V <sub>BAT_REG</sub>	V <sub>BAT</sub> falling, REG04[0] = 1	200	230	265	mV
I <sub>SYSLD</sub>	System discharge load current	V <sub>SYS</sub> = 4.2 V		30		mA
<b>INPUT VOLTAGE AND CURRENT REGULATION</b>						
V <sub>INDPM</sub>	Input voltage regulation limit	V <sub>INDPM</sub> (REG06[3:0] = 0000) = 3.9 V	3.78	3.95	4.1	V
V <sub>INDPM_ACC</sub>	Input voltage regulation accuracy		-3%		5%	
V <sub>INDPM</sub>	Input voltage regulation limit	V <sub>INDPM</sub> (REG06[3:0] = 0110) = 4.4 V	4.268	4.4	4.532	V

## 8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$  and  $V_{VAC} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{INDPM\_ACC}$	Input voltage regulation accuracy	-3%		3%		
$V_{DPM\_VBAT}$	Input voltage regulation limit tracking VBAT	$V_{INDPM} = 3.9\text{V}$ , $V_{DPM\_VBAT\_TRACK} = 300\text{mV}$ , $V_{BAT} = 4.0\text{V}$	4.171	4.3	4.43	V
$V_{DPM\_VBAT\_ACC}$	Input voltage regulation accuracy tracking VBAT	-3%		3%		
$I_{INDPM}$	USB input current regulation limit	$V_{VBUS} = 5\text{V}$ , current pulled from SW, $I_{INDPM} (\text{REG}[4:0] = 00100) = 500\text{mA}$ , $-40 \leq T_J \leq 85^{\circ}\text{C}$	450		500	mA
		$V_{VBUS} = 5\text{V}$ , current pulled from SW, $I_{INDPM} (\text{REG}[4:0] = 01000) = 900\text{mA}$ , $-40 \leq T_J \leq 85^{\circ}\text{C}$	750		900	mA
		$V_{VBUS} = 5\text{V}$ , current pulled from SW, $I_{INDPM} (\text{REG}[4:0] = 01110) = 1.5\text{A}$ , $-40 \leq T_J \leq 85^{\circ}\text{C}$	1.3		1.5	A
$I_{IN\_START}$	Input current limit during system start-up sequence		200		mA	
<b>BAT PIN OVERVOLTAGE PROTECTION</b>						
$V_{BATOVP\_RISE}$	Battery overvoltage threshold	$V_{BAT}$ rising, as percentage of $V_{BAT\_REG}$	103%	104%	105%	
$V_{BATOVP\_FALL}$	Battery overvoltage threshold	$V_{BAT}$ falling, as percentage of $V_{BAT\_REG}$	101%	102%	103%	
<b>THERMAL REGULATION AND THERMAL SHUTDOWN</b>						
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, $T_{REG} (\text{REG}05[1] = 1) = 110^{\circ}\text{C}$		110		$^{\circ}\text{C}$
$T_{JUNCTION\_REG}$	Junction Temperature Regulation Threshold	Temperature Increasing, $T_{REG} (\text{REG}05[1] = 0) = 90^{\circ}\text{C}$		90		$^{\circ}\text{C}$
$T_{SHUT}$	Thermal Shutdown Rising Temperature	Temperature Increasing		160		$^{\circ}\text{C}$
$T_{SHUT\_HYST}$	Thermal Shutdown Hysteresis			30		$^{\circ}\text{C}$
<b>JEITA Thermistor Comparator (BUCK MODE)</b>						
$V_{T1}$	T1 ( $0^{\circ}\text{C}$ ) threshold, Charge suspended T1 below this temperature.	Charger suspends charge. As Percentage to $V_{REGN}$	72.4%	73.3%	74.2%	
$V_{T1}$	Falling	As Percentage to $V_{REGN}$	69%	71.5%	74%	
$V_{T2}$	T2 ( $10^{\circ}\text{C}$ ) threshold, Charge back to $I_{CHG}/2$ and 4.2 V below this temperature	As percentage of $V_{REGN}$	67.2%	68%	69%	
$V_{T2}$	Falling	As Percentage to $V_{REGN}$	66%	66.8%	67.7%	
$V_{T3}$	T3 ( $45^{\circ}\text{C}$ ) threshold, charge back to $I_{CHG}$ and 4.05V above this temperature.	Charger suspends charge. As Percentage to $V_{REGN}$	43.8%	44.7%	45.8%	
$V_{T3}$	Falling	As Percentage to $V_{REGN}$	45.1%	45.7%	46.3%	
$V_{T5}$	T5 ( $60^{\circ}\text{C}$ ) threshold, charge suspended above this temperature.	As Percentage to $V_{REGN}$	33.7%	34.2%	35.1%	
$V_{T5}$	Falling	As Percentage to $V_{REGN}$	34.5%	35.3%	36.3%	
<b>COLD OR HOT THERMISTOR COMPARATOR (BOOST MODE)</b>						
$V_{BCOLD}$	Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to $V_{REGN}$ (Approx. $-20^{\circ}\text{C}$ w/ 103AT), $T_J = -20^{\circ}\text{C} - 125^{\circ}\text{C}$	79.5%	80%	80.5%	
$V_{BCOLD}$	Falling	$T_J = -20^{\circ}\text{C} - 125^{\circ}\text{C}$	78.3%	79%	79.7%	

## 8.5 Electrical Characteristics (continued)

$V_{VAC\_UVLOZ} < V_{VAC} < V_{VAC\_OV}$  and  $V_{VAC} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

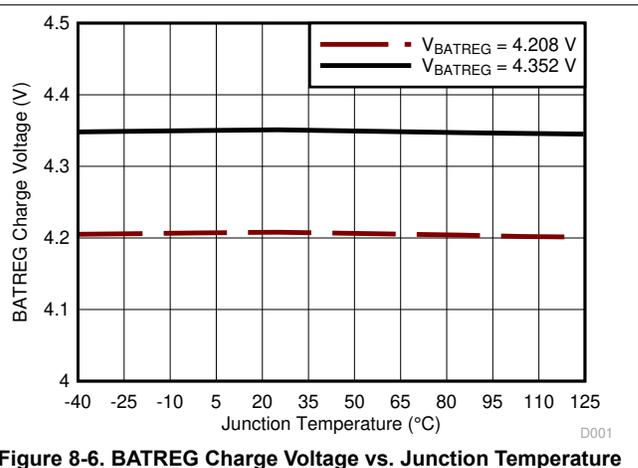
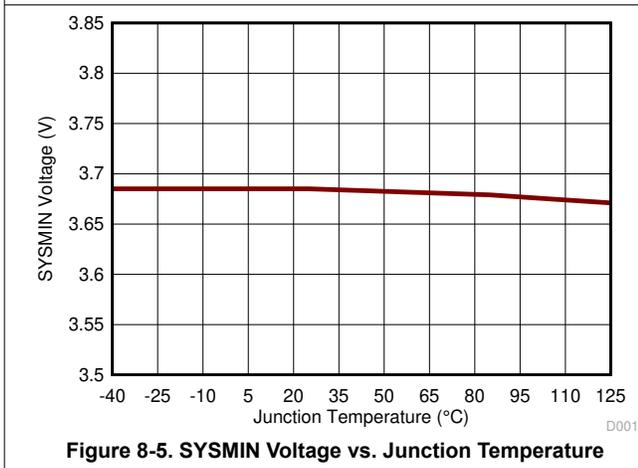
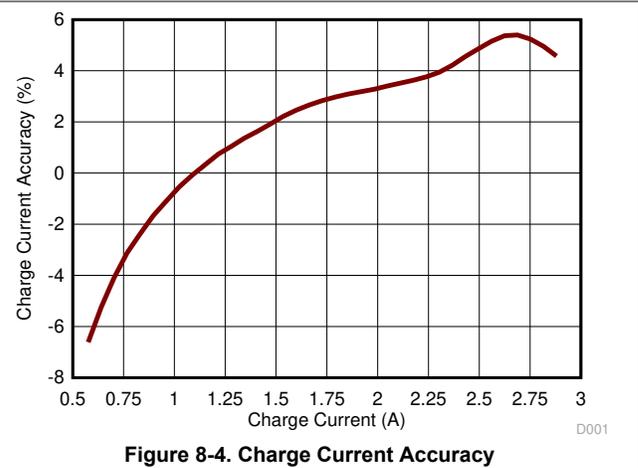
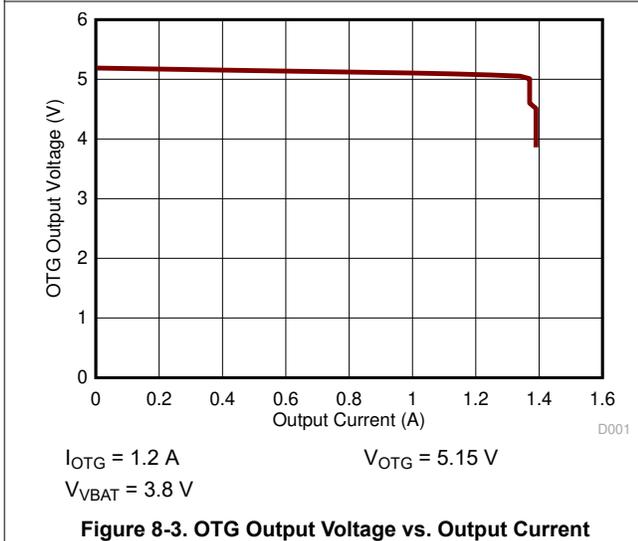
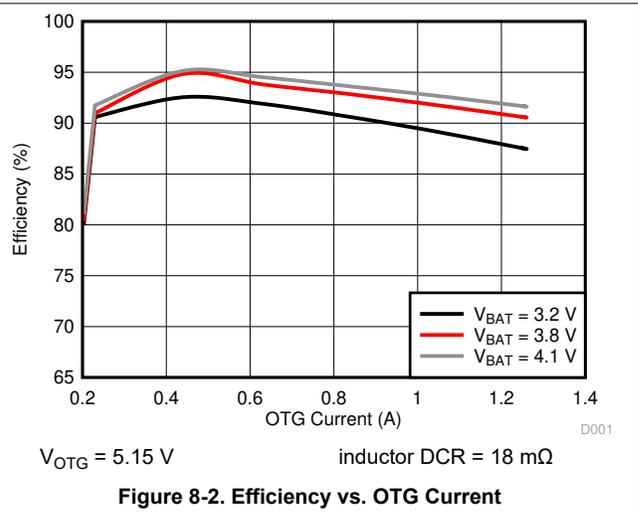
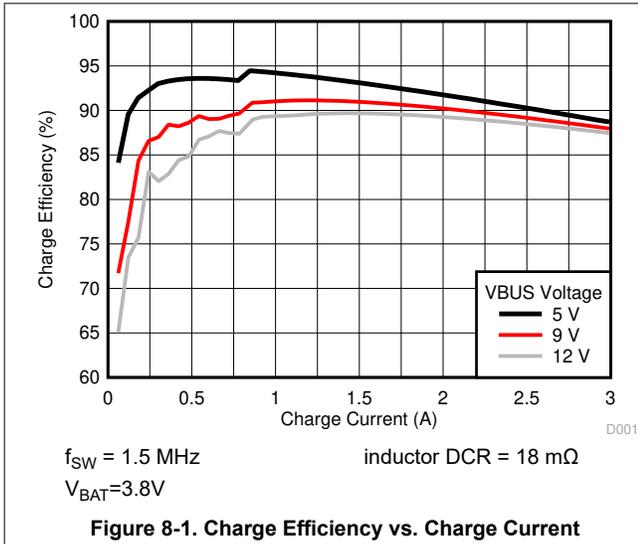
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
$V_{BHOT}$	Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to $V_{REGN}$ (Approx. $60^{\circ}\text{C}$ w/ 103AT), $T_J = -20^{\circ}\text{C} - 125^{\circ}\text{C}$		30.2%	31.2%	32.2%	
$V_{BHOT}$	Rising	$T_J = -20^{\circ}\text{C} - 125^{\circ}\text{C}$		33.8%	34.4%	34.9%	
<b>CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)</b>							
$I_{HSFET\_OCP}$	HSFET cycle-by-cycle over-current threshold			5.2		8.0	A
$I_{BATFET\_OCP}$	System over load threshold			6.0			A
<b>PWM</b>							
$f_{SW}$	PWM switching frequency	Oscillator frequency, buck mode		1320	1500	1680	kHz
		Oscillator frequency, boost mode		1150	1412	1660	kHz
$D_{MAX}$	Maximum PWM duty cycle <sup>(1)</sup>			97%			
<b>BOOST MODE OPERATION</b>							
$V_{OTG\_REG}$	Boost mode regulation voltage	$V_{VBAT} = 3.8\text{ V}$ , $I_{(PMID)} = 0\text{ A}$ , $BOOSTV[1:0] = '10' = 5.15\text{ V}$		4.97	5.126	5.280	V
$V_{OTG\_REG\_ACC}$	Boost mode regulation voltage accuracy	$V_{VBAT} = 3.8\text{ V}$ , $I_{(PMID)} = 0\text{ A}$ , $BOOSTV[1:0] = '10' = 5.15\text{ V}$		-3%		3%	
$V_{BATLOWV\_OTG}$	Battery voltage exiting boost mode	$V_{VBAT}$ falling, $MIN\_VBAT\_SEL$ (REG01[0]) = 0		2.6	2.8	2.93	V
		$V_{VBAT}$ rising, $MIN\_VBAT\_SEL$ (REG01[0]) = 0		2.9	3.0	3.15	V
		$V_{VBAT}$ falling, $MIN\_VBAT\_SEL$ (REG01[0]) = 1		2.38	2.5	2.6	V
		$V_{VBAT}$ rising, $MIN\_VBAT\_SEL$ (REG01[0]) = 1		2.7	2.8	2.93	V
$I_{OTG}$	OTG mode output current	$BOOST\_LIM$ (REG02[7]) = 1		1.2	1.4	1.6	A
$I_{OTG\_OCP\_ACC}$	Boost mode RBFET over-current protection accuracy	$BOOST\_LIM = 0.5\text{ A}$ (REG02[7] = 0)		0.5		0.722	A
$V_{OTG\_OVP}$	OTG overvoltage threshold	Rising threshold		5.55	5.8	6.15	V
<b>REGN LDO</b>							
$V_{REGN}$	REGN LDO output voltage	$V_{VBUS} = 9\text{ V}$ , $I_{REGN} = 40\text{ mA}$		5.6	6		V
$V_{REGN}$	REGN LDO output voltage	$V_{VBUS} = 5\text{ V}$ , $I_{REGN} = 20\text{ mA}$		4.6	4.7		V
<b>LOGIC I/O PIN CHARACTERISTICS ( <math>\overline{CE}</math>, INT, STAT)</b>							
$V_{ILO}$	Input low threshold					0.4	V
$V_{IH}$	Input high threshold			1.3			V
$I_{BIAS}$	High-level leakage current	Pull up rail 1.8 V				1	$\mu\text{A}$
<b>I2C Interface (SCL, SDA)</b>							
$V_{IH}$	Input high threshold level	Pull up rail 1.8 V		1.3			V
$V_{IL}$	Input low threshold level	Pull up rail 1.8 V				0.4	V
$V_{OL}$	Output low threshold level	Sink current = 5 mA,				0.4	V

(1) Specified by design. Not production tested.

## 8.6 Timing Requirements

			MIN	NOM	MAX	UNIT
<b>VBUS/BAT POWER UP</b>						
t <sub>ACOV</sub>	VAC OVP reaction time	VAC rising above ACOV threshold to turn off Q2		200		ns
t <sub>BADSRC</sub>	Bad adapter detection duration			30		ms
<b>BATTERY CHARGER</b>						
t <sub>TERM_DGL</sub>	Deglintch time for charge termination			250		ms
t <sub>RECHG_DGL</sub>	Deglintch time for recharge			250		ms
t <sub>SYSOVLD_DGL</sub>	System over-current deglitch time to turn off Q4			100		µs
t <sub>BATOV</sub>	Battery over-voltage deglitch time to disable charge			1		µs
t <sub>SAFETY</sub>	Typical Charge Safety Timer Range	CHG_TIMER = 1	8	10	12	hr
t <sub>TOP_OFF</sub>	Typical Top-Off Timer Range	TOP_OFF_TIMER[1:0] = 10 (30 min)	24	30	36	min
<b>QON TIMING</b>						
t <sub>SHIPMODE</sub>	/QON low time to turn on BATFET and exit ship mode	-10°C ≤ T <sub>J</sub> ≤ 60°C	0.9		1.3	s
t <sub>QON_RST_2</sub>	QON low time to reset BATFET	-10°C ≤ T <sub>J</sub> ≤ 60°C	8		12	s
t <sub>BATFET_RST</sub>	BATFET off time during full system reset	-10°C ≤ T <sub>J</sub> ≤ 60°C	250		400	ms
t <sub>SM_DLY</sub>	Enter ship mode delay	-10°C ≤ T <sub>J</sub> ≤ 60°C	10		15	s
<b>DIGITAL CLOCK AND WATCHDOG TIMER</b>						
t <sub>WDT</sub>	REG05[4]=1	REGN LDO disabled		40		s
f <sub>LPDIG</sub>	Digital Low Power Clock	REGN LDO disabled		30		kHz
f <sub>DIG</sub>	Digital Clock	REGN LDO enabled		500		kHz
f <sub>SCL</sub>	SCL clock frequency				400	kHz

## 8.7 Typical Characteristics



### 8.7 Typical Characteristics (continued)

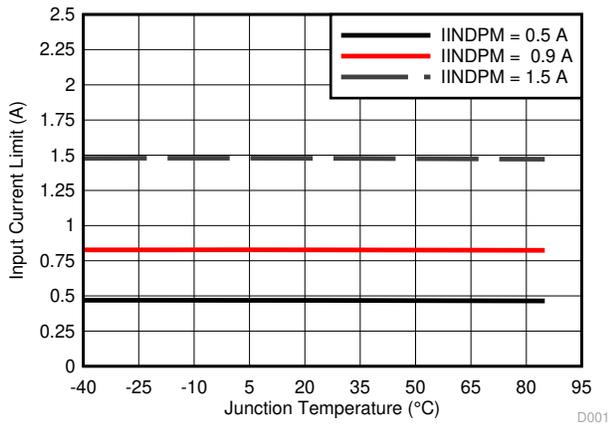


Figure 8-7. Input Current Limit vs. Junction Temperature

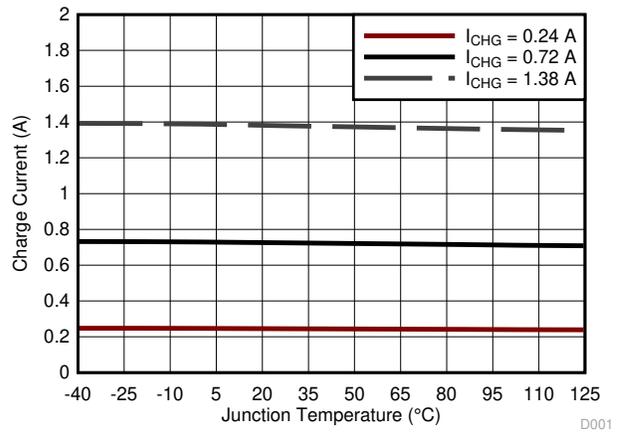


Figure 8-8. Charge Current vs. Junction Temperature

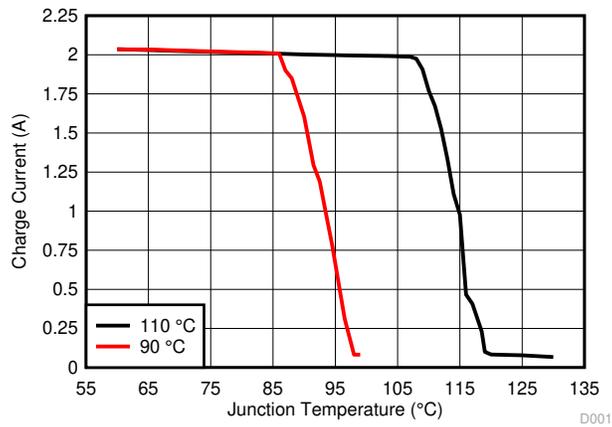


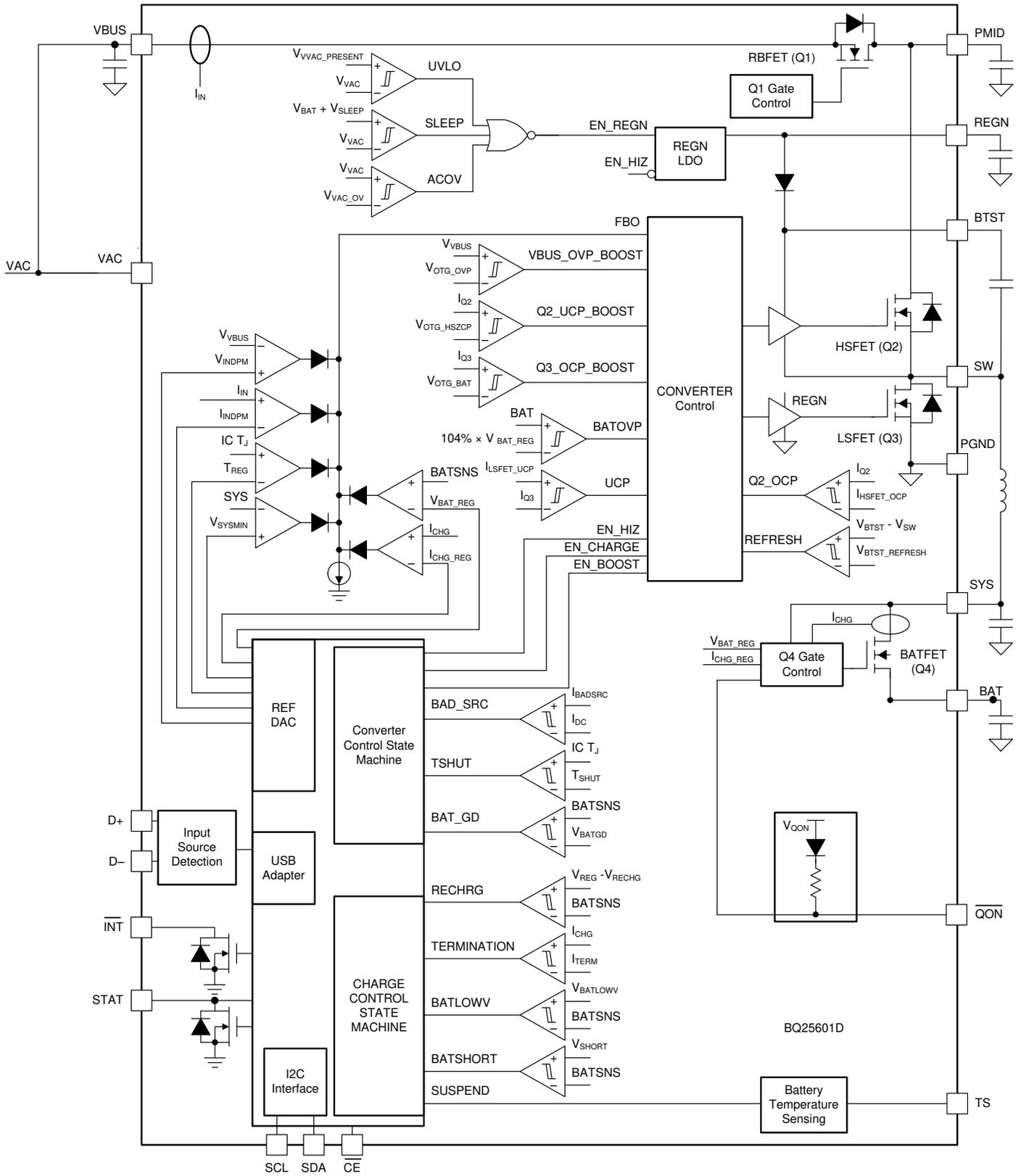
Figure 8-9. Charge Current vs. Junction Temperature

## 9 Detailed Description

### 9.1 Overview

The BQ25601D device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When VBUS rises above  $V_{VBUS\_UVLOZ}$  or BAT rises above  $V_{BAT\_UVLOZ}$ , the sleep comparator, battery depletion comparator and BATFET driver are active. I<sup>2</sup>C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

### 9.3.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold ( $V_{BAT\_DPL\_RISE}$ ), the BATFET turns on and connects battery to system. The REGN stays off to minimize the quiescent current. The low RDSON of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (*Supplement Mode*). When the system is overloaded or shorted ( $I_{BAT} > I_{BATFET\_OCP}$ ), the device turns off BATFET immediately and set BATFET\_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in *BATFET Enable (Exit Shipping Mode)* is applied to re-enable BATFET.

### 9.3.3 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO
2. Poor Source Qualification
3. Input Source Type Detection is based on D+/D– to set default input current limit (IINDPM) register or input source type.
4. Input Voltage Limit Threshold Setting (VINDPM threshold)
5. Converter Power-up

#### 9.3.3.1 Power Up REGN Regulation

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN is enabled when all the below conditions are valid:

- $V_{VAC}$  above  $V_{VAC\_PRESENT}$
- $V_{VAC}$  above  $V_{BAT} + V_{SLEEPZ}$  in buck mode or  $V_{BUS}$  below  $V_{BAT} + V_{SLEEP}$  in boost mode
- After 220-ms delay is completed

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than  $I_{VBUS\_HIZ}$  from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

#### 9.3.3.2 Poor Source Qualification

After REGN LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements in order to start the buck converter.

- VBUS voltage below  $V_{VAC\_OV}$
- VBUS voltage above  $V_{VBUSMIN}$  when pulling  $I_{BADSRC}$  (typical 30 mA)

Once the input source passes all the conditions above, the status register bit  $V_{BUS\_GD}$  is set high and the  $\overline{INT}$  pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

#### 9.3.3.3 Input Source Type Detection

After the  $V_{BUS\_GD}$  bit is set and REGN LDO is powered, the device runs input source detection through D+/D– lines. The BQ25601D follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/DCP) and non-standard adapter through USB D+/D– lines.

After input source type detection is completed, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit
2. PG\_STAT bit is set
3. VBUS\_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

#### 9.3.3.3.1 D+/D– Detection Sets Input Current Limit in BQ25601D

The BQ25601D contains a D+/D– based input source detection to set the input current limit at VBUS plug-in. The D+/D– detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detections. The USB BC1.2 is capable to identify Standard Downstream Port (SDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the non-standard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D– pins. If an adapter is detected as DCP, the input current limit is set at 2.4 A. If an adapter is detected as unknown, the input current limit is set at 0.5 A.

**Table 9-1. Non-Standard Adapter Detection**

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	$V_{D+}$ within $V_{2P7\_VTH}$	$V_{D-}$ within $V_{2P0\_VTH}$	2.1
Divider 2	$V_{D+}$ within $V_{1P2\_VTH}$	$V_{D-}$ within $V_{1P2\_VTH}$	2
Divider 3	$V_{D+}$ within $V_{2P0\_VTH}$	$V_{D-}$ within $V_{2P7\_VTH}$	1
Divider 4	$V_{D+}$ within $V_{2P7\_VTH}$	$V_{D-}$ within $V_{2P7\_VTH}$	2.4

**Table 9-2. Input Current Limit Setting from D+/D– Detection**

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)
USB SDP (USB500)	500 mA
USB DCP	2.4 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Divider 2	2 A
Unknown 5-V Adapter	

#### 9.3.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device supports wide range of input voltage limit (3.9 V – 5.4V) for USB. The device's VINDPM is set at 4.5V. The device supports dynamic VINDPM tracking settings which tracks the battery voltage. This function can be enabled via the VDPM\_BAT\_TRACK[1:0] register bits. When enabled, the actual input voltage limit will be the higher of the VINDPM register and VBAT + VDPM\_BAT\_TRACK offset.

#### 9.3.3.5 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is to the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value set by IINDPM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

The device switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled. The PFM\_DIS bit can be used to prevent PFM operation in either buck or boost configuration. The PFM mod is only enabled when IINDPM is set  $\geq 500$  mA. When IINDPM is set  $\leq 400$  mA, the PFM mode is disabled.

### 9.3.4 Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA output requirement. The maximum output current is up to 1.2 A. The boost operation can be enabled if the conditions are valid:

1. BAT above  $V_{OTG\_BAT}$
2. VBUS less than  $BAT + V_{SLEEP}$  (in sleep mode)
3. Boost mode operation is enabled (OTG\_CONFIG bit = 1)
4. Voltage at TS (thermistor) pin is within acceptable range ( $V_{BHOT} < V_{TS} < V_{BCOLD}$ )
5. After 30-ms delay from boost mode enable

During boost mode, the status register VBUS\_STAT bits is set to 111, the VBUS output is 5.15 V and the output current can reach up to 1.2 A, selected through I<sup>2</sup>C (BOOST\_LIM bit). The boost output is maintained when BAT is above  $V_{OTG\_BAT}$  threshold.

When OTG is enabled, the device starts up with PFM and later transits to PWM to minimize the overshoot. The PFM\_DIS bit can be used to prevent PFM operation in either buck or boost configuration.

### 9.3.5 Host Mode and Standalone Power Management

#### 9.3.5.1 Host Mode and Default Mode in BQ25601D

The BQ25601D is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG\_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG\_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

In default mode, the device keeps charging the battery with default 10-hour fast charging safety timer. At the end of the 10-hour, the charging is stopped and the buck converter continues to operate to supply system load.

Writing a 1 to the WD\_RST bit transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD\_RST bit before the watchdog timer expires (WATCHDOG\_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WATCHDOG\_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, VINDPM, BATFET\_RST\_EN, BATFET\_DLY, and BATFET\_DIS bits.

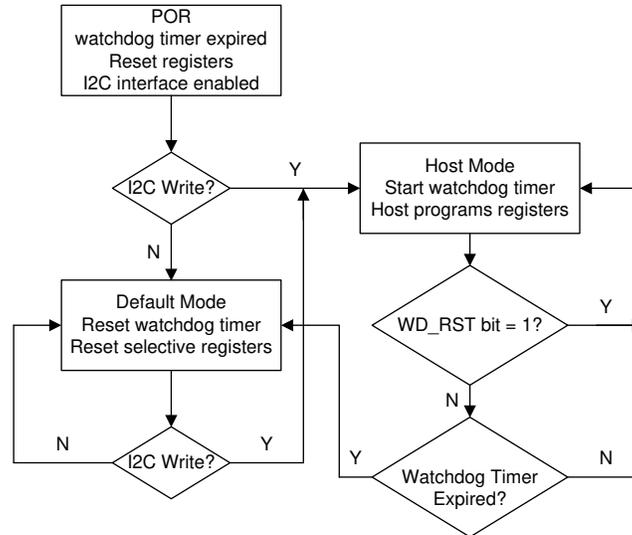


Figure 9-1. Watchdog Timer Flow Chart

### 9.3.6 Power Path Management

The device accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

### 9.3.7 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimize the voltage drop during discharging.

#### 9.3.7.1 Autonomous Charging Cycle

With battery charging is enabled (CHG\_CONFIG bit = 1 and  $\overline{CE}$  pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 9-3. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I<sup>2</sup>C.

Table 9-3. Charging Parameter Default Setting

DEFAULT MODE	BQ25601D
Charging voltage	4.208V
Charging current	2.048 A
Pre-charge current	180 mA
Termination current	180 mA
Temperature profile	JEITA
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG\_CONFIG bit = 1 and I<sub>CHG</sub> register is not 0 mA and  $\overline{CE}$  is low)
- No thermistor fault on TS
- No safety timer fault
- BATFET is not forced to turn off (BATFET\_DIS bit = 0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the

device automatically starts a new charging cycle. After the charge is done, toggle  $\overline{CE}$  pin or CHG\_CONFIG bit can initiate a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting EN\_ICHG\_MON bits = 11. In addition, the status register (CHRG\_STAT) indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT is asserted to notify the host.

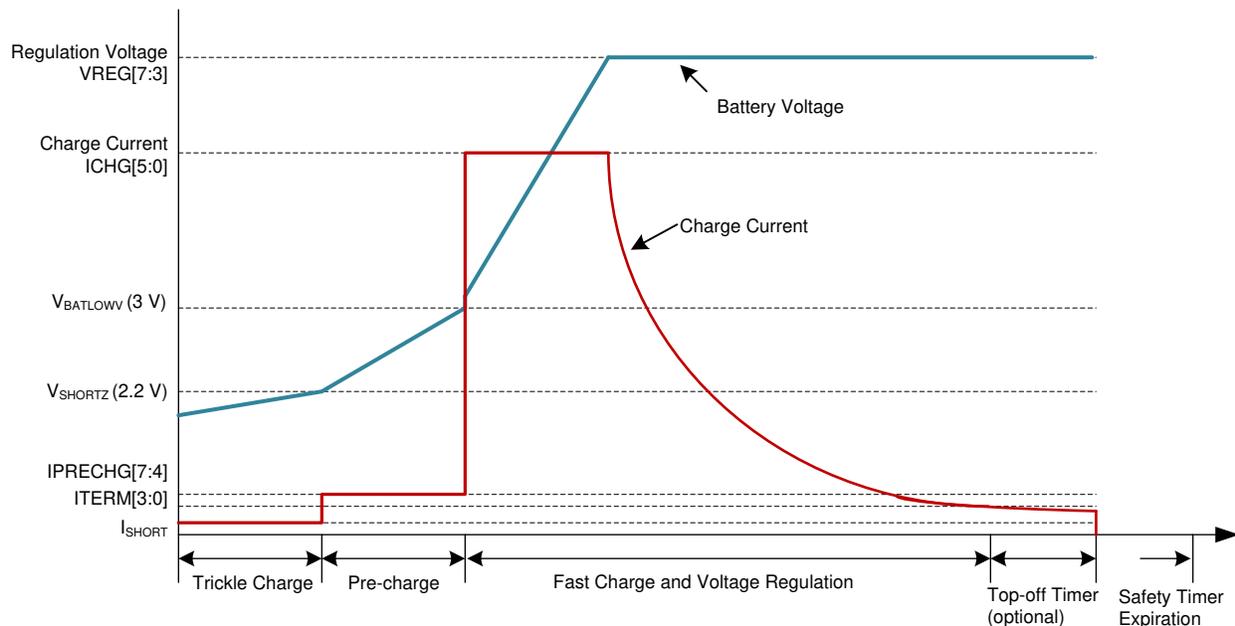
### 9.3.7.2 Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

**Table 9-4. Charging Current Setting**

$V_{BAT}$	CHARGING CURRENT	REGISTER DEFAULT SETTING	CHRG_STAT
< 2.2 V	$I_{SHORT}$	100 mA	01
2.2 V to 3 V	$I_{PRECHG}$	180 mA	01
> 3 V	$I_{CHG}$	2.048 A	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.



**Figure 9-2. Battery Charging Profile**

### 9.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage *Supplement Mode*.

When termination occurs, the status register CHRG\_STAT is set to 11, and an INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN\_TERM bit prior to charge termination.

At low termination currents (25 mA-50 mA), due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer. TOPOFF\_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG\_STAT and TOPOFF\_ACTIVE to find out the termination status.

Top off timer gets reset at one of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG\_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value after termination will have no effect unless a recharge cycle is initiated. An INT is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

### 9.3.7.4 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

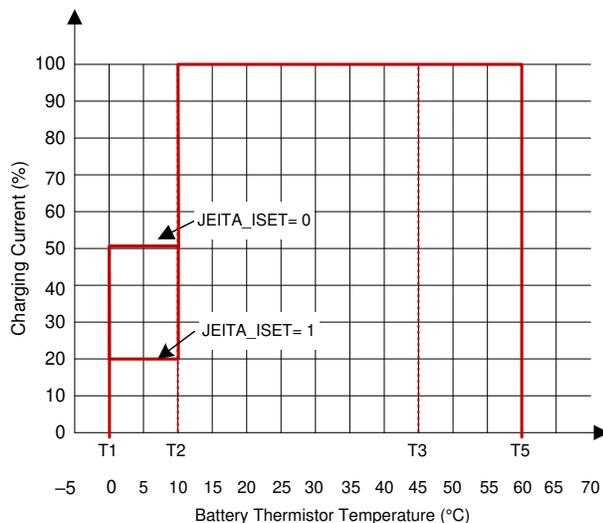
### 9.3.7.5 JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

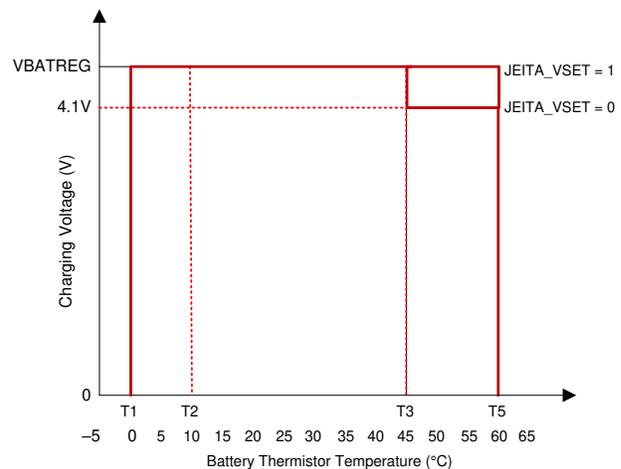
To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V charge termination is disabled for cool and warm conditions.

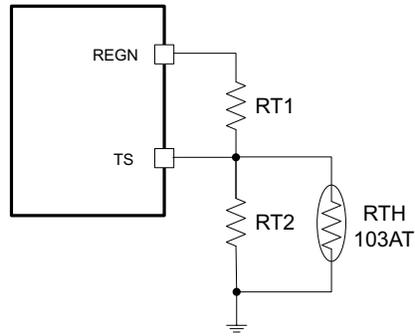
The charger provides flexible voltage/current settings beyond the JEITA requirement. The voltage setting at warm temperature (T3-T5) can be VREG or 4.1V (configured by JEITA\_VSET). The current setting at cool temperature (T1-T2) can be further reduced to 20% of fast charge current (JEITA\_ISET).



**Figure 9-3. JEITA Profile: Charging Current**



**Figure 9-4. JEITA Profile: Charging Voltage**



**Figure 9-5. TS Resistor Network**

Equation 1 through Equation 2 describe updates to the resistor bias network.

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left( \frac{1}{VT1} - \frac{1}{VT5} \right)}{RTH_{HOT} \times \left( \frac{V_{REGN}}{VT5} - 1 \right) - RTH_{COLD} \times \left( \frac{V_{REGN}}{VT1} - 1 \right)} \quad (1)$$

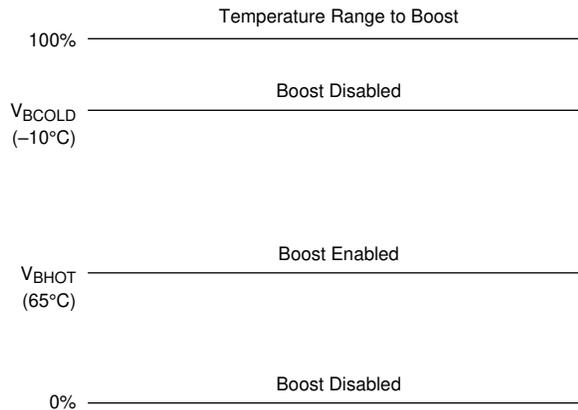
$$RT1 = \frac{\left( \left( \frac{V_{REGN}}{VT1} \right) - 1 \right)}{\left( \frac{1}{RT2} \right) + \left( \frac{1}{RTH_{COLD}} \right)} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

- $RTH_{COLD} = 27.28 \text{ K}\Omega$
- $RTH_{HOT} = 3.02 \text{ K}\Omega$
- $RT1 = 5.23 \text{ K}\Omega$
- $RT2 = 30.9 \text{ K}\Omega$

### 9.3.7.6 Boost Mode Thermistor Monitor During Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the VBCOLD to VBHOT thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. In addition, VBUS\_STAT bits are set to 000 and NTC\_FAULT is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC\_FAULT is cleared.



**Figure 9-6. TS Pin Thermistor Sense Threshold in Boost Mode**

### 9.3.7.7 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below  $V_{BATLOWV}$  threshold and 10 hours when the battery is higher than  $V_{BATLOWV}$  threshold.

The user can program fast charge safety timer through I<sup>2</sup>C (CHG\_TIMER bits). When safety timer expires, the fault register CHRG\_FAULT bits are set to 11 and an INT is asserted to the host. The safety timer feature can be disabled through I<sup>2</sup>C by setting EN\_TIMER bit

During input voltage, current, JEITA cool or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IDPM\_STAT = 1) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This half clock rate feature can be disabled by writing 0 to TMR2X\_EN bit.

During the fault, timer is suspended. Once the fault goes away, timer resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHRG\_CONFIG bit).

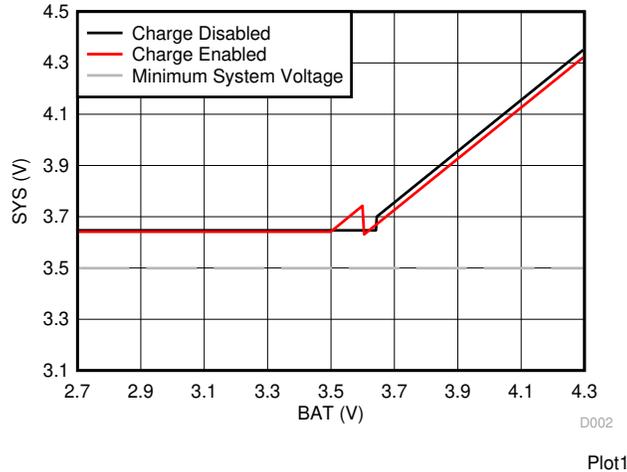
## 9.4 Device Functional Modes

### 9.4.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS\_Min bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the VDS of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS\_STAT bit goes high when the system is in minimum system voltage regulation.



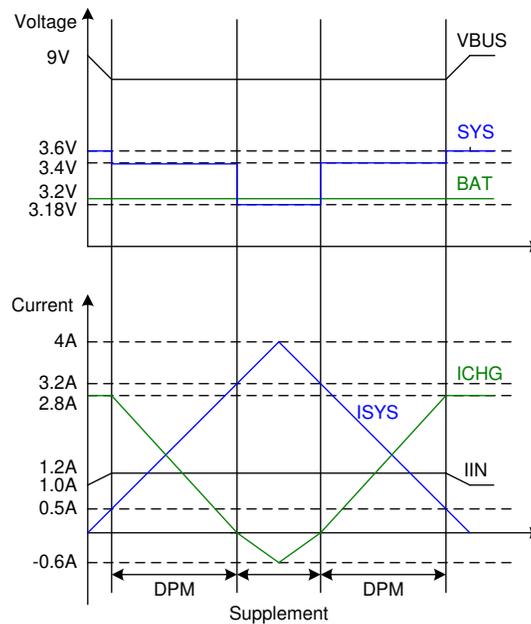
**Figure 9-7. System Voltage vs Battery Voltage**

### 9.4.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VDPM\_STAT (VINDPM) or IDPM\_STAT (IIDPM) goes high. [Figure 9-8](#) shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.5-V minimum system voltage setting.

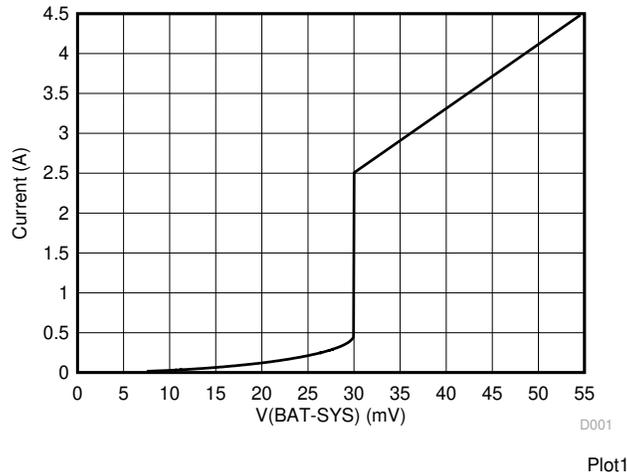


**Figure 9-8. DPM Response**

### 9.4.3 Supplement Mode

When the system voltage falls 180 mV ( $V_{BAT} > V_{SYSMin}$ ) or 45 mV ( $V_{BAT} < V_{SYSMin}$ ) below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET VDS stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce  $R_{DS(on)}$  until the BATFET is in full conduction. At this point onwards, the BATFET VDS linearly increases with discharge current. [Figure 9-9](#) shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.



**Figure 9-9. BATFET V-I Curve**

### 9.4.4 Shipping Mode and $\overline{QON}$ Pin

#### 9.4.4.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET\_DIS bit, the charger can turn off BATFET immediately or delay by  $t_{SM\_DLY}$  as configured by BATFET\_DLY bit.

#### 9.4.4.2 BATFET Enable (Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET\_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET\_DIS bit
3. Set REG\_RST bit to reset all registers including BATFET\_DIS bit to default (0)
4. A logic high to low transition on  $\overline{QON}$  pin with  $t_{SHIPMODE}$  deglitch time to enable BATFET to exit shipping mode

#### 9.4.4.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged-in. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The  $\overline{QON}$  pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the  $\overline{QON}$  pin is driven to logic low for  $t_{QON\_RST}$  while input source is not plugged in and BATFET is enabled (BATFET\_DIS = 0), the BATFET is turned off for  $t_{BATFET\_RST}$  and then it is re-enabled to reset system power. This function can be disabled by setting BATFET\_RST\_EN bit to 0.

#### 9.4.4.4 $\overline{QON}$ Pin Operations

The  $\overline{QON}$  pin incorporates two functions to control BATFET.

1. **BATFET Enable:** A  $\overline{QON}$  logic transition from high to low with longer than  $t_{SHIPMODE}$  deglitch turns on BATFET and exit shipping mode. When exiting shipping mode, HIZ is enabled ( $EN\_HIZ = 1$ ) as well. HIZ can be disabled ( $EN\_HIZ = 0$ ) by the host after exiting shipping mode. OTG cannot be enabled ( $OTG\_CONFIG = 1$ ) until HIZ is disabled.
2. **BATFET Reset:** When  $\overline{QON}$  is driven to logic low by at least  $t_{QON\_RST}$  while adapter is not plugged in (and  $BATFET\_DIS = 0$ ), the BATFET is turned off for  $t_{BATFET\_RST}$ . The BATFET is re-enabled after  $t_{BATFET\_RST}$  duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting  $BATFET\_RST\_EN$  bit to 0.

Figure 9-10 shows the sample external configurations for each.

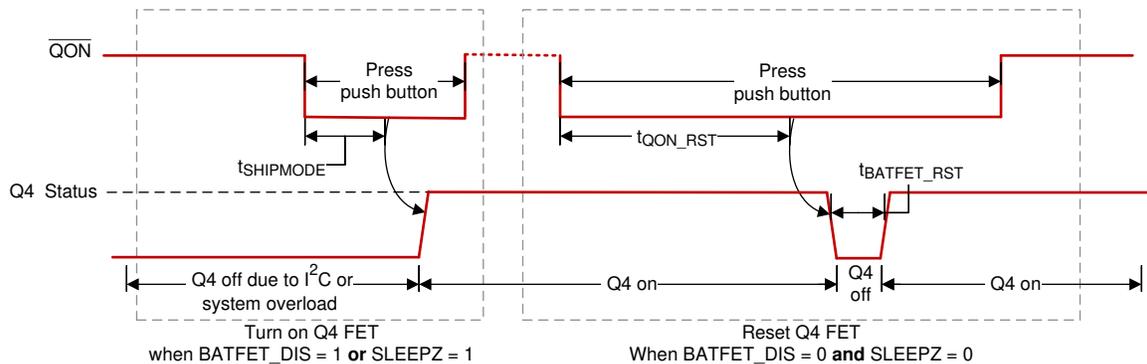


Figure 9-10.  $\overline{QON}$  Timing

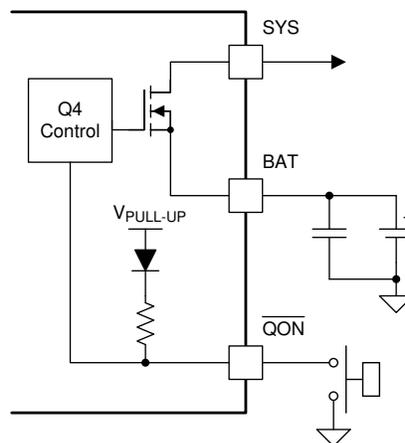


Figure 9-11.  $\overline{QON}$  Circuit

#### 9.4.5 Status Outputs ( $\overline{PG}$ , $\overline{STAT}$ , $\overline{INT}$ )

##### 9.4.5.1 Power Good Indicator ( $\overline{PG}$ Pin $PG\_STAT$ Bit)

The  $PG\_STAT$  bit goes HIGH to indicate a good input source when:

- $VBUS$  above  $V_{VBUS\_UVLO}$
- $VBUS$  above battery (not in sleep)
- $VBUS$  below  $V_{VAC\_OV}$  threshold
- $VBUS$  above  $V_{VBUSMin}$  (typical 3.8 V) when  $I_{BADSRC}$  (typical 30 mA) current is applied (not a poor source)
- Completed *input Source Type Detection*

### 9.4.5.2 Charging Status indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED. The STAT pin function can be disabled by setting the EN\_ICHG\_MON bits = 11.

**Table 9-5. STAT Pin State**

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (input overvoltage, TS fault, timer fault or system overvoltage) Boost Mode suspend (due to TS fault)	Blinking at 1 Hz

### 9.4.5.3 Interrupt to Host ( $\overline{INT}$ )

In some applications, the host does not always monitor the charger operation. The INT pulse notifies the system on the device operation. The following events will generate 256- $\mu$ s INT pulse.

- USB/adaptor source identified (through DPDM detection)
- Good input source detected
  - VBUS above battery (not in sleep)
  - VBUS below  $V_{VAC\_OV}$  threshold
  - VBUS above  $V_{VBUSMin}$  (typical 3.8 V) when  $I_{BADSRC}$  (typical 30 mA) current is applied (not a poor source)
- input removed
- Charge Complete
- Any FAULT event in REG09
- VINDPM / IINDPM event detected (maskable)

When a fault occurs, the charger device sends out INT and keeps the fault state in REG09 until the host reads the fault register. Before the host reads REG09 and all the faults are cleared, the charger device would not send any INT upon new faults. To read the current fault status, the host has to read REG09 two times consecutively. The first read reports the pre-existing fault register status and the second read reports the current fault register status.

## 9.5 Protections

### 9.5.1 Voltage and Current Monitoring in Converter Operation

The device closely monitors the input and system voltage, as well as internal FET currents for safe buck and boost mode operation.

#### 9.5.1.1 Voltage and Current Monitoring in Buck Mode

##### 9.5.1.1.1 Input Overvoltage (ACOV)

If VBUS voltage exceeds  $V_{VAC\_OV}$  (programmable via OVP[2:0] bits), the device stops switching immediately.

During input overvoltage event (ACOV), the fault register CHRG\_FAULT bits are set to 01. An INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

##### 9.5.1.1.2 System Overvoltage Protection (SYSOVP)

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above minimum system regulation voltage when the system is regulate at  $V_{SYSMin}$ . Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30 mA discharge current to bring down the system voltage.

### 9.5.2 Voltage and Current Monitoring in Boost Mode

The device closely monitors the VBUS voltage, as well as RBFET and LSFET current to ensure safe boost mode operation.

### 9.5.2.1 VBUS Soft Start

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

### 9.5.2.2 VBUS Output Protection

The device monitors boost output voltage and other conditions to provide output short circuit and overvoltage protection. The Boost build in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on VBUS, the Boost turns off and retry 7 times. If retries are not successful, OTG is disabled with OTG\_CONFIG bit cleared. In addition, the BOOST\_FAULT bit is set and  $\overline{\text{INT}}$  pulse is generated. The BOOST\_FAULT bit can be cleared by host by re-enabling boost mode.

### 9.5.2.3 Boost Mode Overvoltage Protection

When the VBUS voltage rises above regulation target and exceeds VOTG\_OVP, the device enters overvoltage protection which stops switching, clears OTG\_CONFIG bit and exits boost mode. At Boost overvoltage duration, the fault register bit (BOOST\_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

## 9.5.3 Thermal Regulation and Thermal Shutdown

### 9.5.3.1 Thermal Protection in Buck Mode

The BQ25601D monitors the internal junction temperature  $T_J$  to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM\_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds  $T_{\text{SHUT}}$ (160°C). The fault register CHRG\_FAULT is set to 1 and an  $\overline{\text{INT}}$  is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is  $T_{\text{SHUT\_HYS}}$  (30°C) below  $T_{\text{SHUT}}$ (160°C).

### 9.5.3.2 Thermal Protection in Boost Mode

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds  $T_{\text{SHUT}}$  (160°C), the boost mode is disabled by setting OTG\_CONFIG bit low and BATFET is turned off. When IC junction temperature is below  $T_{\text{SHUT}}$ (160°C) -  $T_{\text{SHUT\_HYS}}$  (30°C), the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG\_CONFIG bit to recover.

## 9.5.4 Battery Protection

### 9.5.4.1 Battery Overvoltage Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT\_FAULT bit goes high and an INT is asserted to the host.

### 9.5.4.2 Battery Over-Discharge Protection

When battery is discharged below  $V_{\text{BAT\_DPL\_FALL}}$ , the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with  $I_{\text{SHORT}}$  (typically 100 mA) current when the  $V_{\text{BAT}} < V_{\text{SHORT}}$ , or precharge current as set in IPRECHG register when the battery voltage is between  $V_{\text{SHORTZ}}$  and  $V_{\text{BAT\_LOWV}}$ .

### 9.5.4.3 System Over-Current Protection

When the system is shorted or significantly overloaded ( $I_{\text{BAT}} > I_{\text{BATOP}}$ ) and the current exceeds BATFET overcurrent limit, the BATFET latches off. Section BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

## 9.6 Programming

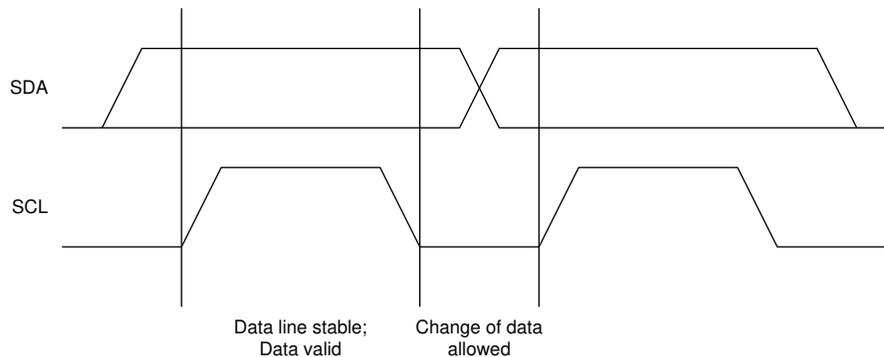
### 9.6.1 Serial Interface

The device uses I<sup>2</sup>C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I<sup>2</sup>CTM is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0B. Register read beyond REG0B (0x0B) returns 0xFF. The I<sup>2</sup>C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

#### 9.6.1.1 Data Validity

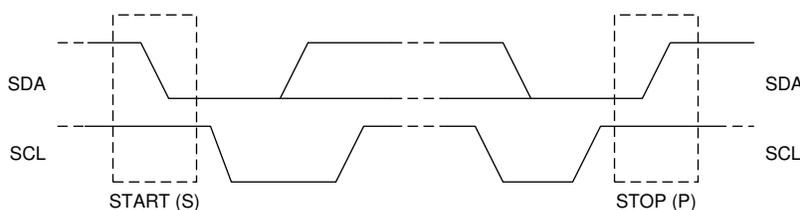
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.



**Figure 9-12. Bit Transfer on the I<sup>2</sup>C Bus**

#### 9.6.1.2 START and STOP Conditions

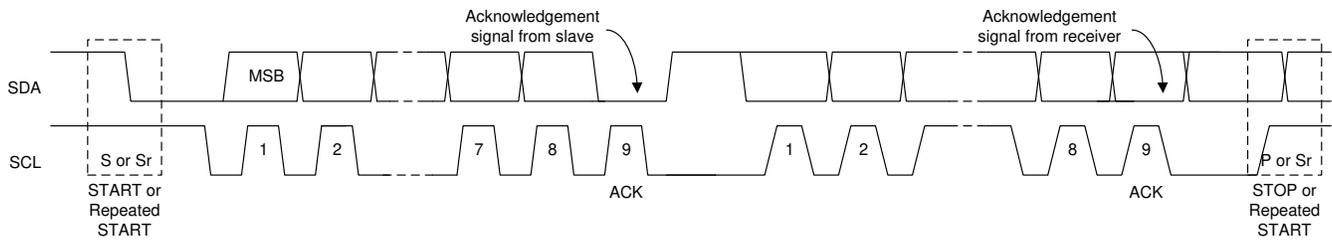
All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.



**Figure 9-13. TS START and STOP Conditions**

#### 9.6.1.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the mAsTter into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.



**Figure 9-14. Data Transfer on the I<sup>2</sup>C Bus**

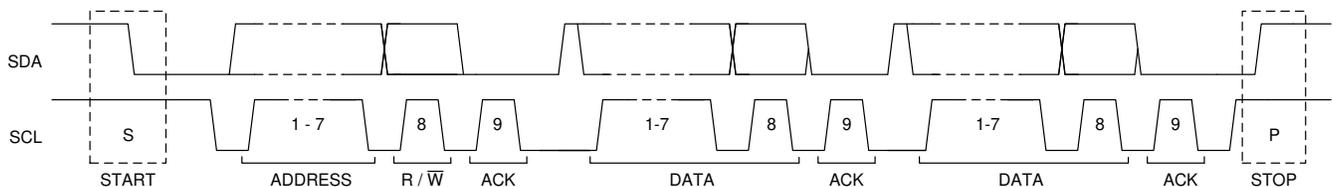
**9.6.1.4 Acknowledge (ACK) and Not Acknowledge (NACK)**

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

**9.6.1.5 Slave Address and Data Direction Bit**

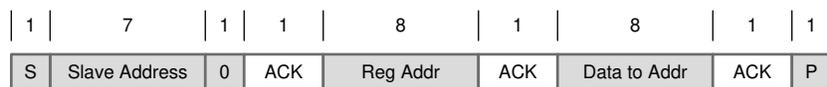
After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).



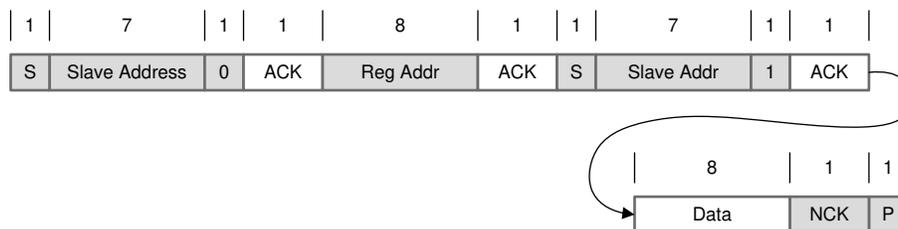
**Figure 9-15. Complete Data Transfer**

**9.6.1.6 Single Read and Write**

If the register address is not defined, the charger IC send back NACK and go back to the idle state.



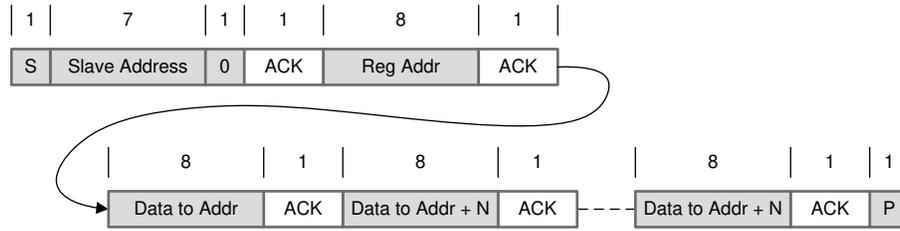
**Figure 9-16. Single Write**



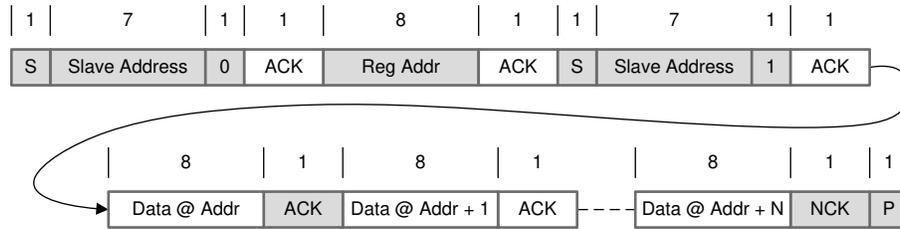
**Figure 9-17. Single Read**

**9.6.1.7 Multi-Read and Multi-Write**

The charger device supports multi-read and multi-write on REG00 through REG0B.



**Figure 9-18. Multi-Write**



**Figure 9-19. Multi-Read**

REG09 is a fault register. It keeps all the fault information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG09 for the second time. The only exception is NTC\_FAULT which always reports the actual condition on the TS pin. In addition, REG09 does not support multi-read and multi-write.

## 9.7 Register Maps

I<sup>2</sup>C Slave Address: 6BH

### 9.7.1 REG00 (address = 00) [reset = 00010111]

**Figure 9-20. REG00 Register**

7	6	5	4	3	2	1	0
EN_HIZ	EN_ICHG_MON[1]	EN_ICHG_MON[0]	IINDPM[4]	IINDPM[3]	IINDPM[2]	IINDPM[1]	IINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-6. REG00 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	0 – Disable, 1 – Enable	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	EN_ICHG_MON[1]	0	R/W	by REG_RST	00 - Enable STAT pin function (default)	
5	EN_ICHG_MON[0]	0	R/W	by REG_RST	01 - Reserved 10 - Reserved 11 - Disable STAT pin function (float pin)	
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default: 2400 mA (10111), maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed Host can over-write IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

**9.7.2 REG01 (address = 01) [reset = 00011010]**

**Figure 9-21. REG01 Register**

7	6	5	4	3	2	1	0
PFM_DIS	WD_RST	OTG_CONFIG	CHG_CONFIG	SYS_Min[2]	SYS_Min[1]	SYS_Min[0]	Min_V <sub>BAT_SEL</sub>
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-7. REG01 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	PFM_DIS	0	R/W	by REG_RST	0 – Enable PFM 1 – Disable PFM	Default: 0 - Enable
6	WD_RST	0	R/W	by REG_RST by Watchdog	I <sup>2</sup> C Watchdog Timer Reset 0 – Normal ; 1 – Reset	Default: Normal (0) Back to 0 after watchdog timer reset
5	OTG_CONFIG	0	R/W	by REG_RST by Watchdog	0 – OTG Disable 1 – OTG Enable	Default: OTG disable (0) Note: 1. OTG_CONFIG would override Charge Enable Function in CHG_CONFIG
4	CHG_CONFIG	1	R/W	by REG_RST by Watchdog	0 - Charge Disable 1- Charge Enable	Default: Charge Battery (1) Note: 1. Charge is enabled when both CE pin is pulled low AND CHG_CONFIG bit is 1.
3	SYS_Min[2]	1	R/W	by REG_RST	System Minimum Voltage	000: 2.6 V 001: 2.8 V 010: 3 V 011: 3.2 V 100: 3.4 V 101: 3.5 V 110: 3.6 V 111: 3.7 V Default: 3.5 V (101)
2	SYS_Min[1]	0	R/W	by REG_RST		
1	SYS_Min[0]	1	R/W	by REG_RST		
0	Min_V <sub>BAT_SEL</sub>	0	R/W	by REG_RST	0 – 2.8 V BAT falling, 1 – 2.5 V BAT falling	Minimum battery voltage for OTG mode. Default falling 2.8 V (0); Rising threshold 3.0 V (0)

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.3 REG02 (address = 02) [reset = 10100 010]

**Figure 9-22. REG02 Register**

7	6	5	4	3	2	1	0
BOOST_LIM	Q1_FULLLON	ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-8. REG02 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	BOOST_LIM	1	R/W	by REG_RST by Watchdog	0 = 0.5 A 1 = 1.2 A	Default: 1.2 A (1) Note: The current limit options listed are minimum current limit specs.
6	Q1_FULLLON	0	R/W	by REG_RST	0 – Use higher Q1 RDSON when programmed IINDPM < 700mA (better accuracy) 1 – Use lower Q1 RDSON always (better efficiency)	In boost mode, full FET is always used and this bit has no effect
5	ICHG[5]	1	R/W	by REG_RST by Watchdog	1920 mA	Fast Charge Current Default: 2040mA (100010) Range: 0 mA (0000000) – 3000 mA (110010) Note: I <sub>CHG</sub> = 0 mA disables charge. I <sub>CHG</sub> > 3000 mA (110010 clamped to register value 3000 mA (110010))
4	ICHG[4]	0	R/W	by REG_RST by Watchdog	960 mA	
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ICHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ICHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.4 REG03 (address = 03) [reset = 001 0001 0]

**Figure 9-23. Register REG03**

7	6	5	4	3	2	1	0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-9. REG03 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	Precharge Current Default: 180 mA (0010) Offset: 60 mA Note: IPRECHG > 780 mA clamped to 780 mA (1100)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
5	IPRECHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
4	IPRECHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	480 mA	Termination Current Default: 180 mA (0010) Offset: 60 mA
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ITERM[0]	0	R/W	by REG_RST by Watchdog	60 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.5 REG04 (address = 04) [reset = 01011000]

**Figure 9-24. Register REG04**

7	6	5	4	3	2	1	0
VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	TOPOFF_TIME R[1]	TOPOFF_TIME R[0]	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-10. REG04 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.847 V Range: 3.847 V to 4.615 V (11000) Default: 4.199 V (01011) Special Value: (01111): 4.343 V Note: Value above 11000 (4.615 V) is clamped to register value 11000 (4.615 V)
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256 mV	
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128 mV	
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64 mV	
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32 mV	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	00 – Disabled (Default) 01 – 15 minutes	The extended time following the termination condition is met. When disabled, charge terminated when termination conditions are met
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog	10 – 30 minutes 11 – 45 minutes	
0	VRECHG	0	R/W	by REG_RST by Watchdog	0 – 100 mV 1 – 200 mV	Recharge threshold Default: 100mV (0)

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.6 REG05 (address = 05) [reset = 10011111]

**Figure 9-25. Register REG05**

7	6	5	4	3	2	1	0
EN_TERM	Reserved	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER	TREG	JEITA_ISET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-11. REG05 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	EN_TERM	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable	Default: Enable termination (1)
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	00 – Disable timer, 01 – 40 s, 10 – 80 s, 11 – 160 s	Default: 40 s (01)
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog		
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable both fast charge and precharge timer	Default: Enable (1)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	0 – 5 hrs 1 – 10 hrs	Default: 10 hours (1)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 - 90°C 1 - 110°C	Default: 110°C (1)
0	JEITA_ISET (0C-10C)	1	R/W	by REG_RST by Watchdog	0 – 50% of ICHG 1 – 20% of ICHG	Default: 20% (1)

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.7 REG06 (address = 06) [reset = 01100110]

**Figure 9-26. Register REG06**

7	6	5	4	3	2	1	0
OVP[1]	OVP[0]	BOOSTV[1]	BOOSTV[0]	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-12. REG06 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	OVP[1]	0	R/W	by REG_RST	Default: 6.5V (01)	VAC OVP threshold: 00 - 5.5 V 01 – 6.5 V (5-V input) 10 – 10.5 V (9-V input) 11 – 14 V (12-V input)
6	OVP[0]	1	R/W	by REG_RST		
5	BOOSTV[1]	1	R/W	by REG_RST		Boost Regulation Voltage: 00 - 4.85V 01 - 5.00V 10 - 5.15V 11 - 5.30V
4	BOOSTV[0]	0	R/W	by REG_RST		
3	VINDPM[3]	0	R/W	by REG_RST	800 mV	Absolute VINDPM Threshold Offset: 3.9 V Range: 3.9 V (0000) – 5.4 V (1111) Default: 4.5V (0110)
2	VINDPM[2]	1	R/W	by REG_RST	400 mV	
1	VINDPM[1]	1	R/W	by REG_RST	200 mV	
0	VINDPM[0]	0	R/W	by REG_RST	100 mV	

(1) LEGEND: R/W = Read/Write; R = Read only

**9.7.8 REG07 (address = 07) [reset = 01001100]**

**Figure 9-27. Register REG07**

7	6	5	4	3	2	1	0
IINDET_EN	TMR2X_EN	BATFET_DIS	JEITA_VSET	BATFET_DLY	BATFET_RST_EN	VDPM_BAT_TRACK[1]	VDPM_BAT_TRACK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 9-13. REG07 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description	Comment
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	0 - Not in input current limit detection 1 - Force input current limit detection when VBUS is present	Returns to 0 after input detection is complete
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Safety timer slowed by 2X during input DPM (both V and I) or JEITA cool, or thermal regulation	
5	BATFET_DIS	0	R/W	by REG_RST	0 – Allow Q4 turn on, 1 – Turn off Q4 with t <sub>BATFET_DLY</sub> delay time (REG07[3])	Default: Allow Q4 turn on(0)
4	JEITA_VSET (45C-60C)	0	R/W	by REG_RST by Watchdog	0 – Set Charge Voltage to 4.1V ( max), 1 – Set Charge Voltage to VREG	
3	BATFET_DLY	1	R/W	by REG_RST	0 – Turn off BATFET immediately when BATFET_DIS bit is set 1 – Turn off BATFET after t <sub>BATFET_DLY</sub> (typ. 10 s) when BATFET_DIS bit is set	Default: 1 Turn off BATFET after t <sub>BATFET_DLY</sub> (typ. 10 s) when BATFET_DIS bit is set
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	0 – Disable BATFET reset function 1 – Enable BATFET reset function	Default: 1 Enable BATFET reset function
1	VDPM_BAT_TRACK[1]	0	R/W	by REG_RST	00 - Disable function (VINDPM set by register) 01 - VBAT + 200mV 10 - VBAT + 250mV 11 - VBAT + 300mV	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT + VDPM_BAT_TRACK
0	VDPM_BAT_TRACK[0]	0	R/W	by REG_RST		

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.9 REG08 (address = 08) [reset = xxxxxxxx]

**Figure 9-28. Register REG08**

7	6	5	4	3	2	1	0
VBUS_STAT[2]	VBUS_STAT[1]	VBUS_STAT[0]	CHRG_STAT[1]	CHRG_STAT[0]	PG_STAT	THERM_STAT	VSYS_STAT
R	R	R	R	R	R	R	R

**Table 9-14. REG08 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description
7	VBUS_STAT[2]	x	R	NA	VBUS Status register BQ25601D 000: No input 001: USB Host SDP 010: USB CDP: (1.5A) 011: USB DCP (2.4 A) 101: Unknown Adapter (500 mA) 110: Non-Standard Adapter (1A/2A/2.1A/2.4A) 111: OTG Software current limit is reported in IINDPM register
6	VBUS_STAT[1]	x	R	NA	
5	VBUS_STAT[0]	x	R	NA	
4	CHRG_STAT[1]	x	R	NA	Charging status: 00 – Not Charging 01 – Pre-charge ( $< V_{BATLOWV}$ ) 10 – Fast Charging 11 – Charge Termination
3	CHRG_STAT[0]	x	R	NA	
2	PG_STAT	x	R	NA	Power Good status: 0 – Power Not Good 1 – Power Good
1	THERM_STAT	x	R	NA	0 – Not in ther mA regulation 1 – in ther mA regulation
0	VSYS_STAT	x	R	NA	0 – Not in VSYSMin regulation ( $BAT > VSYSMin$ ) 1 – in VSYSMin regulation ( $BAT < VSYSMin$ )

(1) LEGEND: R/W = Read/Write

**9.7.10 REG09 (address = 09) [reset = xxxxxxxx]**

**Figure 9-29. Register REG09**

7	6	5	4	3	2	1	0
WATCHDOG_FAULT	BOOST_FAULT	CHRG_FAULT[1]	CHRG_FAULT[0]	BAT_FAULT	NTC_FAULT[2]	NTC_FAULT[1]	NTC_FAULT[0]
R	R	R	R	R	R	R	R

**Table 9-15. REG09 Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description
7	WATCHDOG_FAULT	x	R	NA	0 – Normal, 1- Watchdog timer expiration
6	BOOST_FAULT	x	R	NA	0 – Normal, 1 – VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that we cannot start boost function)
5	CHRG_FAULT[1]	x	R	NA	00 – Normal, 01 – input fault (VAC OVP or VBAT < VBUS < 3.8 V), 10 - Thermal shutdown, 11 – Charge Safety Timer Expiration
4	CHRG_FAULT[0]	x	R	NA	
3	BAT_FAULT	x	R	NA	0 – Normal, 1 – BATOVP
2	NTC_FAULT[2]	x	R	NA	JEITA 000 – Normal, 010 – Warm, 011 – Cool, 101 – Cold, 110 – Hot (Buck mode)
1	NTC_FAULT[1]	x	R	NA	
0	NTC_FAULT[0]	x	R	NA	

(1) LEGEND: R/W = Read/Write; R = Read only

### 9.7.11 REG0A (address = 0A) [reset = xxxxxx00]

**Figure 9-30. Register REG0A**

7	6	5	4	3	2	1	0
VBUS_GD	VINDPM_STAT	IINDPM_STAT	Reserved	TOPOFF_ACTI VE	ACOV_STAT	VINDPM_INT_ MASK	IINDPM_INT_ MASK
R	R	R	R	R	R	R/W	R/W

**Table 9-16. REG0A Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description
7	VBUS_GD	x	R	NA	0 – Not VBUS attached, 1 – VBUS Attached
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM, 1 – in VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM, 1 – in IINDPM
4	Reserved	x	R	NA	
3	TOPOFF_ACTIVE	x	R	NA	0 – Top off timer not counting. 1 – Top off timer counting
2	ACOV_STAT	x	R	NA	0 – Device is NOT in ACOV 1 – Device is in ACOV
1	VINDPM_INT_MASK	0	R/W	by REG_RST	0 - Allow VINDPM INT pulse 1 - Mask VINDPM INT pulse
0	IINDPM_INT_MASK	0	R/W	by REG_RST	0 - Allow IINDPM INT pulse 1 - Mask IINDPM INT pulse

(1) LEGEND: R/W = Read/Write; R = Read only

**9.7.12 REG0B (address = 0B) [reset = 00111xxx]**

**Figure 9-31. Register REG0B**

7	6	5	4	3	2	1	0
REG_RST	PN[3]	PN[2]	PN[1]	PN[0]	Reserved	DEV_REV[1]	DEV_REV[0]
R/W	R	R	R	R	R	R	R

**Table 9-17. REG0B Field Descriptions**

Bit	Field	POR	Type <sup>(1)</sup>	Reset	Description
7	REG_RST	0	R/W	NA	Register reset 0 – Keep current register setting 1 – Reset to default register value and reset safety timer Note: Bit resets to 0 after register reset is completed
6	PN[3]	0	R	NA	BQ25601D : 0010
5	PN[2]	1	R	NA	
4	PN[1]	1	R	NA	
3	PN[0]	1	R	NA	
2	Reserved	x	R	NA	
1	DEV_REV[1]	x	R	NA	
0	DEV_REV[0]	x	R	NA	

(1) LEGEND: R/W = Read/Write; R = Read only

## Application and Implementation

---

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

### 10.1 Application information

A typical application consists of the device configured as an I<sup>2</sup>C controlled power path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.



$$I_{\text{RIPPLE}} = \frac{V_{\text{IN}} \times D \times (1 - D)}{f_s \times L} \quad (4)$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

### 10.2.2.2 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current  $I_{\text{CIN}}$  occurs where the duty cycle is closest to 50% and can be estimated using [Equation 5](#).

$$I_{\text{CIN}} = I_{\text{CHG}} \times \sqrt{D \times (1 - D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15 V input voltage. Capacitance of 22- $\mu\text{F}$  is suggested for typical of 3A charging current.

### 10.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. [Equation 6](#) shows the output capacitor RMS current  $I_{\text{COUT}}$  calculation.

$$I_{\text{COUT}} = \frac{I_{\text{RIPPLE}}}{2 \times \sqrt{3}} \approx 0.29 \times I_{\text{RIPPLE}} \quad (6)$$

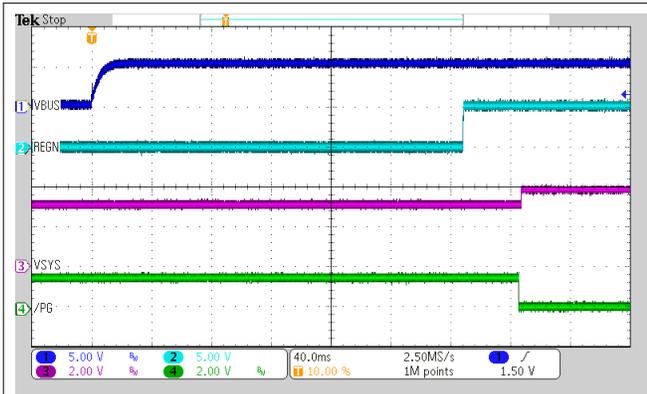
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_{\text{O}} = \frac{V_{\text{OUT}}}{8LCf_s^2} \left( 1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right) \quad (7)$$

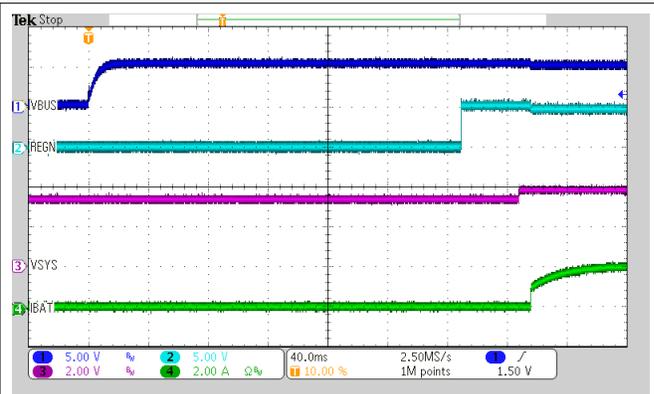
At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensation optimized for  $\leq 20\mu\text{F}$  ceramic output capacitance. The preferred ceramic capacitor is 10V rating, X7R or X5R.

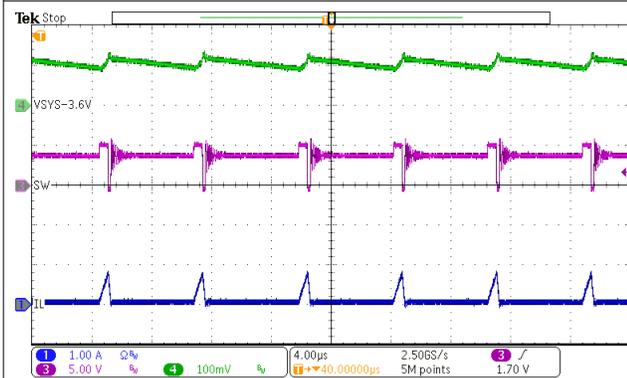
### 10.2.3 Application Curves



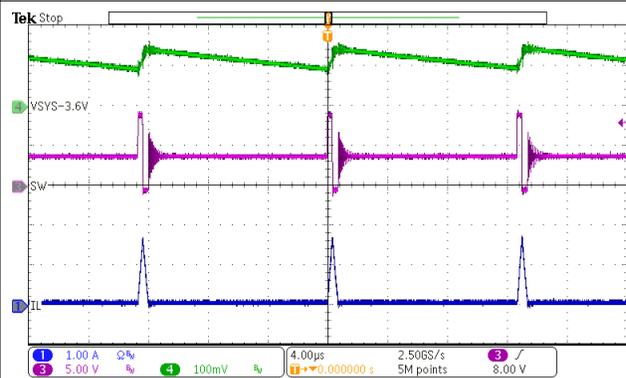
$V_{VBUS} = 5\text{ V}$        $V_{VBAT} = 3.2\text{ V}$   
**Figure 10-2. Power-Up with Charge Disabled**



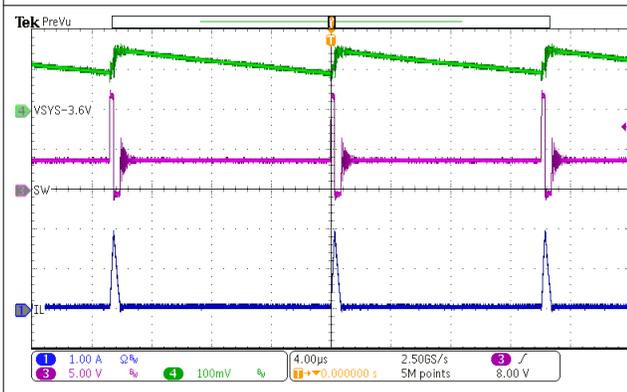
$V_{VBUS} = 5\text{ V}$        $V_{VBAT} = 3.2\text{ V}$   
 $I_{CHG} = 2\text{ A}$   
**Figure 10-3. Power-Up with Charge Enabled**



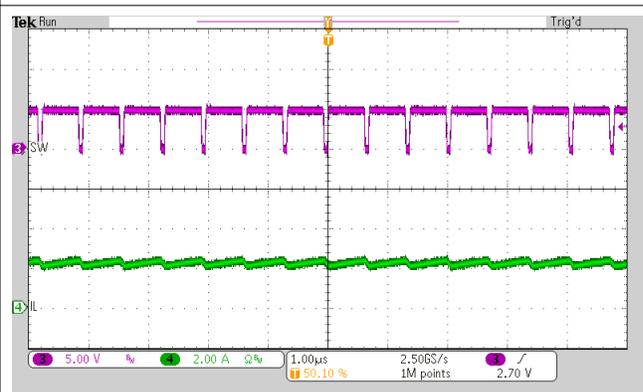
$V_{VBUS} = 5\text{ V}$       Charge Disabled  
 $I_{SYS} = 50\text{ mA}$   
**Figure 10-4. PFM Switching in Buck Mode**



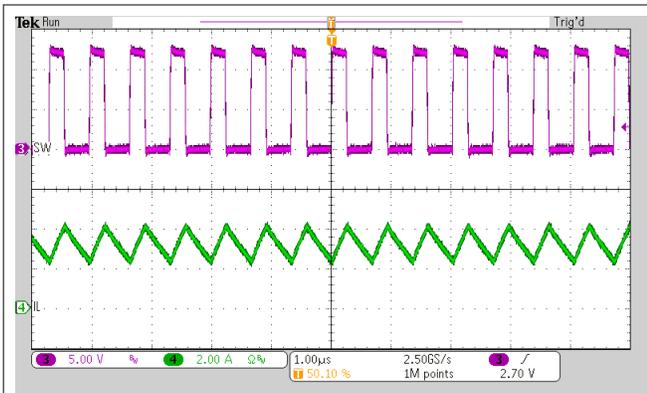
$V_{VBUS} = 9\text{ V}$       Charge Disabled  
 $I_{SYS} = 50\text{ mA}$   
**Figure 10-5. PFM Switching in Buck Mode**



$V_{VBUS} = 12\text{ V}$       Charge Disabled  
 $I_{SYS} = 50\text{ mA}$   
**Figure 10-6. PFM Switching in Buck Mode**

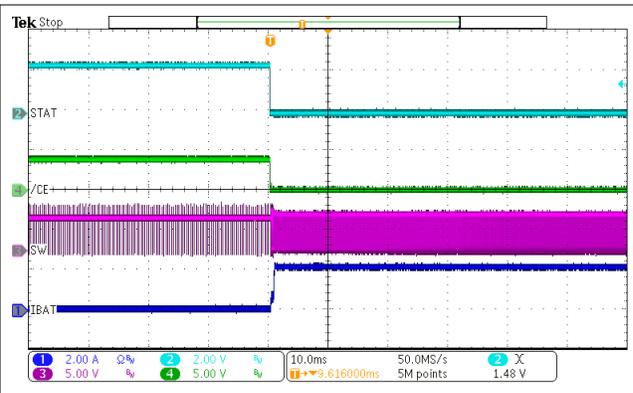


$V_{VBUS} = 5\text{ V}$        $V_{VBAT} = 3.8\text{ V}$   
 $I_{CHG} = 2\text{ A}$   
**Figure 10-7. PWM Switching in Buck Mode**



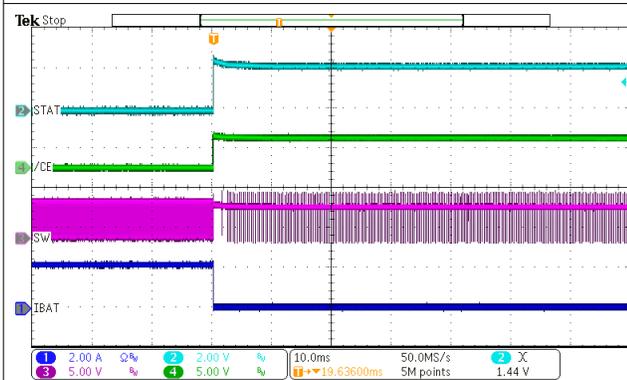
$V_{VBUS} = 12\text{ V}$                        $V_{VBAT} = 3.8\text{ V}$   
 $I_{CHG} = 2\text{ A}$

**Figure 10-8. PWM Switching in Buck Mode**



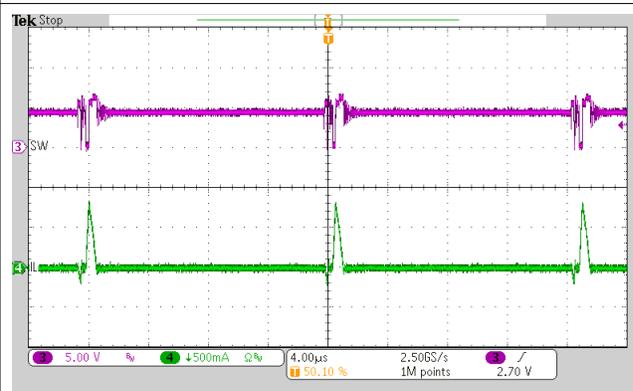
$V_{VBUS} = 5\text{ V}$                                $V_{VBAT} = 3.2\text{ V}$   
 $I_{CHG} = 2\text{ A}$

**Figure 10-9. Charge Enable**



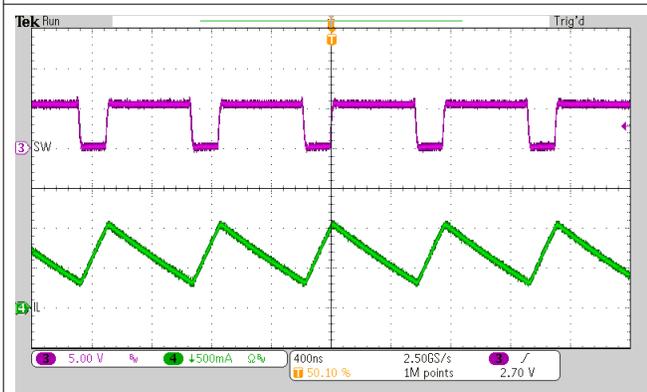
$V_{VBUS} = 5\text{ V}$                                $V_{VBAT} = 3.2\text{ V}$   
 $I_{CHG} = 2\text{ A}$

**Figure 10-10. Charge Disable**



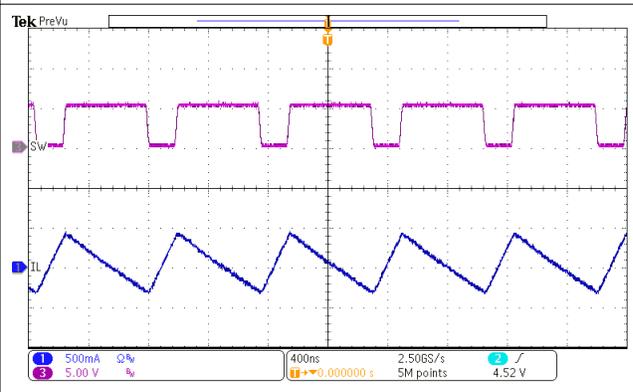
$V_{VBAT} = 4\text{ V}$   
 $I_{LOAD} = 50\text{ mA}$                               PFM Enabled

**Figure 10-11. OTG Switching**



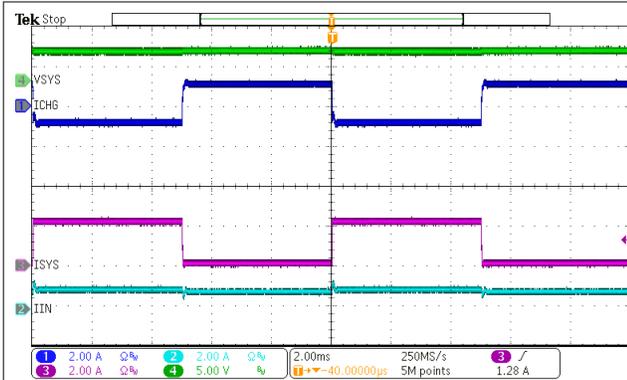
$V_{VBAT} = 4\text{ V}$   
 $I_{LOAD} = 1\text{ A}$                                       PFM Enabled

**Figure 10-12. OTG Switching**



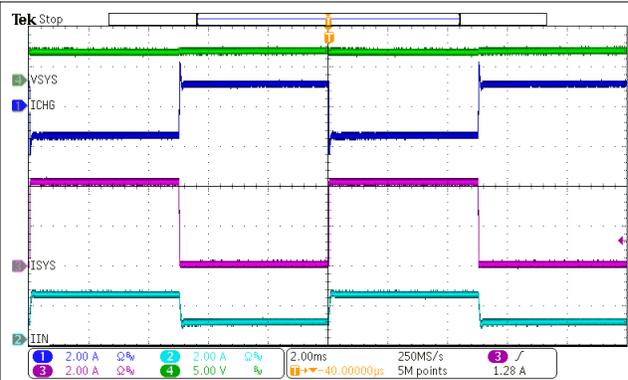
$V_{VBAT} = 4\text{ V}$   
 $I_{LOAD} = 0\text{ A}$                                       PFM Disabled

**Figure 10-13. OTG Switching**



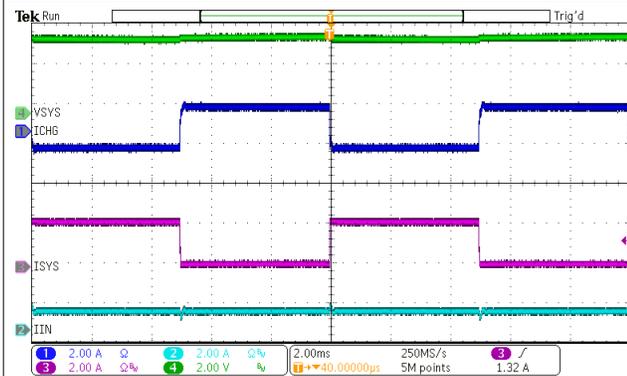
$V_{BUS} = 5\text{ V}$   
 $I_{SYS}$  from 0 A to 2 A  
 $V_{BAT} = 3.7\text{ V}$   
 $I_{INDPM} = 1\text{ A}$   
 $I_{CHG} = 1\text{ A}$

**Figure 10-14. System Load Transient**



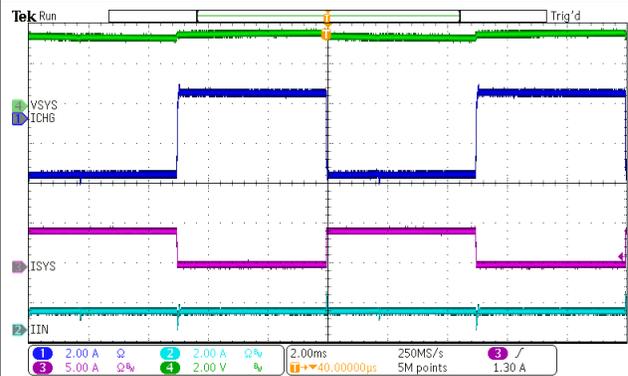
$V_{BUS} = 5\text{ V}$   
 $I_{SYS}$  from 0 A to 4 A  
 $V_{BAT} = 3.7\text{ V}$   
 $I_{INDPM} = 2\text{ A}$   
 $I_{CHG} = 1\text{ A}$

**Figure 10-15. System Load Transient**



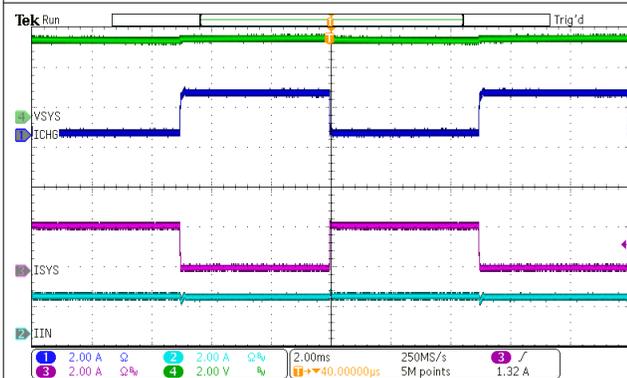
$V_{BUS} = 5\text{ V}$   
 $I_{SYS}$  from 0 A to 2 A  
 $V_{BAT} = 3.7\text{ V}$   
 $I_{INDPM} = 1\text{ A}$   
 $I_{CHG} = 2\text{ A}$

**Figure 10-16. System Load Transient**



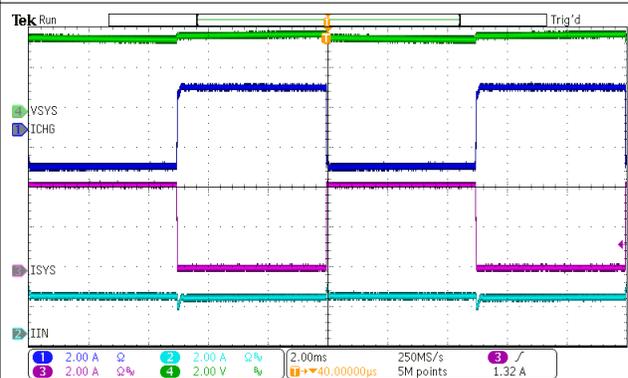
$V_{BUS} = 5\text{ V}$   
 $I_{SYS}$  from 0 A to 4 A  
 $V_{BAT} = 3.7\text{ V}$   
 $I_{INDPM} = 1\text{ A}$   
 $I_{CHG} = 2\text{ A}$

**Figure 10-17. System Load Transient**



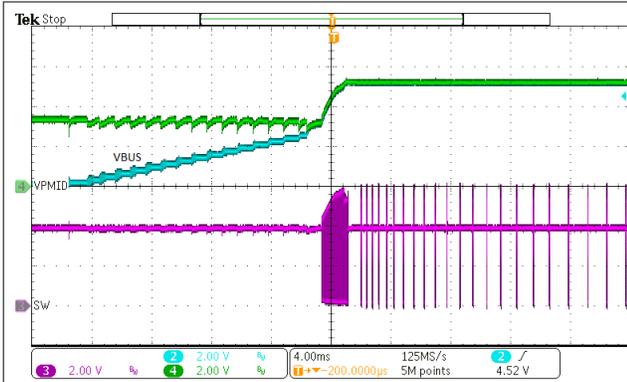
$V_{BUS} = 5\text{ V}$   
 $I_{SYS}$  from 0 A to 2 A  
 $V_{BAT} = 3.7\text{ V}$   
 $I_{INDPM} = 2\text{ A}$   
 $I_{CHG} = 2\text{ A}$

**Figure 10-18. System Load Transient**



$V_{BUS} = 5\text{ V}$   
 $I_{SYS}$  from 0 A to 4 A  
 $V_{BAT} = 3.7\text{ V}$   
 $I_{INDPM} = 2\text{ A}$   
 $I_{CHG} = 2\text{ A}$

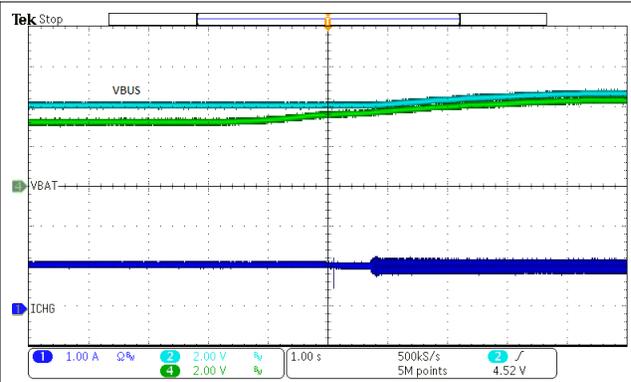
**Figure 10-19. System Load Transient**



$V_{BAT} = 3.8\text{ V}$

$C_{LOAD} = 470\text{ }\mu\text{F}$

**Figure 10-20. OTG Start-Up**



Adaptor  $I_{LIM} = 1\text{ A}$

**Figure 10-21. VINDPM Tracking Battery Voltage**

## Power Supply Recommendations

in order to provide an output voltage on SYS, the BQ25601D device requires a power supply between 3.9 V and 14.2 V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with voltage  $> V_{BATUVLO}$  connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter of the charger to provide maximum output power to SYS.

## 10 Layout

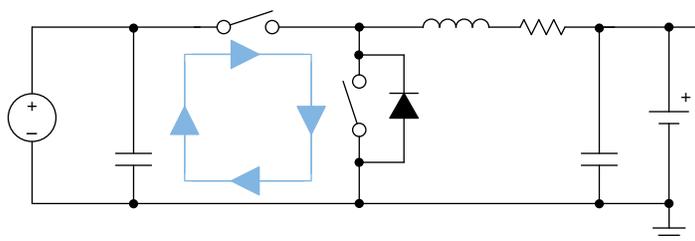
### 10.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see [Figure 10-1](#)) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

See the EVM user's guide [BQ25601 and BQ25601D \(PWR877\) Evaluation Module User's Guide](#) for the recommended component placement with trace and via locations. For the VQFN information, refer to [Quad Flatpack No-Lead Logic Packages Application Report](#) and [QFN and SON PCB Attachment Application Report](#).

### 10.2 Layout Example



**Figure 10-1. High Frequency Current Path**

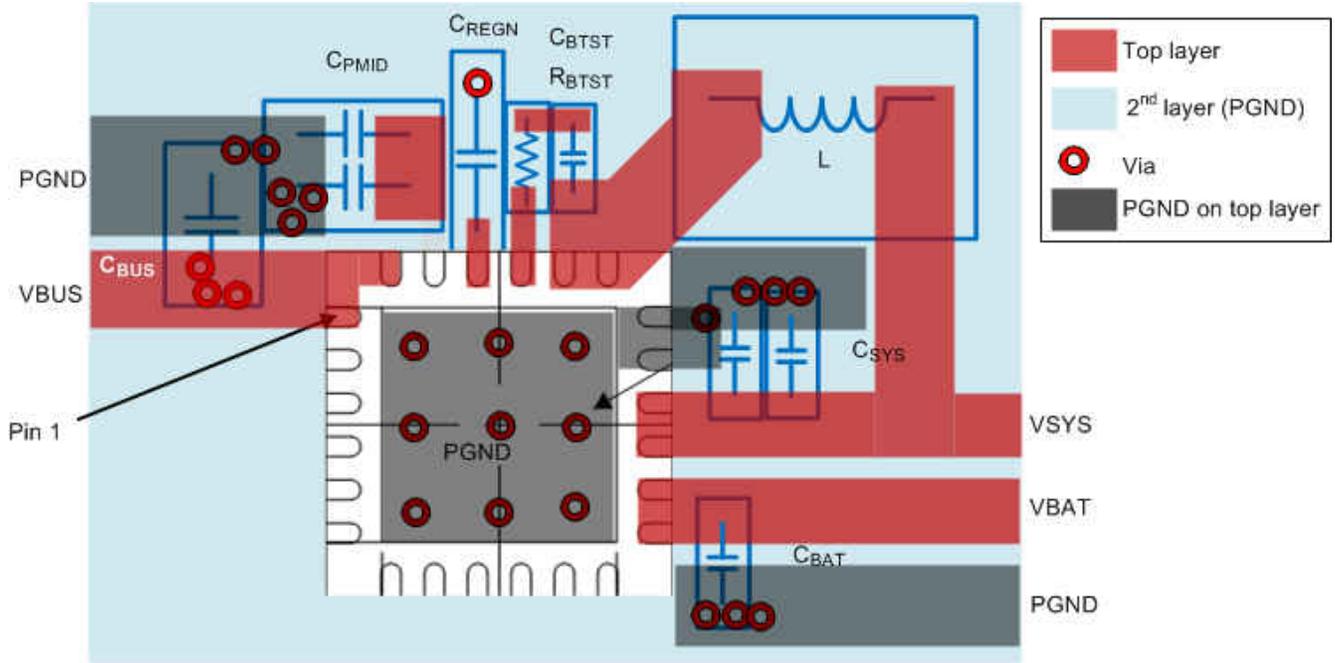


Figure 10-2. Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

- [BQ25601 and BQ25601D \(PWR877\) Evaluation Module User's Guide](#)

### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## **Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25601DRTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D	
BQ25601DRTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25601D	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

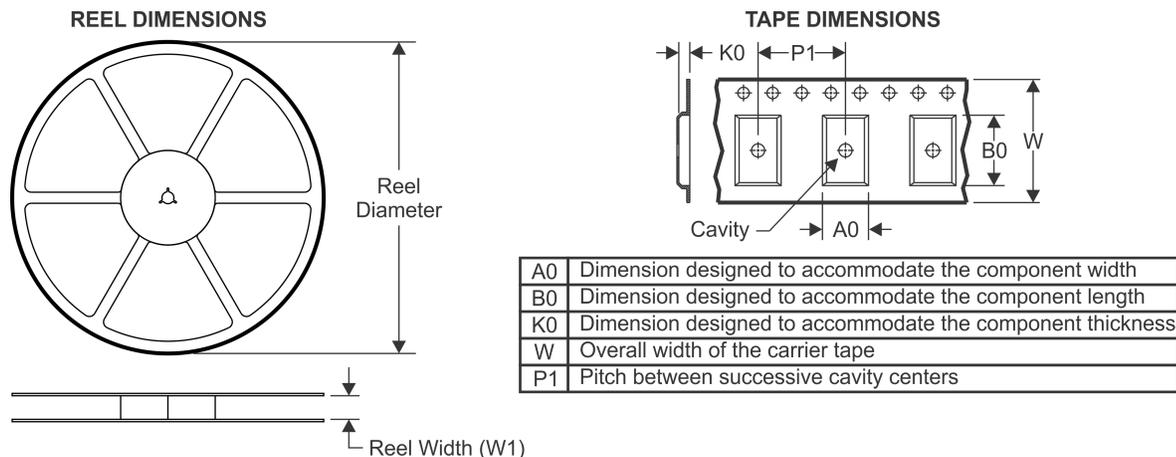
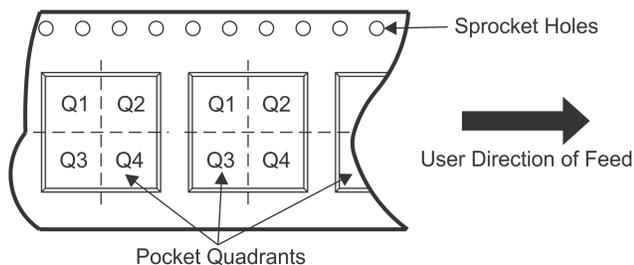
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

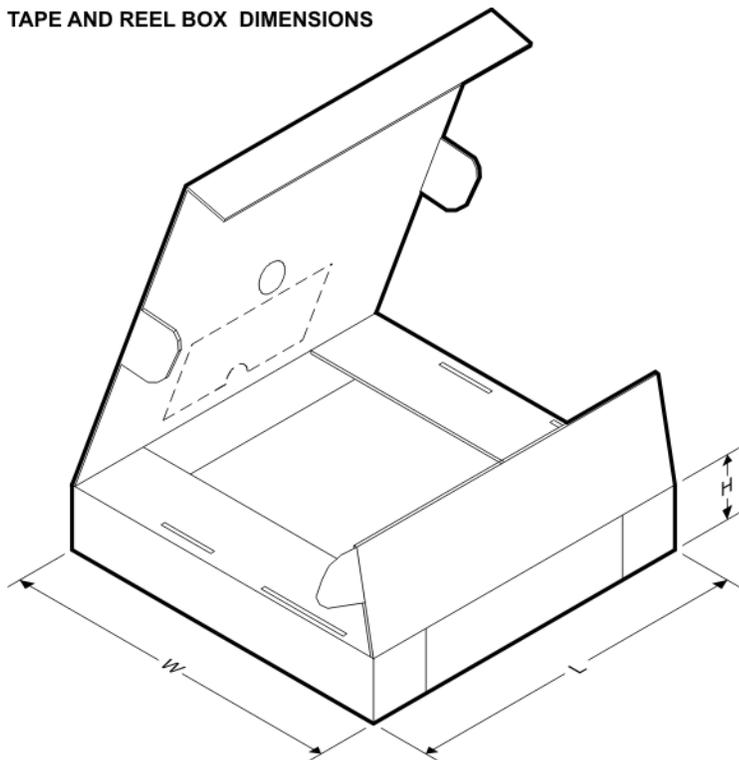
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25601DRTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25601DRTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25601DRTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
BQ25601DRTWT	WQFN	RTW	24	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

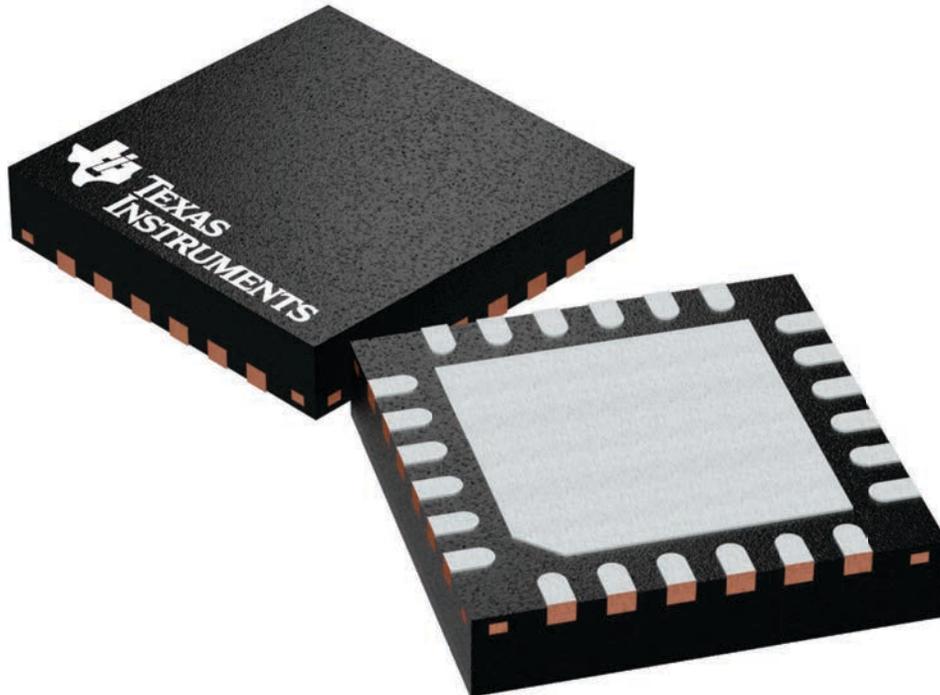
**RTW 24**

**WQFN - 0.8 mm max height**

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

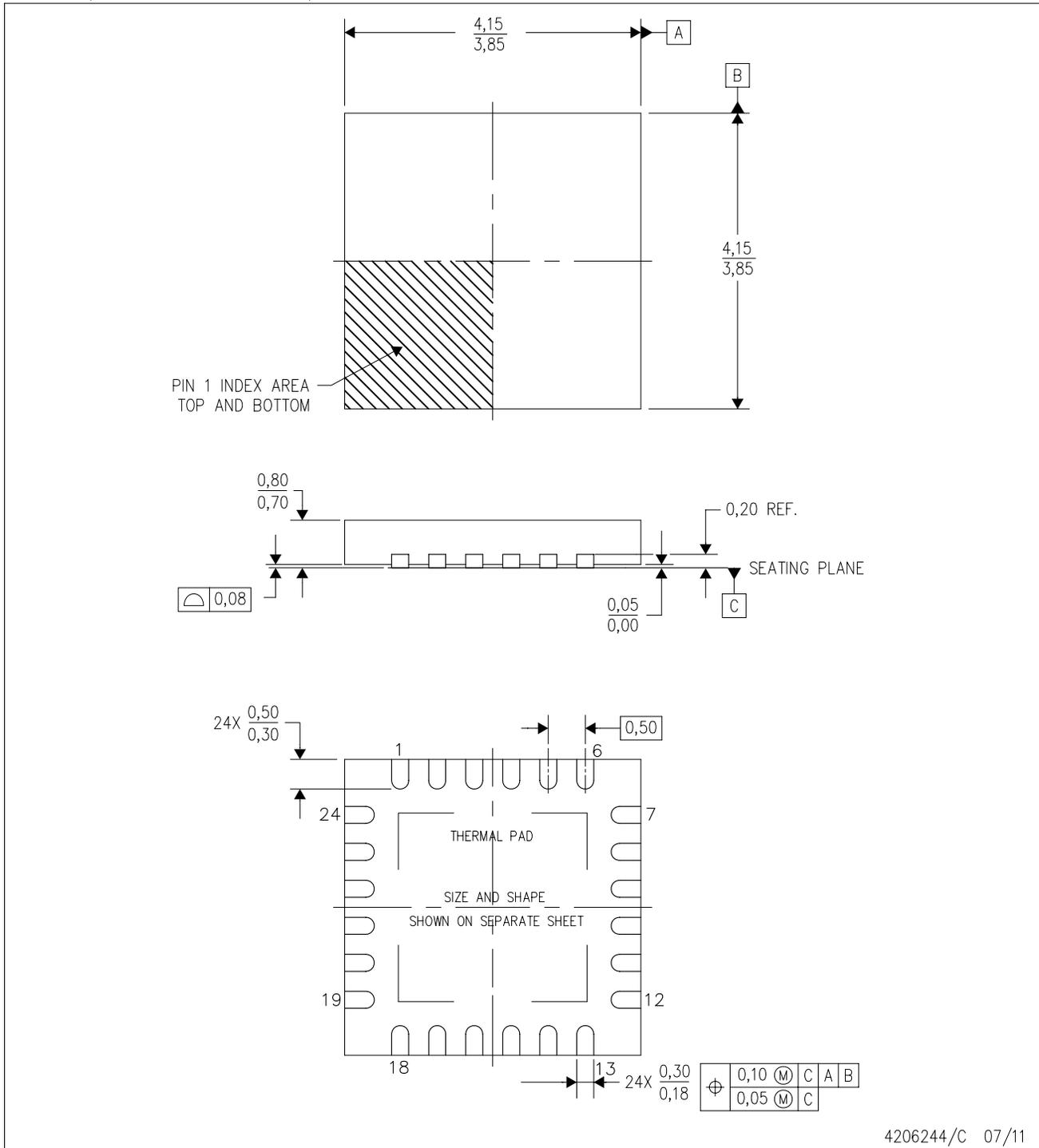
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224801/A

RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4206244/C 07/11

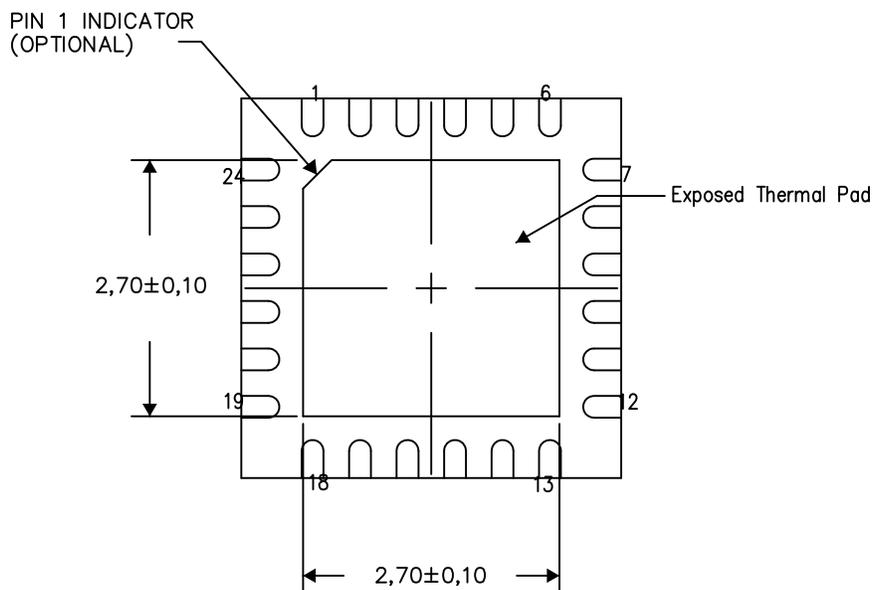
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

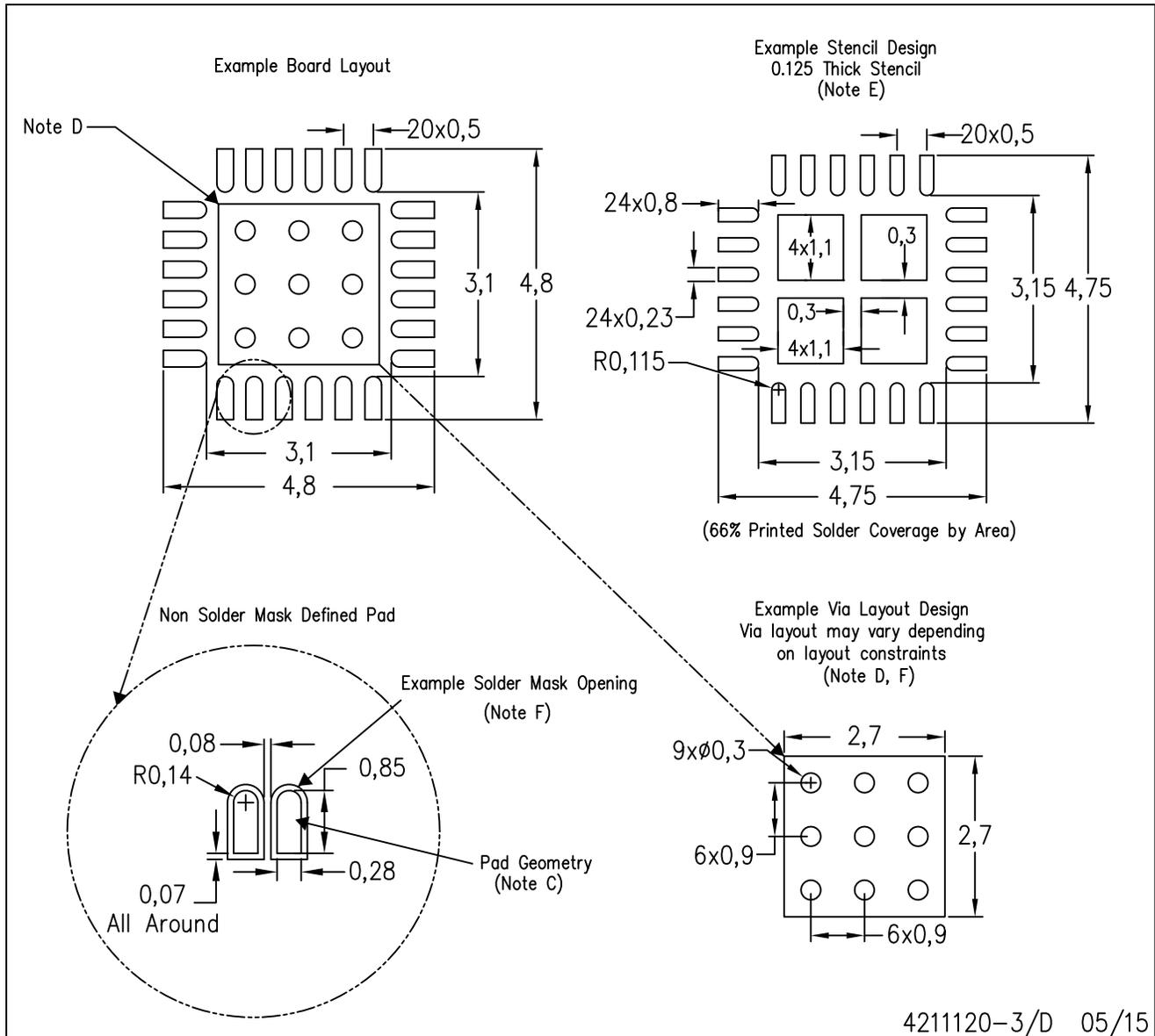
Exposed Thermal Pad Dimensions

4206249-5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S-PWQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated