DATA SHEET

BFM505
Dual NPN wideband transistor

Product specification
Supersedes data of 1995 Sep 04

1996 Oct 08

Dual NPN wideband transistor BFM505

FEATURES

- Small size
- Temperature and h_{FE} matched
- Low noise and high gain
- High gain at low current and low capacitance at low voltage
- Gold metallization ensures excellent reliability.

APPLICATIONS

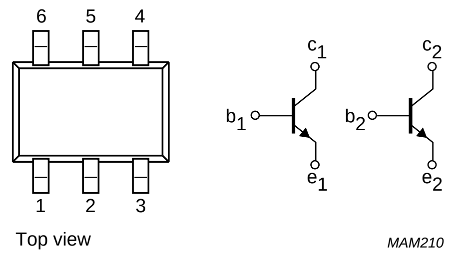
- Oscillator and buffer amplifiers
- Balanced amplifiers
- LNA/mixer.

DESCRIPTION

Dual transistor with two silicon NPN RF dies in a surface mount, 6-pin SOT363 (S-mini) package. The transistors are primarily intended for wideband applications in the GHz-range in the RF front end of analog and digital cellular phones, cordless phones, radar detectors, pagers and satellite TV-tuners.

PINNING - SOT363A

PIN	SYMBOL	DESCRIPTION
1	b_1	base 1
2	e_1	emitter 1
3	c_2	collector 2
4	b_2	base 2
5	e_2	emitter 2
6	c_1	collector 1



Marking code: N0.

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Any single transistor						
C_{re}	feedback capacitance	$I_e = 0$; $V_{CB} = 3$ V; f = 1 MHz	–	0.22	–	pF
f_T	transition frequency	$I_C = 5$ mA; $V_{CE} = 3$V; f = 1 GHz	–	9	–	GHz
$\|s_{21}\|^2$	insertion power gain	$I_C = 5$ mA; $V_{CE} = 3$ V; f = 900 MHz; $T_{amb} = 25$ °C	14	15	–	dB
G_{UM}	maximum unilateral power gain	$I_C = 5$ mA; $V_{CE} = 3$ V; f = 900 MHz; $T_{amb} = 25$ °C	–	17	–	dB
F	noise figure	$I_C = 1$ mA; $V_{CE} = 3$ V; f = 900 MHz; $\Gamma_S = \Gamma_{opt}$	–	1.1	1.6	dB
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	single loaded	–	–	230	K/W
		double loaded	–	–	115	K/W

LIMITING VALUES

In accordance with the Absolute Maximum System IEC 134.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Any single transistor					
V_{CBO}	collector-base voltage	open emitter	–	20	V
V_{CEO}	collector-emitter voltage	open base	–	8	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	DC collector current		–	18	mA
P_{tot}	total power dissipation	up to T_s = 118 °C; note 1	–	500	mW
T_{stg}	storage temperature		–65	+175	°C
T_j	junction temperature		–	175	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point; note 1	single loaded	230	K/W
		double loaded	115	K/W

Note to the Limiting values and Thermal characteristics

1. T_s is the temperature at the soldering point of the collector pin.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC characteristics of any single transistor						
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 2.5 μA; I_E = 0	20	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 10 μA; I_B = 0	8	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 2.5 μA; I_C = 0	2.5	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 6 V; I_E = 0	–	–	50	nA
h_{FE}	DC current gain	I_C = 5 mA; V_{CE} = 6 V	60	120	250	
DC characteristics of the dual transistor						
Δh_{FE}	ratio of highest and lowest DC current gain	$I_{C1} = I_{C2}$ = 5 mA; $V_{CE1} = V_{CE2}$ = 6 V	1	1.2	–	
ΔV_{BEO}	difference between highest and lowest base-emitter voltage (offset voltage)	$I_{E1} = I_{E2}$ = 10 mA; T_{amb} = 25 °C	0	1	–	mV
AC characteristics of any single transistor						
f_T	transition frequency	I_C = 5 mA; V_{CE} = 3 V; f = 1 GHz	–	9	–	GHz
C_c	collector capacitance	$I_E = i_e$ = 0; V_{CB} = 3 V; f = 1 MHz	–	0.31	–	pF
C_{re}	feedback capacitance	I_C = 0; V_{CB} = 3 V; f = 1 MHz	–	0.22	–	pF
G_{UM}	maximum unilateral power gain; note 1	I_C = 5 mA; V_{CE} = 3 V; T_{amb} = 25 °C; f = 900 MHz	–	17	–	dB
		I_C = 5 mA; V_{CE} = 3 V; T_{amb} = 25 °C; f = 2 GHz	–	10	–	dB
$\lvert s_{21}\rvert^2$	insertion power gain	I_C = 5 mA; V_{CE} = 3 V; f = 900 MHz; T_{amb} = 25 °C	14	15	–	dB
F	noise figure	I_C = 5 mA; V_{CE} = 3 V; f = 900 MHz; $\Gamma_S = \Gamma_{opt}$	–	1.4	1.8	dB
		I_C = 5 mA; V_{CE} = 3 V; f = 2 GHz; $\Gamma_S = \Gamma_{opt}$	–	1.9	–	dB
		I_C = 1 mA; V_{CE} = 3 V; f = 900 MHz; $\Gamma_S = \Gamma_{opt}$	–	1.1	1.6	dB

Note

1. G_{UM} is the maximum unilateral power gain, assuming s_{12} is zero. $G_{UM} = 10 \log \frac{\lvert s_{21}\rvert^2}{(1-\lvert s_{11}\rvert^2)(1-\lvert s_{22}\rvert^2)}$ dB

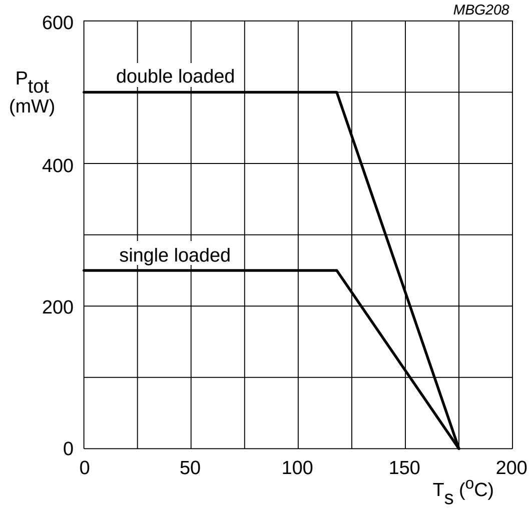
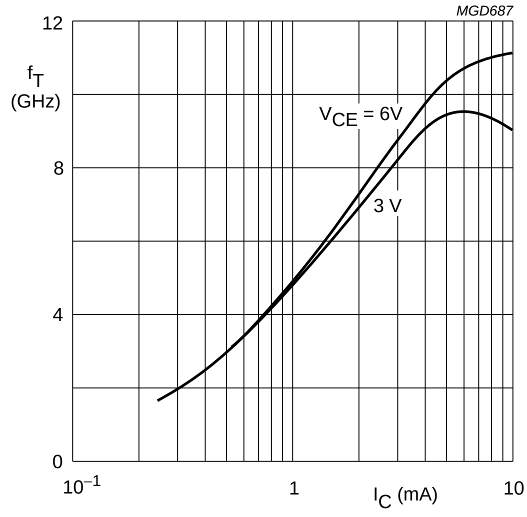
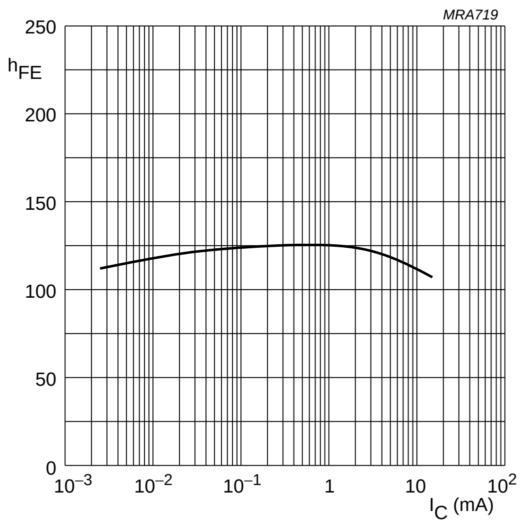


Fig.2 Power derating as a function of soldering point temperature; typical values.



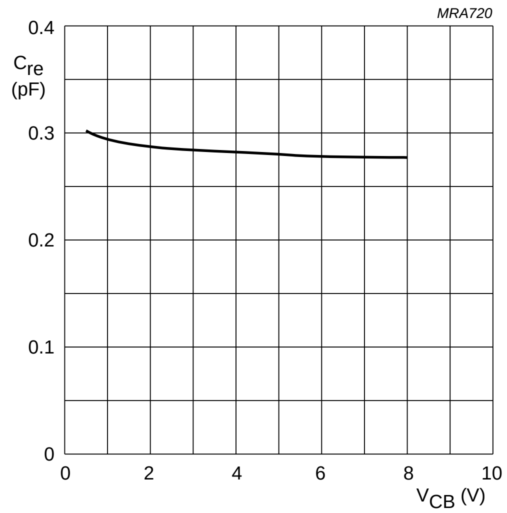
f = 1 GHz; T_{amb} = 25 °C.

Fig.3 Transition frequency as a function of collector current; typical values.



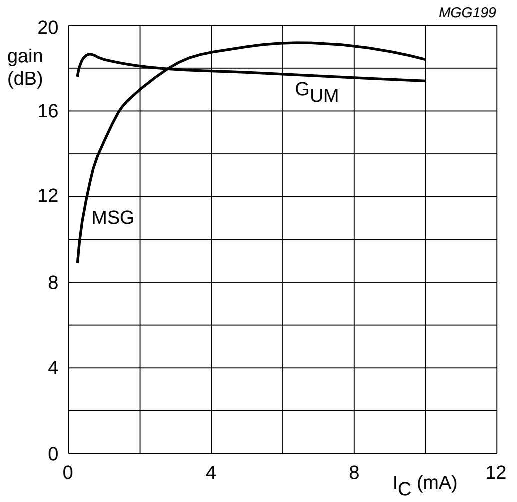
V_{CE} = 6 V.

Fig.4 DC current gain as a function of collector current; typical values.



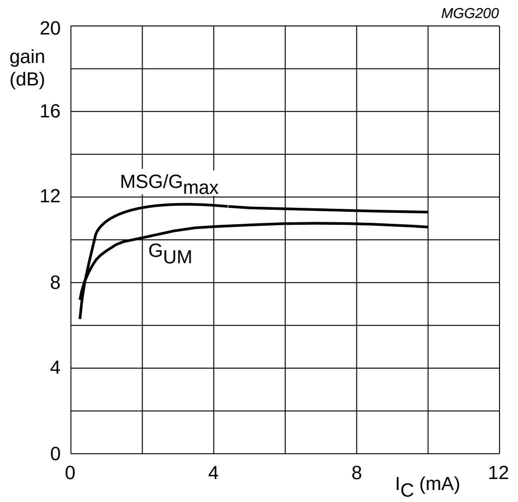
I_C = 0; f = 1 MHz.

Fig.5 Feedback capacitance as a function of collector-base voltage; typical values.



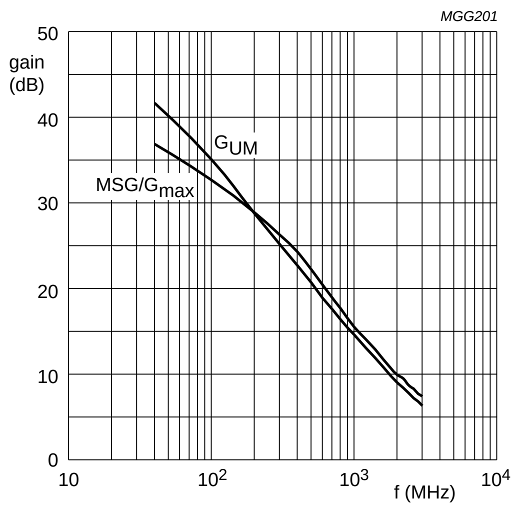
f = 900 MHz; V_{CE} = 3 V.

Fig.6 Gain as a function of collector current; typical values.



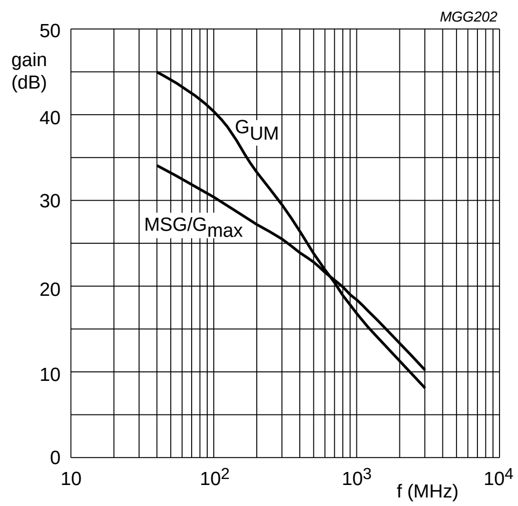
f = 2 GHz; V_{CE} = 3 V.

Fig.7 Gain as a function of collector current; typical values.



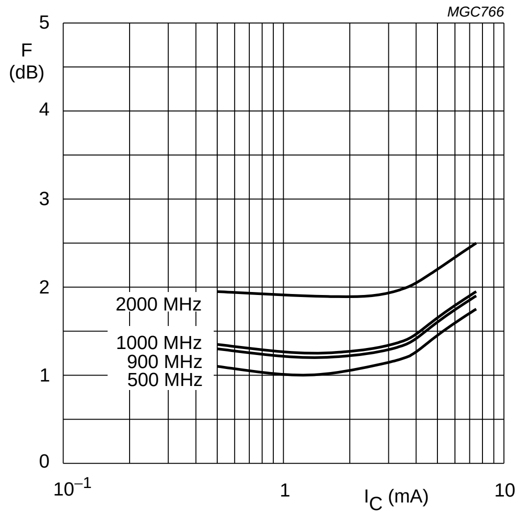
I_C = 1 mA; V_{CE} = 3 V.

Fig.8 Gain as a function of frequency; typical values.



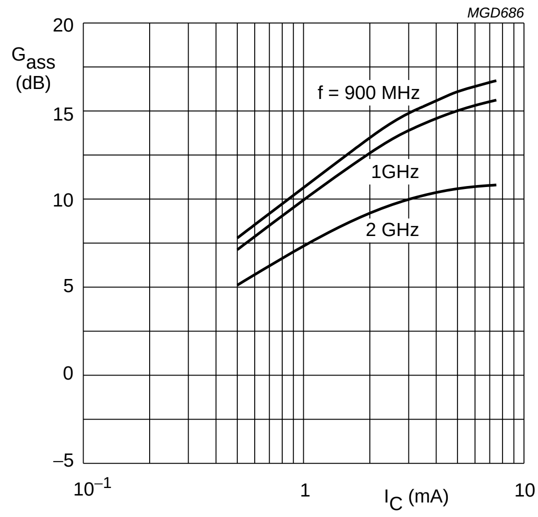
I_C = 5 mA; V_{CE} = 3 V.

Fig.9 Gain as a function of frequency; typical values.



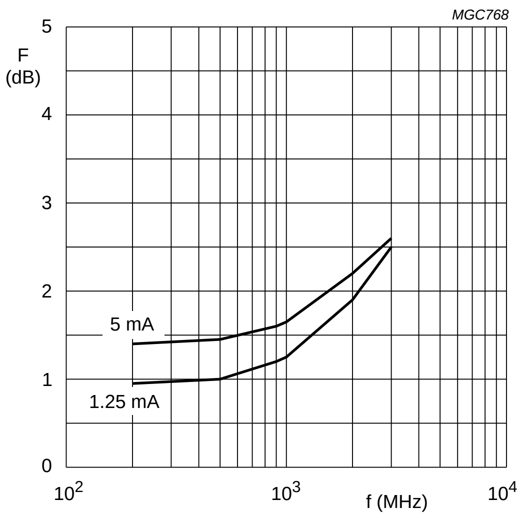
V_{CE} = 3 V.

Fig.10 Minimum noise figure as a function of collector current; typical values.



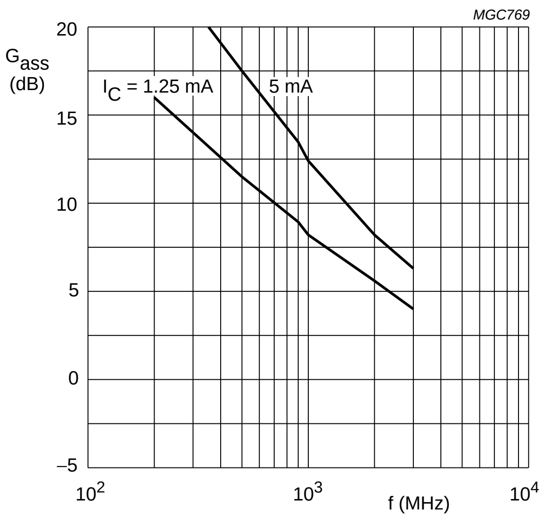
V_{CE} = 3 V.

Fig.11 Associated available gain as a function of collector current; typical values.



V_{CE} = 3 V.

Fig.12 Minimum noise figure as a function of frequency; typical values.



V_{CE} = 3 V.

Fig.13 Associated available gain as a function of frequency; typical values.

APPLICATION INFORMATION

SPICE parameters for any single BFM505 die

SEQUENCE No.	PARAMETER	VALUE	UNIT
1	IS	134.1	aA
2	BF	180.0	–
3	NF	0.988	–
4	VAF	38.34	V
5	IKF	150.0	mA
6	ISE	27.81	fA
7	NE	2.051	–
8	BR	55.19	–
9	NR	0.982	–
10	VAR	2.459	V
11	IKR	2.920	mA
12	ISC	17.45	aA
13	NC	1.062	–
14	RB	20.00	Ω
15	IRB	1.000	μA
16	RBM	20.00	Ω
17	RE	1.171	Ω
18	RC	4.350	Ω
19(1)	XTB	0.000	–
20(1)	EG	1.110	eV
21(1)	XTI	3.000	–
22	CJE	284.7	fF
23	VJE	600.0	mV
24	MJE	0.303	–
25	TF	7.037	ps
26	XTF	12.34	–
27	VTF	1.701	V
28	ITF	30.64	mA
29	PTF	0.000	deg
30	CJC	242.4	fF
31	VJC	188.6	mV
32	MJC	0.041	–
33	XCJC	0.130	–
34	TR	1.332	ns
35(1)	CJS	0.000	F
36(1)	VJS	750.0	mV
37(1)	MJS	0.000	–
38	FC	0.897	–

Note

1. These parameters have not been extracted, the default values are shown.

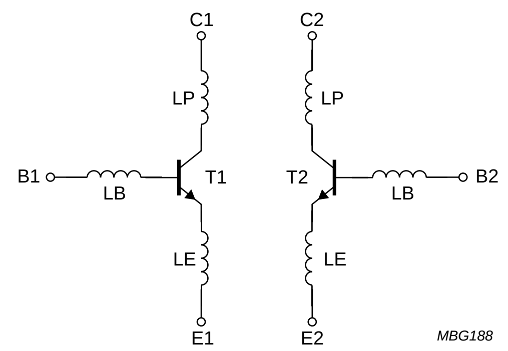


Fig.14 Package equivalent circuit SOT363A (inductance only).

Lead inductances (nH)

LP	0.4
LB	0.6
LE	1.0

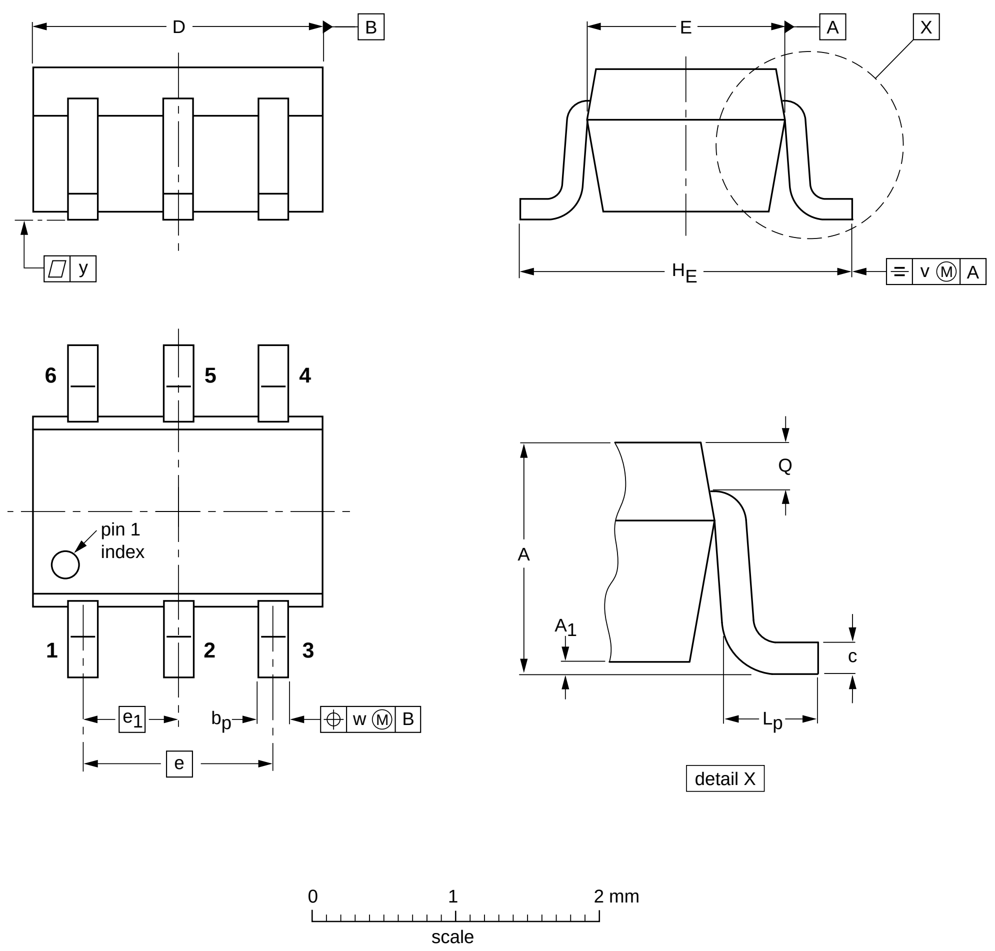
	B1	E2	E1	B2	C2
E2	3				
E1	27	6			
B2	1	27	3		
C2	3	17	36	48	
C1	48	36	17	3	6

MBG189

Fig.15 Package capacitance (fF) between indicated nodes.

PACKAGE OUTLINE

Plastic surface-mounted package; 6 leads **SOT363**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT363			SC-88			~~04-11-08~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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