Revision 1.0.0
ADV Issue Date: 07/10/2020

CUSTOMER ADVISORY

ADV2021

Intel® Stratix® 10 Device Datasheet, User Guides, and Reference Documents Updates

Description:

Intel® is notifying customers of important updates to Intel Stratix® 10 Device Datasheet, User Guides, and other reference documents.

Refer to Table 1 for the list of major updates and Table 2 for further details.

Table 1

Updates	Reference for further details
Clarification of nCONFIG Operation	Table 2; S# 1
Removal of SDMMC Configuration Scheme in Intel Stratix 10 Devices	Table 2; S# 2
Removal of estimated configuration time specification in Intel Stratix 10 Device Datasheet	Table 2; S# 3
Correction of typo error in Intel Stratix 10 Device Datasheet	Table 2; S# 4
Updated bit stream sizes for selected Intel Stratix 10 Devices	Table 2; S# 5
Updated Intel Stratix 10 GX 10M Device specifications	Table 2; S# 6

Table 2

S#	Update Details	Updated Resource Links
1.	**Clarification of nCONFIG Operation:** To ensure error recovery under all circumstances, Intel recommends that you design your system to support power cycling the device if needed. In almost all use cases, asserting nCONFIG will provide adequate error recovery, however, a power cycle may be required in rare instances. A power cycle completely re-initializes the device, samples MSEL, reads the fuses and runs the SDM BootROM code. Device power up and power down sequences must be followed during the power cycle.	• Intel Stratix 10 Device Design Guidelines • Intel Stratix 10 Pin Connection Guidelines • Intel Stratix 10 Configuration User Guide • Intel Stratix 10 HPS Technical Reference Manual
2.	**Removal of SDMMC Configuration Scheme in Intel Stratix 10 Devices:** Intel is removing support for the SD/MMC configuration scheme for Intel Stratix 10 devices. SD/MMC is currently not enabled in the Intel Quartus Prime software for customer use.	• Intel Stratix 10 Device Datasheet • Intel Stratix 10 Device Design Guidelines • Intel Stratix 10 Pin Connection Guidelines • Intel Stratix 10 Configuration User Guide • Intel Stratix 10 HPS Technical Reference Manual • Intel Stratix 10 SoC FPGA Boot User Guide
3.	**Estimated configuration time guidance:** Maximum configuration time estimation in Table 104 and Table 105 in Intel Stratix 10 Device Datasheet has been removed. For guidance on estimated configuration time, refer to section 2.6 of the Intel Stratix 10 Configuration User Guide.	• Intel Stratix 10 Device Datasheet • Intel Stratix 10 Configuration User Guide

<table>
<tr>
<td>4.</td>
<td>Correction of typo error in Intel Stratix 10 Device Datasheet:

Footnote (17) related to HPS_PORSEL in Intel Stratix 10 Device Datasheet has been removed.</td>
<td>• Intel Stratix 10 Device Datasheet</td>
</tr>
<tr>
<td>5.</td>
<td>Updated bit stream sizes for selected Intel Stratix 10 Devices:

Following are the bitstream size updates made in Table 103 in the Intel Stratix 10 Device Datasheet.
<table>
<tr><th rowspan="2">Product Line</th><th colspan="2">Compressed Configuration Bitstream Sizes (Mbits)</th></tr>
<tr><th>Change From</th><th>Change To</th></tr>
<tr><td>GX400, SX400</td><td>127</td><td>79</td></tr>
<tr><td>GX1650, GX2100, SX1650, SX2100</td><td>379</td><td>577</td></tr>
</table>
</td>
<td>• Intel Stratix 10 Device Datasheet</td>
</tr>
<tr>
<td>6.</td>
<td>Updated Intel Stratix 10 GX 10M Device specifications

Intel Stratix 10 GX 10M Device specifications have been added to the Intel Stratix 10 Device Datasheet.</td>
<td>• Intel Stratix 10 Device Datasheet</td>
</tr>
</table>

Recommended Actions:

Customers are requested to review the changes and determine the impact on their designs. Refer to the revision history of the updated documents for a complete list and history of updates.

For questions or support, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

All Intel Stratix 10 Devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2021-opn-list.xlsx

Change Implementation:

Table 3

Milestone	Availability
Availability of Intel Stratix 10 Device datasheet update	Now
Availability of Intel Stratix 10 Device Design Guidelines update	Now
Availability of Intel Stratix 10 Pin Connection Guidelines update	Now
Availability of Intel Stratix 10 Configuration User Guide update	Now
Availability of Intel Stratix 10 HPS Technical Reference Manual update	Now
Availability of Intel Stratix 10 SoC FPGA Boot User Guide	Now

Contact:

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Revision History

Date	Rev	Description
07/10/2020	1.0.0	Initial Release