Noti	ification Number:	20210423004	Notification D	ate:	May 7, 2021	
Title: Datasheet for ADC12DJ3200, ADC08DJ3200, and ADC12DJ2700						
Cus	tomer Contact: Not	ification Manager		Dept:	Quality Serv	ices
Cha	nge Type: Electrical Sp	pecification				
	cription of Change:					
	as Instruments Incorpo			y notifica	tion.	
	product datasheet(s) is					
	following change histor				ADC12D	J3200
				SLVSD97A-	JUNE 2017-REVISED AP	
Ch	anges from Original (June 20	17) to Revision A				Page
•	Changed Pin Functions table I					5
•	Deleted reference to footnote the Power-Down Mode section					7
•	Deleted note underneath the Recommended Operating Conditions table regarding reliable serializer operation. The information has moved to the Power-Down Modes section. 10					
•	Changed <i>Electrical Characteristics - AC Specifications</i> table to include only the Dual-Channel Mode specifications and renamed the table to <i>Electrical Characteristics: AC Specifications (Dual-Channel Mode)</i> . Single-Channel Mode specifications have been split into a separate table for ease of reading			14		
•	Added Electrical Characteristic easier to read				•	17
	Changed figure order in Typical Characteristics section					
	Added FG calibration to conditions of ENOB vs Input Frequency figure					
•	Changed title of HD2, HD3, TH					
•	Added f _{CLK} = 3200 MHz to con	ditions of SNR, SINAD, SFI	DR vs Temperature figur	e		31
•	Added f _{CLK} = 3200 MHz to con	ditions of HD2, HD3, THD v	s Temperature figure			31
•	Changed title of ENOB vs Ten	nperature and Calibration Ty	/pe figure			31
•				31		
•	Added f_{CLK} = 3200 MHz to con	ditions of SNR, SINAD, SF	DR vs Supply Voltage fig	ure		32
•	Added f_{CLK} = 3200 MHz to con	ditions of ENOB vs Supply	Voltage figure			32
•	Added f_{CLK} = 3200 MHz to con					
•	Added f_{CLK} = 3200 MHz to Sup					
		ver Consumption vs Tempe				

•	Changed JMODE2 to JMODE0 in Background Calibration Core Transition (AC Signal) figure	36
•	Changed curve data for Background Calibration Core Transition (AC Signal), Background Calibration Core Transition (AC Signal Zoomed), Background Calibration Core Transition (DC Signal), and Background Calibration	
	Core Transition (DC Signal Zoomed) figures	
•	Changed JMODE2 to JMODE0 in Background Calibration Core Transition (AC Signal Zoomed) figure	
•	Changed product description in Overview section	37
•	Added Device Comparison section.	38
•	Changed location of Analog Reference Voltage section.	40
•	Changed location of Temperature Monitoring Diode section.	42
•	Added requirement for at least 3 rising edges of SYSREF before SYSREF_POS output is valid	45
•	Changed note in Basic NCO Frequency Setting Mode section	50
•	Added sentence describing Common NCO_RDIV Values (For 10-kHz Frequency Steps) table	51
•	Added clarification of NCO synchronization using DC-coupled SYSREF.	51
•	Added clarification of NCO synchronization using AC-coupled SYSREF.	52
•	Changed note in <i>Power-Down Modes</i> section to caution note explaining reliable serializer operation instead of the information being presented under the <i>Recommended Operating Conditions</i> table.	71
•	Changed the Low-Power Background Calibration (LPBG) Mode section to provide additional detail of how to operate the device in low-power background calibration mode.	77
•	Added clarity about offset calibration when both CAL_OS and CAL_BG are enabled.	78
•	Changed <i>Trimming</i> section to limit trimming to foreground (FG) calibration mode only to better reflect customer use cases and simplify the explanation.	79
•	Changed additional clarity to Offset Filtering section to explain the frequency domain impact of the feature	80
•	Changed third sentence of SDI section to include and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address)	81
•	Added ADC12DJ3200 Access Type Codes table	87
•	Changed description of bit 0 in DEVCLK Timing Adjust Ramp Control Register section	129
•	Added Application Information section discussion	. 132
•	Added Reconfigurable Dual-Channel 2.5-GSPS or Single-Channel 5.0-Gsps Oscilloscope section	135
•	Changed Top Layer Routing: Analog Inputs, CLK and SYSREF, DA0-3, DB0-3 to Bottom Layer Routing: Additional CLK Routing, DA4-7, DB4-7 figures	. 142



ADC08DJ3200

SLVSDR1A-FEBRUARY 2018-REVISED APRIL 2020

CI	Changes from Original (February 2018) to Revision A			
•	Changed Pin Functions table listed in alphanumeric order by pin name	4		
•	Changed FFT plots in Typical Characteristics section to show improved look	23		
•	Changed product description in Overview section	33		
•	Changed Device Comparison section to include all devices in the family.	34		
•	Changed location of Analog Reference Voltage section.	36		
•	Changed location of Temperature Monitoring Diode section.	38		
•	Added requirement for at least 3 rising edges of SYSREF before SYSREF_POS output is valid.	40		
•	Changed note in <i>Power-Down Modes</i> section to caution note explaining reliable serializer operation instead of the information being presented under the <i>Pin Functions</i> table.	54		
•	Changed the Low-Power Background Calibration (LPBG) Mode section to provide additional detail of how to operate the device in low-power background calibration mode.	58		
•	Added clarity about offset calibration when both CAL_OS and CAL_BG are enabled.	59		
•	Changed <i>Trimming</i> section to limit trimming to foreground (FG) calibration mode only to better reflect customer use cases and simplify the explanation	60		
•	Changed additional clarity to Offset Filtering section to explain the frequency domain impact of the feature	61		



ADC12DJ2700

SLVSEH9A - JANUARY 2018 - REVISED APRIL 2020

С	hanges from Original (January 2018) to Revision A Pag				
•	Changed Pin Functions table listed in alphanumeric order by pin name	5			
•	Deleted reference to footnote below the Pin Functions table and moved the information to the Power-Down Mode section.	7			
•	Added Operating free-air temperature parameter to Absolute Maximum Ratings table	9			
•	Added Storage temperature parameter to Recommended Operating Conditions table	10			
•	Changed FFT plots in Typical Characteristics section to show improved look	25			
•	Changed product description in Overview section	35			
•	Changed Device Comparison section to include all devices in the family.	36			
•	Changed location of Analog Reference Voltage section.	38			
•	Changed location of Temperature Monitoring Diode section.	40			
•	Added requirement for at least 3 rising edges of SYSREF before SYSREF_POS output is valid.	43			
•	Added clarification of NCO synchronization using DC-coupled SYSREF.	49			
•	Added clarification of NCO synchronization using AC-coupled SYSREF.	50			
•	Changed note in <i>Power-Down Modes</i> section to caution note explaining reliable serializer operation instead of the information being presented under the <i>Pin Functions</i> table.	69			
•	Changed the Low-Power Background Calibration (LPBG) Mode section to provide additional detail of how to operate the device in low-power background calibration mode.	75			
•	Added clarity about offset calibration when both CAL_OS and CAL_BG are enabled.	76			
•	Changed <i>Trimming</i> section to limit trimming to foreground (FG) calibration mode only to better reflect customer use cases and simplify the explanation	77			
•	Changed additional clarity to Offset Filtering section to explain the frequency domain impact of the feature	78			
•	Added ADC12DJ2700 Access Type Codes table	85			
	Added Reconfigurable Dual-Channel 2.5-GSPS or Single-Channel 5.0-Gsps Oscilloscope section	133			
	Changed Top Layer Routing: Analog Inputs, CLK and SYSREF, DA0-3, DB0-3 to Bottom Layer Routing: Additional CLK Routing, DA4-7, DB4-7 figures	140			

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADC12DJ3200	SLVSD97	SLVSD97A
ADC08DJ3200	SLVSDR1	SLVSDR1A
ADC12DJ2700	SLVSEH9	SLVSEH9A

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/ADC12DJ3200 http://www.ti.com/product/ADC08DJ3200 http://www.ti.com/product/ADC12DJ2700

Reason for Change:

To accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this notification:

None.

Product Affected:						
AD	C12DJ3200AAV	ADC12DJ3200AAVT	ADC12DJ3200ZEG	ADC12DJ3200ZEGT		
AD	C08DJ3200AAV	ADC08DJ3200AAVT	ADC12DJ2700AAV	ADC12DJ2700AAV		
AD	C12DJ2700ZEG	ADC12DJ2700ZEGT				

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