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Team Nexperia

Product data sheet

Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed USB, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in a leadless small DFN2510A-10 (SOT1176-1) plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.5 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to $\pm 10~\text{kV}$ contact exceeding IEC 61000-4-2, level 4.

1.2 Features and benefits

- System ESD protection for USB 2.0 and SuperSpeed USB 3.0, HDMI, DisplayPort, eSATA and LVDS
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.5 pF for each channel
- Design-friendly 'pass-through' signal routing

1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles



2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	10 0 0 7 0	4 0 4 5
2	CH2	channel 2 ESD protection	10 9 8 7 6	1 2 4 5
3	GND	ground		
4	CH3	channel 3 ESD protection	1 2 3 4 5	나 나 本 난 난
5	CH4	channel 4 ESD protection	Transparent top view	本本 本本
6	n.c.	not connected		3, 8 , 42 , 224
7	n.c.	not connected		0, 018aaa001
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4294CZ10-TBR	DFN2510A-10	plastic extremely thin small outline package; no leads; 10 terminals; body $1 \times 2.5 \times 0.5$ mm	SOT1176-1

4. Marking

Table 3. Marking codes

Type number	Marking code
IP4294CZ10-TBR	94

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{I}	input voltage		-0.5	+5.5	V
V _{ESD}	electrostatic discharge	IEC 61000-4-2, level 4	<u>[1]</u>		
	voltage	contact discharge	-10	+10	kV
		air discharge	-15	+15	kV
T _{amb}	ambient temperature		-40	+85	°C
T _{stg}	storage temperature		-55	+125	°C

^[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

 $T_{amb} = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{BR}	breakdown voltage	$I_I = 1 \text{ mA}$	6	-	-	V
I _{LR}	reverse leakage current	per channel; V _I = 3 V	-	-	1	μΑ
V_{F}	forward voltage	$I_I = 1 \text{ mA}$	-	0.7	-	V
C _{line}	line capacitance	$f = 1 \text{ MHz}; V_1 = 3.3 \text{ V}$	<u>[1]</u> -	0.5	0.6	pF
ΔC_{line}	line capacitance difference	$f = 1 \text{ MHz}; V_1 = 3.3 \text{ V}$	<u>[1]</u> -	0.05	-	pF
r _{dyn}	dynamic resistance	surge	[2]			
		positive transient	-	0.36	-	Ω
		negative transient	-	0.35	-	Ω
		TLP	[3]			
		positive transient	-	0.41	-	Ω
		negative transient	-	0.34	-	Ω
V_{CL}	clamping voltage	I _{PP} = 4 A	[2]			
		positive transient	-	4.1	-	V
		$I_{PP} = -4 A$	[2]			
		negative transient	-	-2.2	-	V

^[1] This parameter is guaranteed by design.

^[2] According to IEC 61000-4-5 (8/20 μs current waveform).

^{[3] 100} ns Transmission Line Pulse (TLP); 50 Ω ; pulser at 80 ns.

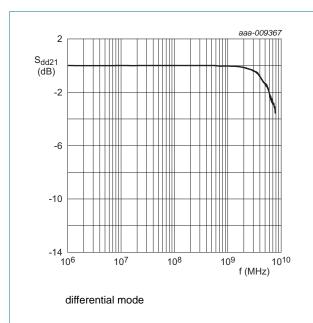
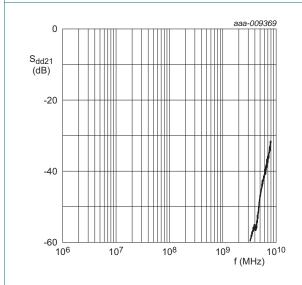
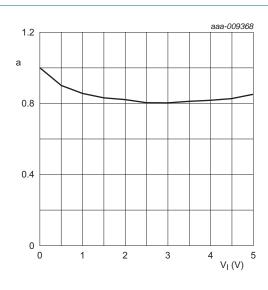


Fig 1. Insertion loss; typical values



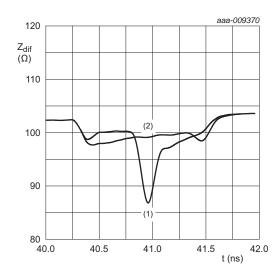
Sdd21 normalized to 100 $\Omega;$ differential pairs CH1/CH2 versus CH3/CH4

Fig 3. Crosstalk; typical values



$$a = \frac{C_{line}}{C_{line(V_I = 0 \text{ V})}}$$

Fig 2. Relative capacitance as a function of input voltage; typical values

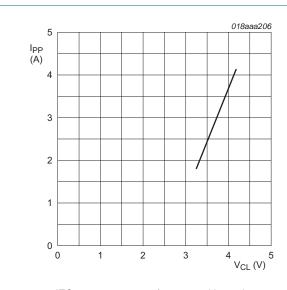


t_r = 200 ps; differential pair CH1 + CH2

- (1) IP4294CZ10-TBR on reference board
- (2) Reference board without device under test (DUT)

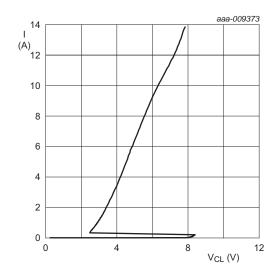
Fig 4. Differential Time Domain Reflectometer (TDR) plot; typical values

4 of 12



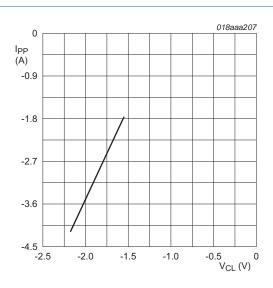
IEC 61000-4-5; $t_p = 8/20 \mu s$; positive pulse

Fig 5. Dynamic resistance with positive clamping; typical values



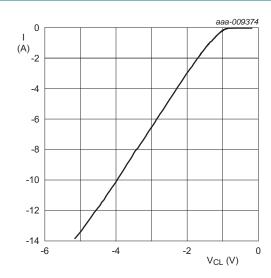
t_o = 100 ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with positive clamping; typical values



IEC 61000-4-5; $t_p = 8/20 \mu s$; negative pulse

Fig 6. Dynamic resistance with negative clamping; typical values



 t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 8. Dynamic resistance with negative clamping; typical values

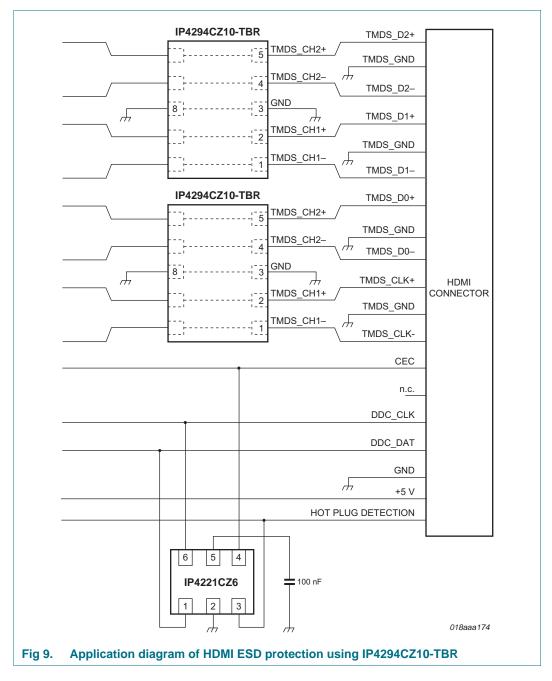
The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

A basic application diagram for the ESD protection of an HDMI interface is shown in Figure 9.



Package outline 8.

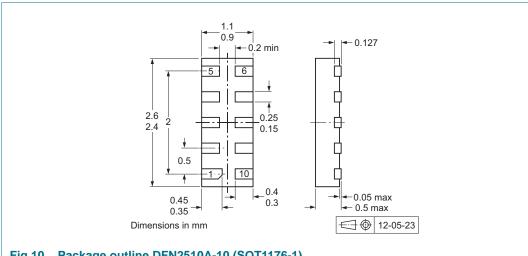
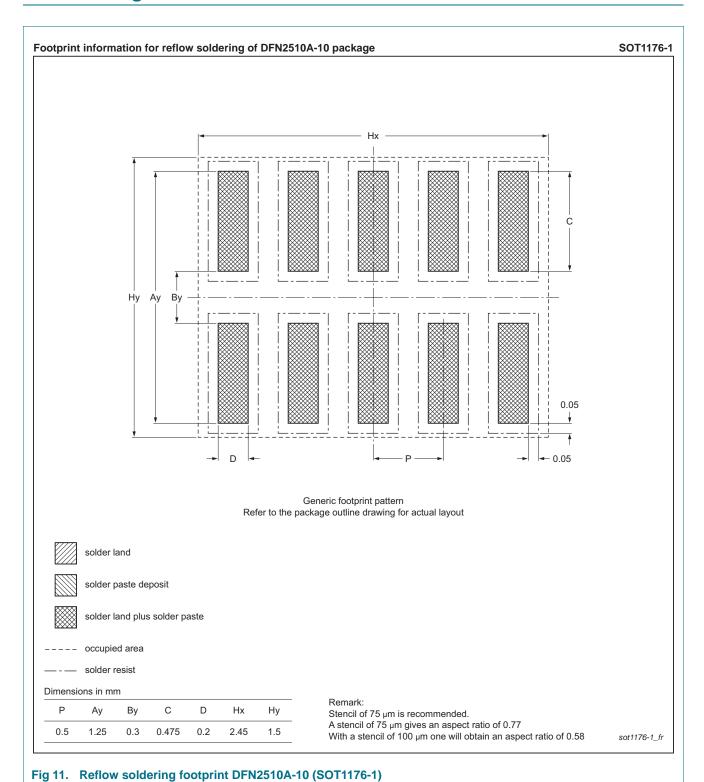


Fig 10. Package outline DFN2510A-10 (SOT1176-1)

7 of 12

Soldering



IP4294CZ10-TBR



10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4294CZ10-TBR v.4	20131101	Product data sheet	-	IP4294CZ10-TBR v.3
Modifications:	 Measureme 	nts updated after silicon man	ufacturing transfer.	
IP4294CZ10-TBR v.3	20120224	Product data sheet	-	IP4294CZ10-TBR v.2
IP4294CZ10-TBR v.2	20120229	Preliminary data sheet	-	IP4294CZ10-TBR v.1
IP4294CZ10-TBR v.1	20111125	Preliminary data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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IP4294CZ10-TBR

ESD protection for ultra high-speed interfaces

13. Contents

1	Product profile
1.1	General description
1.2	Features and benefits
1.3	Applications
2	Pinning information 2
3	Ordering information 2
4	Marking 2
5	Limiting values
6	Characteristics 3
7	Application information 6
8	Package outline
9	Soldering 8
10	Revision history9
11	Legal information
11.1	Data sheet status
11.2	Definitions
11.3	Disclaimers
11.4	Trademarks11
12	Contact information
13	Contents

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