# **PEB1757E** TETHYS™ 2 STS-192/STM-64, 16 STS-48/STM-16, MUX/DEMUX

Powering Connectivity

## **GENERAL DESCRIPTION**

Tethys<sup>™</sup> PEB1757E is optimized for SONET/SDH applications as a full-duplex two STS-192/STM64 or sixteen STS-48/STM-16 or a mix of sixteen STS-12/ STM-4 and STS-3/STM-1 MUX/DEMUX channel device with full framer functionality including pointer processing, and overhead termination; ideal for aggregation, ADM and DWDM applications. In the demultiplex ingress direction, Tethys™ PEB1757E accepts either two STS-192/STM-64 or sixteen STS-48/ STM-16, or a mix of sixteen STS-12/STM-4 and STS-3/ STM-1 signals in serial 2.5 Gbit/s or serial 622 Mbit/s or serial 155 Mbit/s format. Tethys™ PEB1757E locates the incoming SONET/SDH frame, optionally de-scrambles the data, monitors the TOH and POH, and provides STS-1 level pointer processing. In addition, Tethys™ PEB1757E supports TOH and POH overhead transparency.

In the multiplex direction, Tethys<sup>™</sup> PEB1757E accepts sixteen STS-48/STM-16 signals in serial 2.5 Gbit/s format. Tethys<sup>™</sup> PEB1757E further provides corresponding functionality in the DEMUX direction.

### APPLICATIONS

- ADM
- Metro Aggregation
- Digital Cross Connects
- Repeaters
- DWDM Equipment
- Test Equipment

#### FEATURES

- Provides 2 SFI4.1 interfaces for STS-192/STM-64 links
- Provides serial STS-48/STM-16, STS-12/STM-4 or STS-3/STM-1 links
- Differential CML 2.5 Gbit/s I/O interface to optics
- Differential CML 2.5 Gbit/s I/O interface to system/ backplane
- TFI-5 Support
- Processes SONET/SDH sixteen STS-48/STM-16 or a mix of sixteen STM-12/STM-4 and STS-3/STM-1 on the line side interface
- Processes SONET/SDH sixteen STS-48/STM-16 on the system/client side serial 2.5 Gbit/s interface

- · Provides line timing of all line and system side interfaces
- Processes SONET/SDH flexible concatenation streams of STS-2c, 3c, 4c, ... to 192c
- Supports auto-detection of concatenation streams STS-3c/STM-1, STS-12c/STM-4 and STS-48c/STM-16
- Supports STS-1 level pointer processing of STS-48/STM-16 or STM-12/STM-4 or STS-3/STM-1 streams
- Provides interfaces for dropping alarm and status information, and for forcing alarm conditions
- Power dissipation of 15 W, depending on mode of operation
- Terminates and generates SONET section, line, and path layers
- Provides TOH and POH transparency
- Provides monitoring of POH bytes B3 and N1/Z5
- Provides B2 SF/SD capability for Poisson and bursty error distribution
- Provides full TOH/POH add/drop
- Provides STS-1 level POH add/drop
- Supports more than ± 746 UI programmable output skew on STS48/STM-16 system side output links to external cross-connects
- For diagnostic purposes, Tethys provides PRBS generator/checker and loop backs
- Provides B1, B2, H1 and H2 bit error generation for both receive and transmit direction diagnostics
- Provides 1 second performance monitors
- 0.13 micron process, 1.2 V core, 3.3 V I/O
- Motorola 32-bit synchronous microprocessor interface for configuration, control, and status monitoring
- Complies with GR-253, GR-1377, ITU-T G.707, and ANSI T1.105
- Provides a standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes

#### SPECIFICATIONS

• OIF TFI-5

#### STANDARDS

- ANSI T1.105-2000-193R2 (DRAFT)
- ANSI T1.105.05-1994
- T1X1.3/93-005RI -1993 preliminary
- GR-253-CORE Sept. 2000

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
PEB1757E	1397 CBGA	-40°C to +85°C

## PEB1757E

# Powering Connectivity REV. 1.0.2

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#### FIGURE 1. PEB1757E BLOCK DIAGRAM IN STS-48 APPLICATION

