# BF1100; BF1100R

### **Dual-gate MOS-FETs**

Rev. 02 — 13 November 2007

**Product data sheet** 

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**NXP Semiconductors** 



### **Dual-gate MOS-FETs**

BF1100; BF1100R

#### **FEATURES**

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

#### **APPLICATIONS**

 VHF and UHF applications such as television tuners and professional communications equipment.

#### **DESCRIPTION**

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source

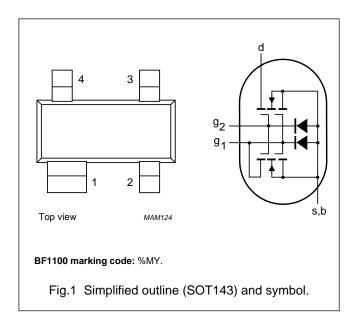
and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

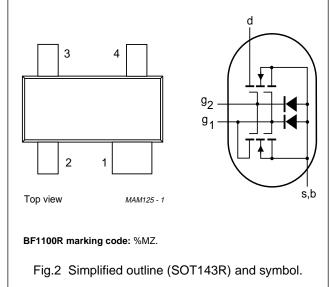
### **CAUTION**

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

#### **PINNING**

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	<b>g</b> <sub>2</sub>	gate 2
4	<b>g</b> 1	gate 1





**QUICK REFERENCE DATA** 

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		_	_	14	V
I <sub>D</sub>	drain current		_	_	30	mA
P <sub>tot</sub>	total power dissipation		_	_	200	mW
Tj	operating junction temperature		_	_	150	°C
y <sub>fs</sub>	forward transfer admittance		24	28	33	mS
C <sub>ig1-s</sub>	input capacitance at gate 1		_	2.2	2.6	pF
C <sub>rs</sub>	reverse transfer capacitance	f = 1 MHz	_	25	35	fF
F	noise figure	f = 800 MHz	_	2	_	dB

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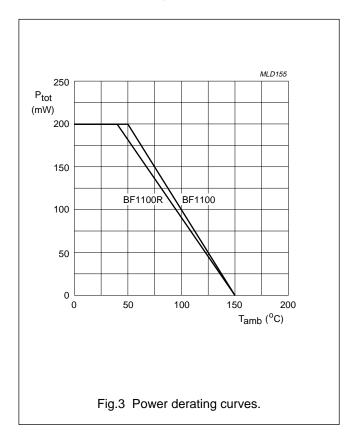
### **LIMITING VALUES**

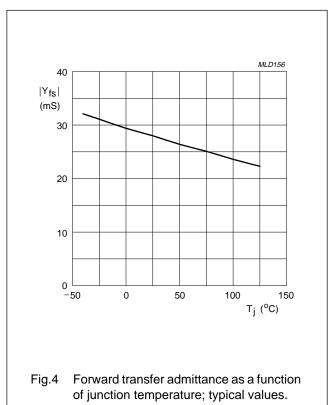
In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>DS</sub>	drain-source voltage		_	14	V
I <sub>D</sub>	drain current		_	30	mA
I <sub>G1</sub>	gate 1 current		_	±10	mA
$I_{G2}$	gate 2 current		_	±10	mA
P <sub>tot</sub>	total power dissipation	see Fig.3			
	BF1100	up to $T_{amb} = 50 ^{\circ}C$ ; note 1	_	200	mW
	BF1100R	up to $T_{amb} = 40 ^{\circ}C$ ; note 1	_	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	operating junction temperature		_	+150	°C

#### Note

1. Device mounted on a printed-circuit board.





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### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th j-a</sub>	thermal resistance from junction to ambient	note 1		
	BF1100		500	K/W
	BF1100R		550	K/W
R <sub>th j-s</sub>	thermal resistance from junction to soldering point	note 2		
	BF1100	T <sub>s</sub> = 92 °C	290	K/W
	BF1100R	T <sub>s</sub> = 78 °C	360	K/W

### Notes

- 1. Device mounted on a printed-circuit board.
- 2.  $T_s$  is the temperature at the soldering point of the source lead.

### STATIC CHARACTERISTICS

 $T_i = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>(BR)G1-SS</sub>	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{G1-S} = 1 \text{ mA}$	13.2	20	V
V <sub>(BR)G2-SS</sub>	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{G2-S} = 1 \text{ mA}$	13.2	20	V
V <sub>(F)S-G1</sub>	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{S-G1} = 10 \text{ mA}$	0.5	1.5	V
V <sub>(F)S-G2</sub>	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{S-G2} = 10 \text{ mA}$	0.5	1.5	V
V <sub>G1-S(th)</sub>	gate 1-source threshold voltage	$V_{G2-S} = 4 \text{ V}; V_{DS} = 9 \text{ V};$ $I_D = 20 \mu A$	0.3	1	V
		$V_{G2-S} = 4 \text{ V}; V_{DS} = 12 \text{ V};$ $I_D = 20 \mu\text{A}$	0.3	1	V
V <sub>G2-S(th)</sub>	gate 2-source threshold voltage	$V_{G1-S} = 4 \text{ V}; V_{DS} = 9 \text{ V};$ $I_D = 20 \mu\text{A}$	0.3	1.2	V
		$V_{G1-S} = 4 \text{ V}; V_{DS} = 12 \text{ V};$ $I_D = 20 \mu\text{A}$	0.3	1.2	V
I <sub>DSX</sub>	drain-source current	$V_{G2-S} = 4 \text{ V}; V_{DS} = 9 \text{ V};$ $R_{G1} = 180 \text{ k}\Omega; \text{ note 1}$	8	13	mA
		$V_{G2-S} = 4 \text{ V}; V_{DS} = 12 \text{ V};$ $R_{G1} = 250 \text{ k}\Omega; \text{ note } 2$	8	13	mA
I <sub>G1-SS</sub>	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0; V_{G1-S} = 12 \text{ V}$	_	50	nA
I <sub>G2-SS</sub>	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0; V_{G2-S} = 12 \text{ V}$	_	50	nA

### Notes

- 1.  $R_{G1}$  connects gate 1 to  $V_{GG}$  = 9 V; see Fig.27.
- 2.  $R_{G1}$  connects gate 1 to  $V_{GG}$  = 12 V; see Fig.27.

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### **DYNAMIC CHARACTERISTICS**

Common source;  $T_{amb}$  = 25 °C;  $V_{G2-S}$  = 4 V;  $I_D$  = 10 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
y <sub>fs</sub>	forward transfer admittance	pulsed; T <sub>j</sub> = 25 °C				
		V <sub>DS</sub> = 9 V	24	28	33	mS
		V <sub>DS</sub> = 12 V	24	28	33	mS
C <sub>ig1-s</sub>	input capacitance at gate 1	f = 1 MHz				
		V <sub>DS</sub> = 9 V	_	2.2	2.6	pF
		V <sub>DS</sub> = 12 V	_	2.2	2.6	pF
C <sub>ig2-s</sub>	input capacitance at gate 2	f = 1 MHz				
		V <sub>DS</sub> = 9 V	_	1.6	_	pF
		V <sub>DS</sub> = 12 V	_	1.4	_	pF
Cos	drain-source capacitance	f = 1 MHz				
		V <sub>DS</sub> = 9 V	_	1.4	1.8	pF
		V <sub>DS</sub> = 12 V	_	1.1	1.5	pF
C <sub>rs</sub>	reverse transfer capacitance	f = 1 MHz				
		V <sub>DS</sub> = 9 V	_	25	35	fF
		V <sub>DS</sub> = 12 V	_	25	35	fF
F	noise figure	$f = 800 \text{ MHz}$ ; $G_S = G_{Sopt}$ ; $B_S = B_{Sopt}$				
		V <sub>DS</sub> = 9 V	_	2	2.8	dB
		V <sub>DS</sub> = 12 V	_	2	2.8	dB

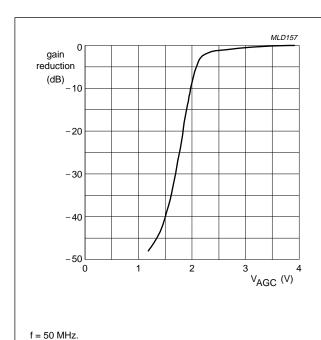
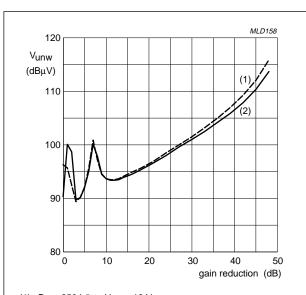


Fig.5 Gain reduction as a function of the AGC voltage; typical values.

 $T_j = 25 \, ^{\circ}C$ .



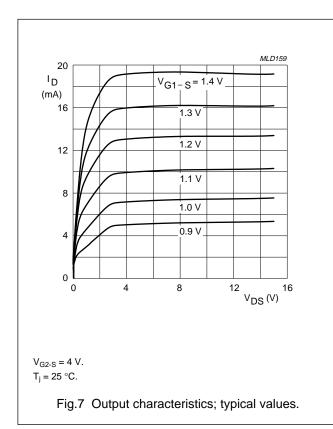
- (1)  $R_G$  = 250  $k\Omega$  to  $V_{GG}$  = 12 V
- (2)  $R_G = 180 \text{ k}\Omega \text{ to } V_{GG} = 9 \text{ V}$

 $f_w$  = 50 MHz;  $f_{unw}$  = 60 MHz;  $T_{amb}$  = 25 °C.

Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.27.

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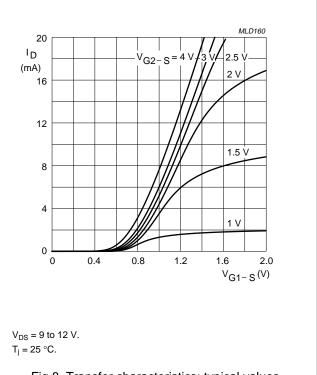
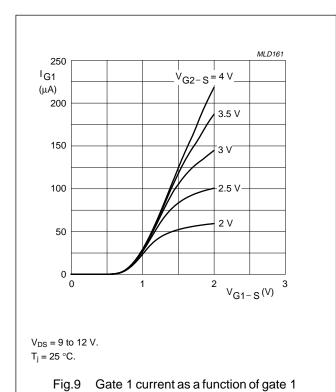
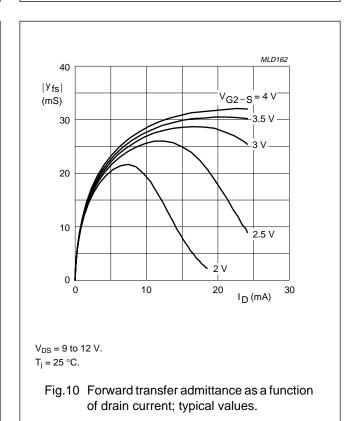


Fig.8 Transfer characteristics; typical values.

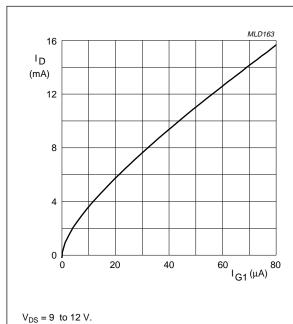


voltage; typical values.



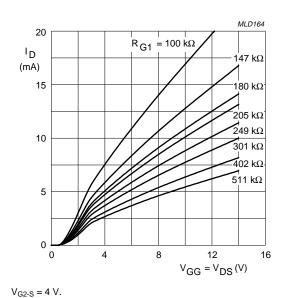
### **Dual-gate MOS-FETs**

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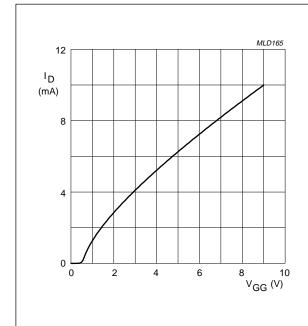
 $V_{G2-S} = 4 \text{ V}.$   $T_i = 25 \text{ °C}.$ 

Fig.11 Drain current as a function of gate 1 current; typical values.



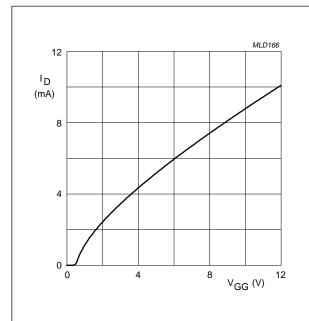
 $V_{G2-S} = 4 \text{ V}.$   $R_{G1}$  connected to  $V_{GG}.$   $T_j = 25 \text{ °C}.$ 

Fig.12 Drain current as a function of gate 1 supply voltage (=  $V_{GG}$ ) and drain supply voltage; typical values; see Fig.27.



 $V_{DS} = 9 \text{ V; } V_{G2\text{-}S} = 4 \text{ V.}$   $R_{G1} = 180 \text{ k}\Omega \text{ (connected to } V_{GG}); T_j = 25 \text{ °C.}$ 

Fig.13 Drain current as a function of gate 1 voltage (= V<sub>GG</sub>); typical values; see Fig.27.



 $V_{DS} = 12 \text{ V; } V_{G2\text{-}S} = 4 \text{ V.}$   $R_{G1} = 250 \text{ k}\Omega \text{ (connected to } V_{GG}); T_j = 25 \text{ °C.}$ 

Fig.14 Drain current as a function of gate 1 voltage;  $(= V_{GG})$ ; typical values; see Fig.27.

### **Dual-gate MOS-FETs**

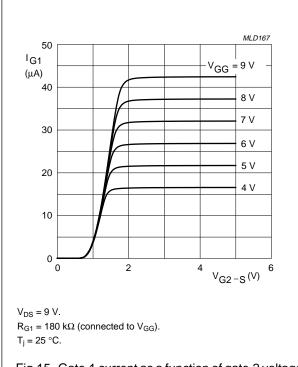


Fig.15 Gate 1 current as a function of gate 2 voltage; typical values.

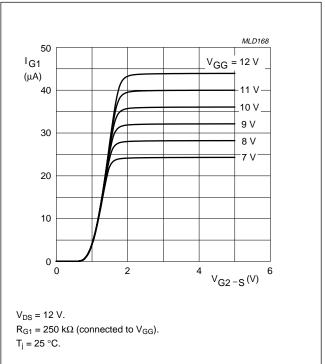
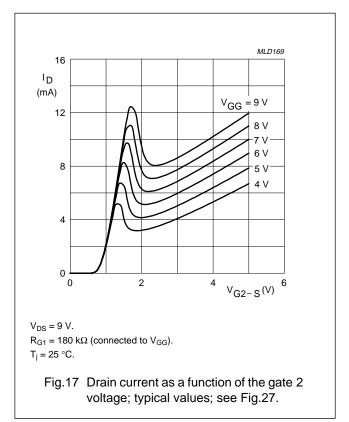
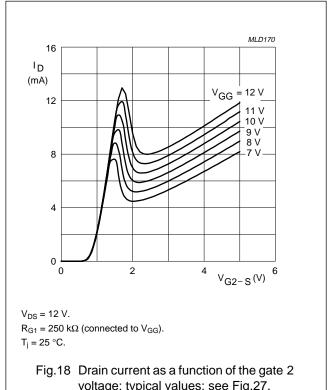


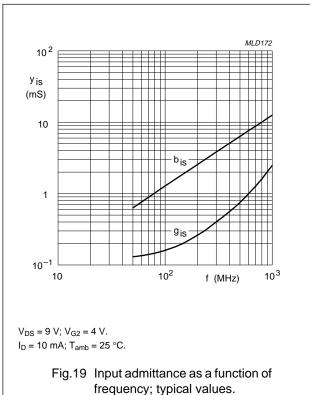
Fig.16 Gate 1 current as a function of gate 2 voltage; typical values.

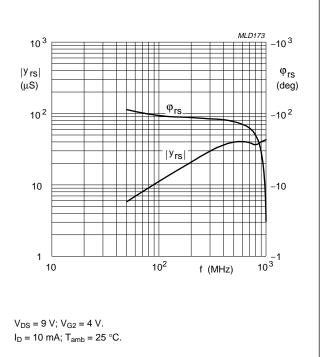




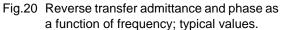
voltage; typical values; see Fig.27.

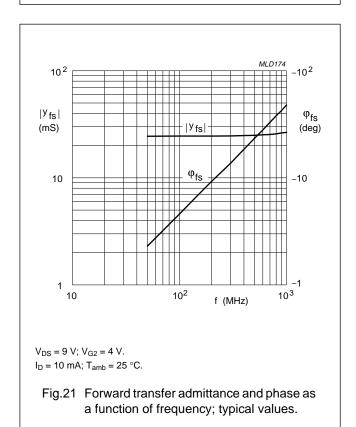
### **Dual-gate MOS-FETs**

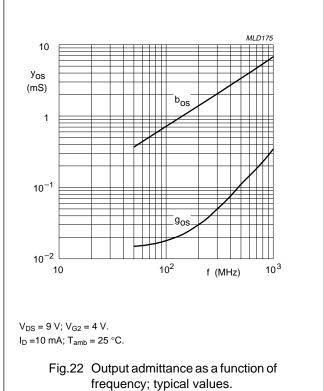




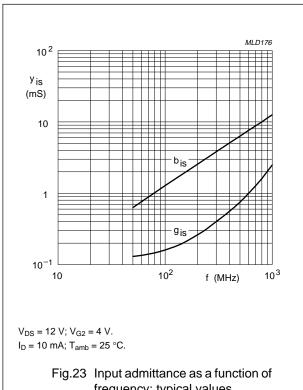
frequency; typical values.





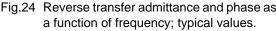


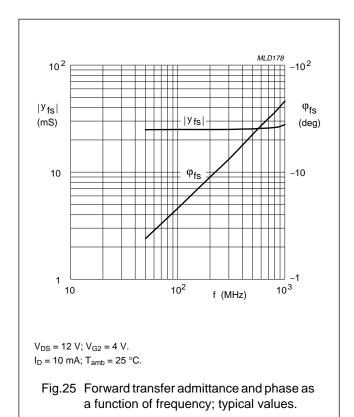
### **Dual-gate MOS-FETs**

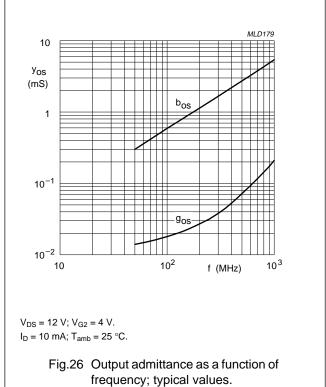


-10<sup>3</sup> 10<sup>3</sup>  $\phi_{\text{rs}}$  $|y_{rs}|$ (μS) (deg) -10<sup>2</sup> 10<sup>2</sup> 10 10<sup>3</sup> 10<sup>2</sup> 10 f (MHz)  $V_{DS} = 12 \text{ V}; V_{G2} = 4 \text{ V}.$  $I_D$  = 10 mA;  $T_{amb}$  = 25 °C. Fig.24 Reverse transfer admittance and phase as

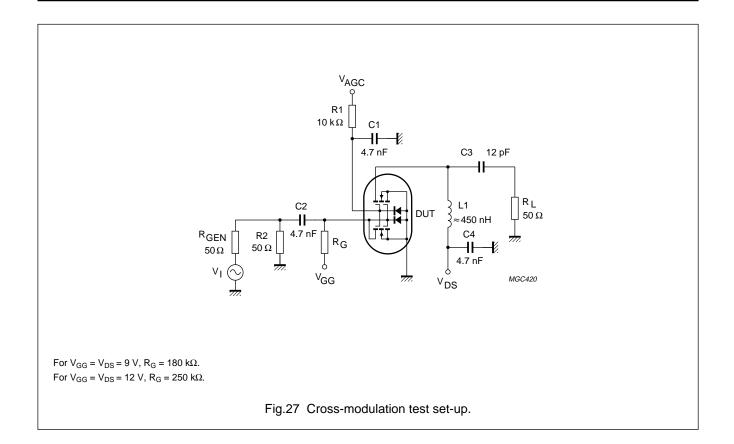
frequency; typical values.







# **Dual-gate MOS-FETs**



### **Dual-gate MOS-FETs**

**Table 1** Scattering parameters:  $V_{DS} = 9 \text{ V}$ ;  $V_{G2-S} = 4 \text{ V}$ ;  $I_D = 10 \text{ mA}$ 

f	S <sub>11</sub>	S <sub>11</sub>		s <sub>21</sub>			S <sub>22</sub>	
(MHz)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	-3.6	2.528	174.4	0.001	63.7	1.000	-2.0
100	0.983	-7.4	2.531	169.8	0.001	80.7	1.000	-4.2
200	0.974	-14.7	2.490	159.5	0.002	81.0	0.996	-8.1
300	0.960	-21.8	2.446	149.8	0.002	80.3	0.994	-11.9
400	0.953	-28.7	2.412	139.8	0.003	76.3	0.992	-15.7
500	0.933	-35.4	2.341	130.1	0.003	76.5	0.987	-19.4
600	0.915	-42.0	2.283	120.4	0.004	79.0	0.984	-23.0
700	0.895	-47.9	2.205	111.6	0.003	81.5	0.981	-26.7
800	0.880	-53.5	2.146	102.9	0.003	90.8	0.978	-30.3
900	0.864	-59.6	2.087	93.4	0.003	106.6	0.974	-33.9
1000	0.839	-65.0	1.998	84.4	0.003	135.4	0.971	-37.6

**Table 2** Noise data:  $V_{DS} = 9 \text{ V}$ ;  $V_{G2-S} = 4 \text{ V}$ ;  $I_D = 10 \text{ mA}$ 

f	F <sub>min</sub>	$\Gamma_{opt}$		
(MHz)	(dB)	(ratio)	(deg)	'n
800	2.00	0.67	43.9	0.89

**Table 3** Scattering parameters:  $V_{DS} = 12 \text{ V}$ ;  $V_{G2-S} = 4 \text{ V}$ ;  $I_D = 10 \text{ mA}$ 

	S <sub>11</sub>		S <sub>21</sub> S <sub>12</sub> S <sub>22</sub>		S <sub>21</sub> S <sub>12</sub>			
(MHz)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.986	-3.7	2.478	174.7	0.001	72.2	1.000	-1.6
100	0.984	-7.4	2.480	170.3	0.001	80.9	1.000	-3.5
200	0.974	-14.6	2.440	160.6	0.002	82.7	0.997	-6.6
300	0.960	-21.8	2.400	151.4	0.002	79.9	0.996	-9.7
400	0.953	-28.7	2.371	141.9	0.003	77.7	0.994	-12.8
500	0.933	-35.3	2.306	132.7	0.003	77.1	0.991	-15.8
600	0.915	-41.9	2.255	123.6	0.004	77.1	0.989	-18.7
700	0.894	-47.8	2.183	115.3	0.004	79.3	0.986	-21.7
800	0.879	-53.5	2.131	107.2	0.003	83.9	0.984	-24.6
900	0.863	-59.5	2.080	98.2	0.003	95.1	0.982	-27.5
1000	0.838	-65.0	1.999	89.7	0.003	115.8	0.980	-30.4

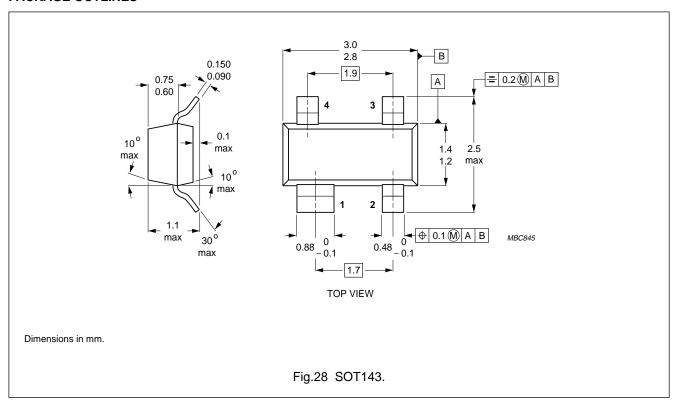
**Table 4** Noise data:  $V_{DS} = 12 \text{ V}$ ;  $V_{G2-S} = 4 \text{ V}$ ;  $I_D = 10 \text{ mA}$ 

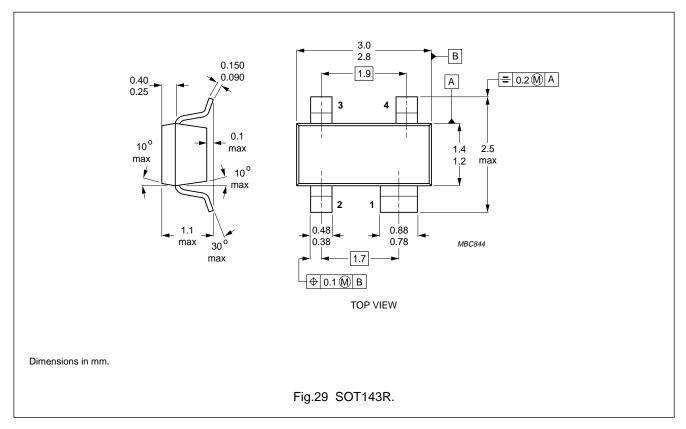
f	F <sub>min</sub>	$\Gamma_{opt}$		
(MHz)	(dB)	(ratio)	(deg)	'n
800	2.00	0.66	43.3	0.97

# **Dual-gate MOS-FETs**

BF1100; BF1100R

### **PACKAGE OUTLINES**





**Dual-gate MOS-FETs** 

### **Legal information**

### **Data sheet status**

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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**Dual-gate MOS-FETs** 

# **Revision history**

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Document ID	Release date	Data sheet status	Change notice	Supersedes		
BF1100_N_2	20071113	Product data sheet	-	BF1100_1		
Modifications: • Fig. 1 and 2 on page 2; Figure note changed						
BF1100_1	19950425	Product specification	-	-		

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