



## FCPF11N65

### N-Channel SuperFET® MOSFET

650 V, 11 A, 380 mΩ

February 2015

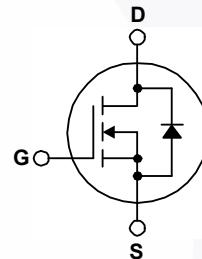
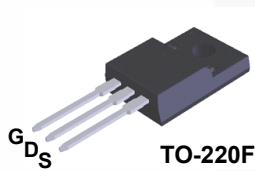


#### Features

- Typ.  $R_{DS(on)}$  = 320 mΩ
- Ultra Low Gate Charge (Typ.  $Q_g$  = 40 nC)
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)}$  = 95 pF)
- 100% Avalanche Tested

#### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



#### Absolute Maximum Ratings

Symbol	Parameter	FCPF11N65	Unit
$V_{DSS}$	Drain-Source Voltage	650	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	11* 7*	A A
$I_{DM}$	Drain Current - Pulsed	(Note 1)	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$I_{AR}$	Avalanche Current	(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate Above $25^\circ\text{C}$	36 0.29	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature.

#### Thermal Characteristics

Symbol	Parameter	FCPF11N65	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF11N65	FCPF11N65	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

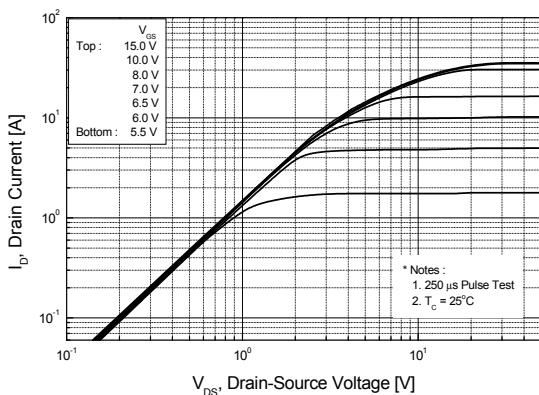
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 25^\circ\text{C}$	650	--	--	V
		$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}, T_J = 150^\circ\text{C}$	--	700	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	$^\circ\text{C}$
$BV_{DS}$	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 11 \text{ A}$	--	700	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 480 \text{ V}, T_C = 125^\circ\text{C}$	--	--	1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	3.0	--	5.0	V
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 5.5 \text{ A}$	--	0.32	0.38	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 5.5 \text{ A}$	--	9.7	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	--	1148	1490	pF
$C_{oss}$	Output Capacitance		--	671	870	pF
$C_{rss}$	Reverse Transfer Capacitance		--	63	--	pF
$C_{oss}$	Output Capacitance		--	35	--	pF
$C_{oss(\text{eff.})}$	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 400 \text{ V}, V_{GS} = 0 \text{ V}$	--	95	--	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300 \text{ V}, I_D = 11 \text{ A}, R_G = 25 \Omega$	--	34	80	ns
$t_r$	Turn-On Rise Time		--	98	205	ns
$t_{d(off)}$	Turn-Off Delay Time		--	119	250	ns
$t_f$	Turn-Off Fall Time		--	56	120	ns
$Q_g$	Total Gate Charge	$V_{DS} = 480 \text{ V}, I_D = 11 \text{ A}, V_{GS} = 10 \text{ V}$	--	40	52	nC
$Q_{gs}$	Gate-Source Charge		--	7.2	--	nC
$Q_{gd}$	Gate-Drain Charge		--	21	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	11	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	33	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 11 \text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = 11 \text{ A}$ $dI_F/dt = 100 \text{ A}/\mu\text{s}$	--	390	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	5.7	--	$\mu\text{C}$

### Notes:

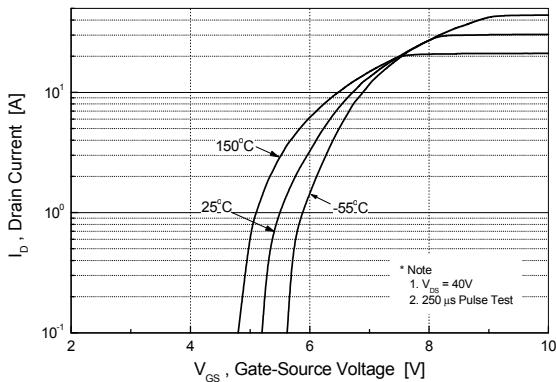
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 5.5 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 11 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

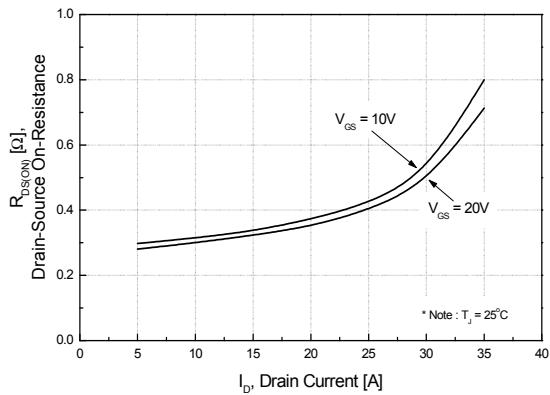
**Figure 1. On-Region Characteristics**



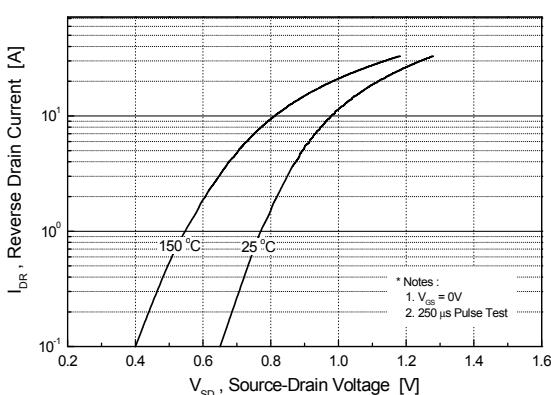
**Figure 2. Transfer Characteristics**



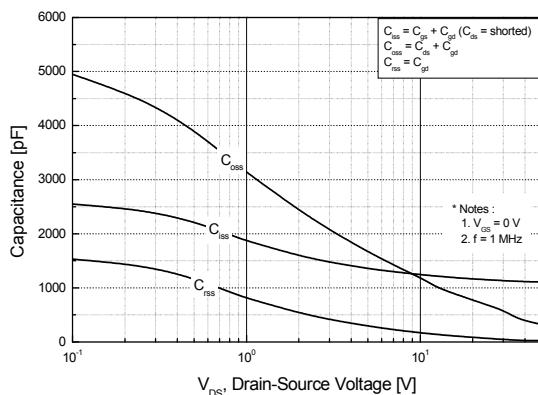
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



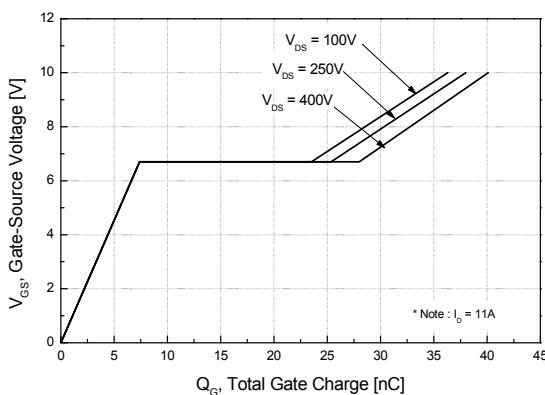
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

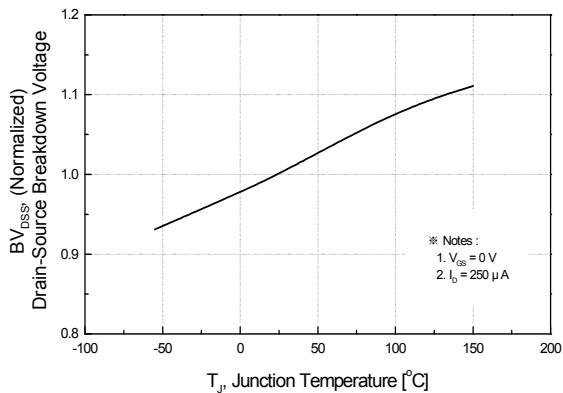


**Figure 6. Gate Charge Characteristics**

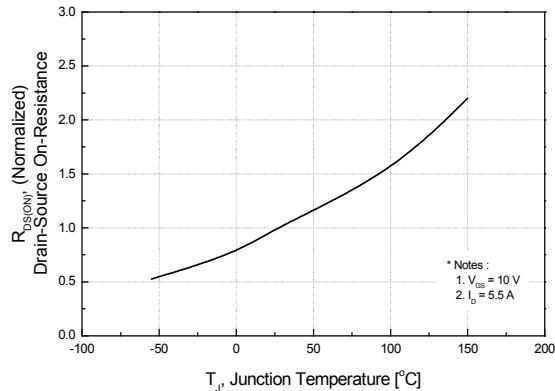


## Typical Performance Characteristics (Continued)

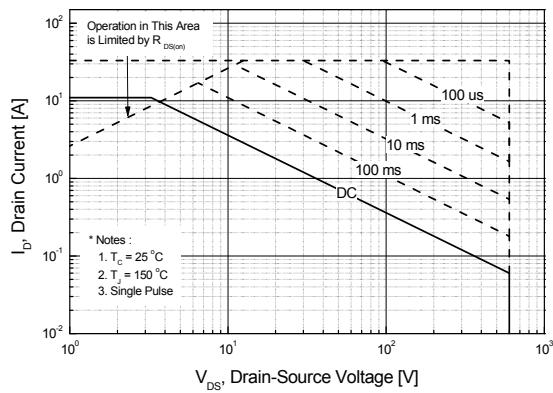
**Figure 7. Breakdown Voltage Variation vs. Temperature**



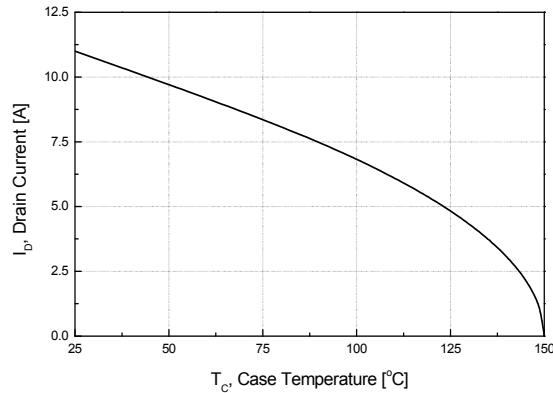
**Figure 8. On-Resistance Variation vs. Temperature**



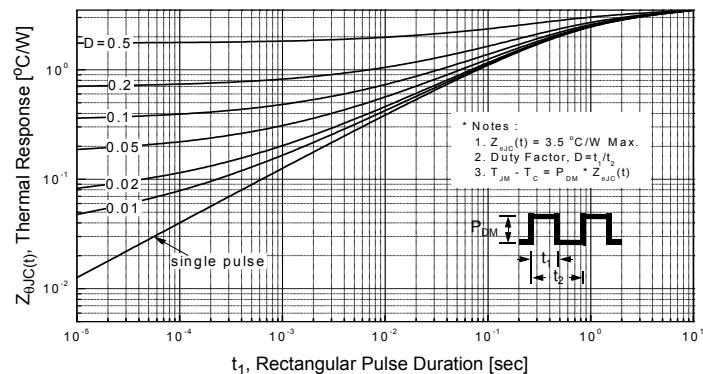
**Figure 9. Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Resistance Curve**



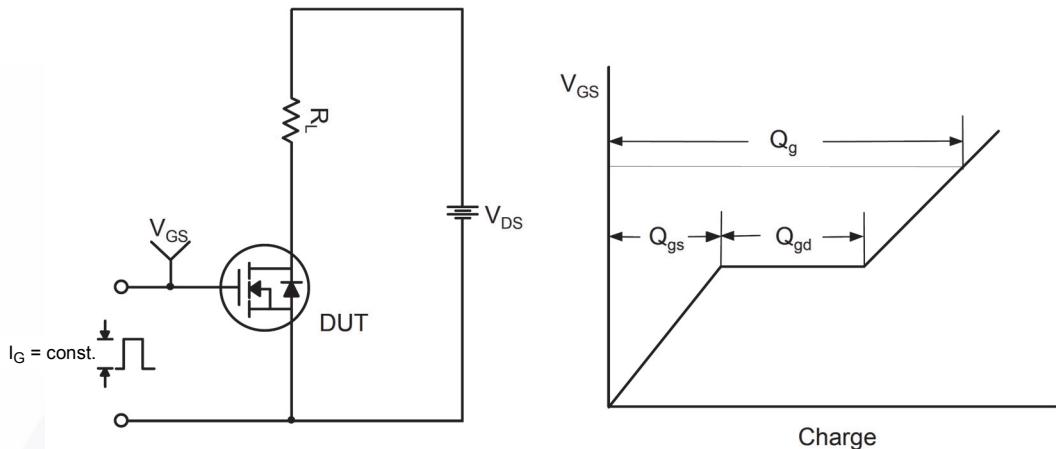


Figure 12. Gate Charge Test Circuit & Waveform

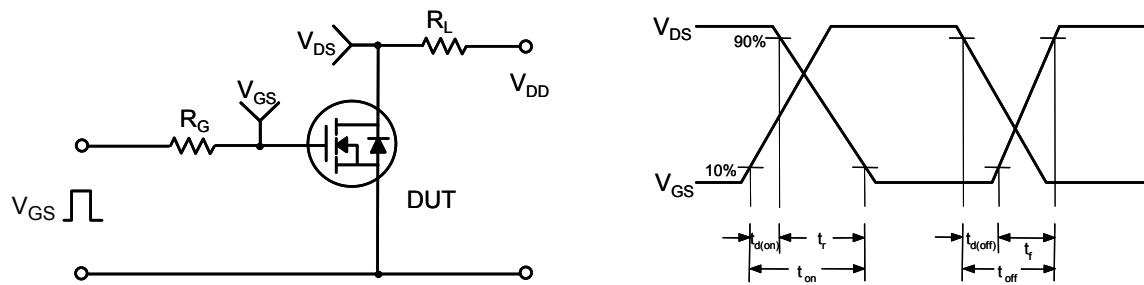


Figure 13. Resistive Switching Test Circuit & Waveforms

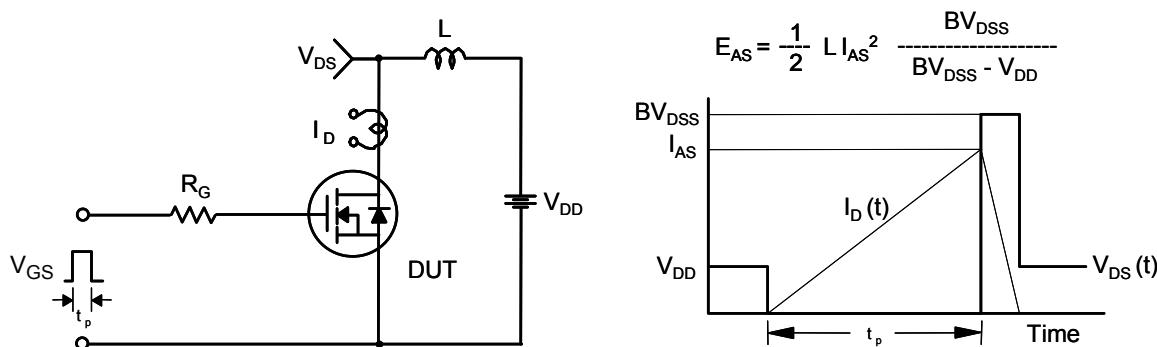


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

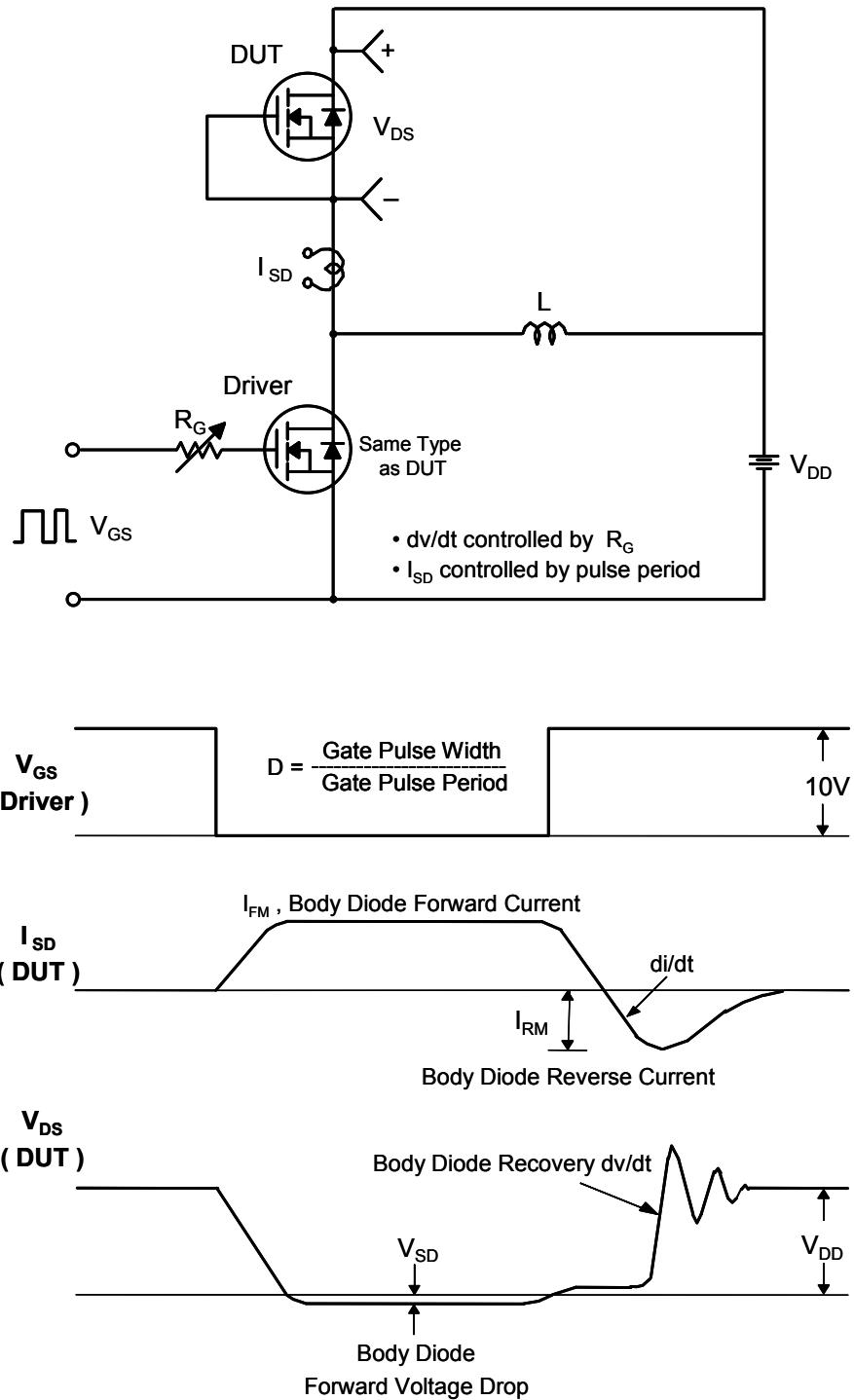
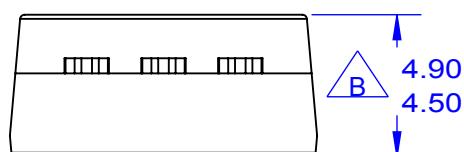
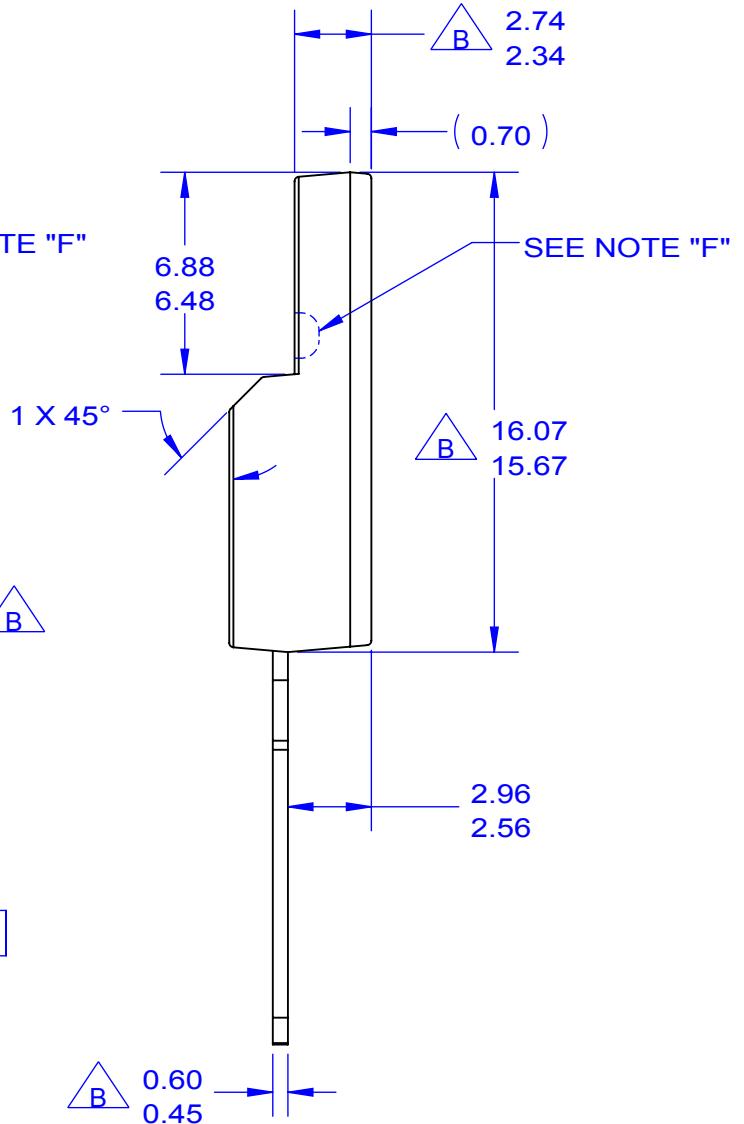
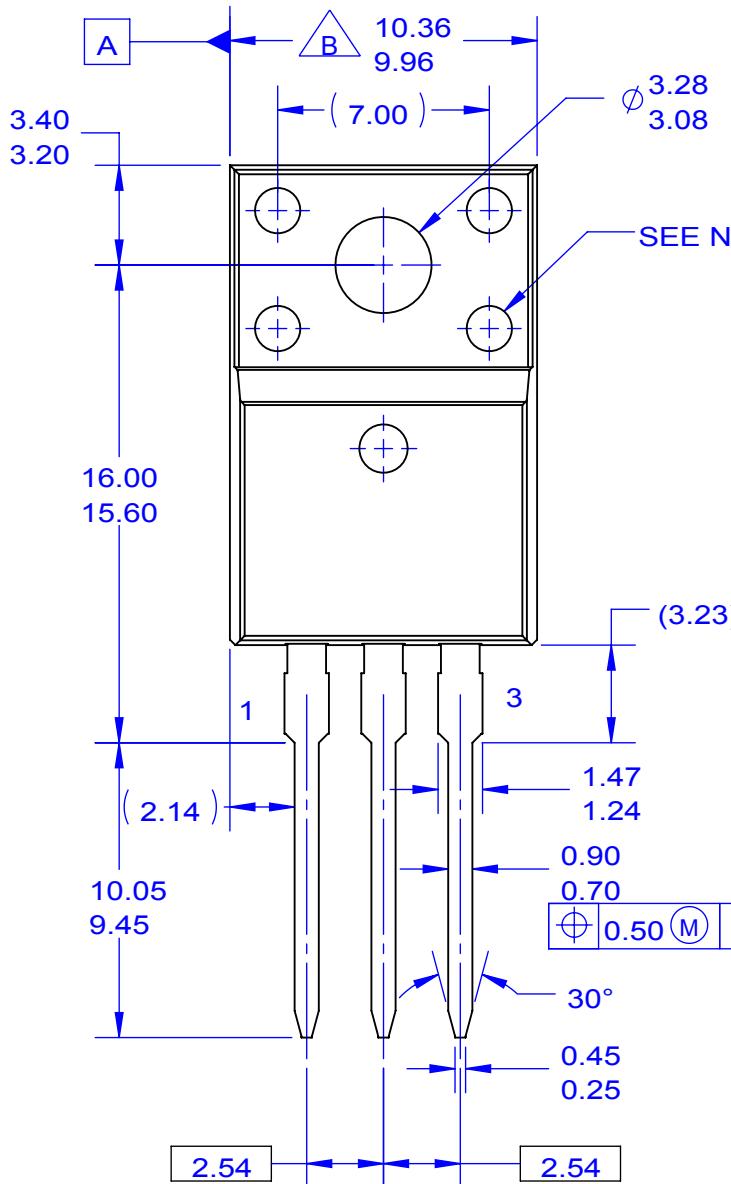


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



#### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3



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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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