*Click **here** to ask an associate for production status of specific part numbers.*

MAX22205

65V, 7.6A High Current Single H-Bridge with Integrated Current-Sense

General Description

The MAX22205 integrates a high current 65V, $7.6A_{MAX}$ H-Bridge to drive one Brushed DC motor or one half Stepper motor. The H-Bridge FETs feature very low impedance, resulting in high driving efficiency and low heat. The typical total R_{ON} (high-side + low-side) is 0.15Ω. The H-Bridge can be PWM controlled by two logic inputs (DINA, DINB). A third Enable (EN) logic input can be used to configure the outputs to high impedance for coasting the motor.

The MAX22205 features an accurate optional Current Drive Regulation (CDR), which can be used to limit the start up current of a Brushed DC motor or control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired threshold current. As soon as the bridge current exceeds the threshold (I_{TRIP}), the device enforces the decay for a fixed OFF-time (t_{OFF}). The non-dissipative ICS eliminates the bulky external power resistors normally required for this function, resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor. A current proportional to the internally-sensed motor current is output to the analog pins (ISENA, ISENB) to monitor current. Also, one open-drain output (CDR pin) is asserted every time the internal current regulation is taking control of the driver so that the activity of the internal current loop can be monitored.

The maximum output current per H-Bridge is I_{MAX} = $7.6A_{MAX}$ limited by the Overcurrent Protection (OCP). The device delivers up to 4ARMS at VM = +24V and TA = 25°C with proper PCB ground plane for thermal dissipation. The current capability depends on the PCB thermal characteristic (PCB ground planes, heatsinks, ventilation, etc.).

The MAX22205 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During Thermal Shutdown and Undervoltage Lockout, all the channels are disabled until normal operating conditions are restored.

The MAX22205 is packaged into a small TQFN38 5mm x 7mm package.

Applications

- Brushed DC Motor Driver
- Stepper Motor Driver
- Solenoid Driver
- Latched Valves

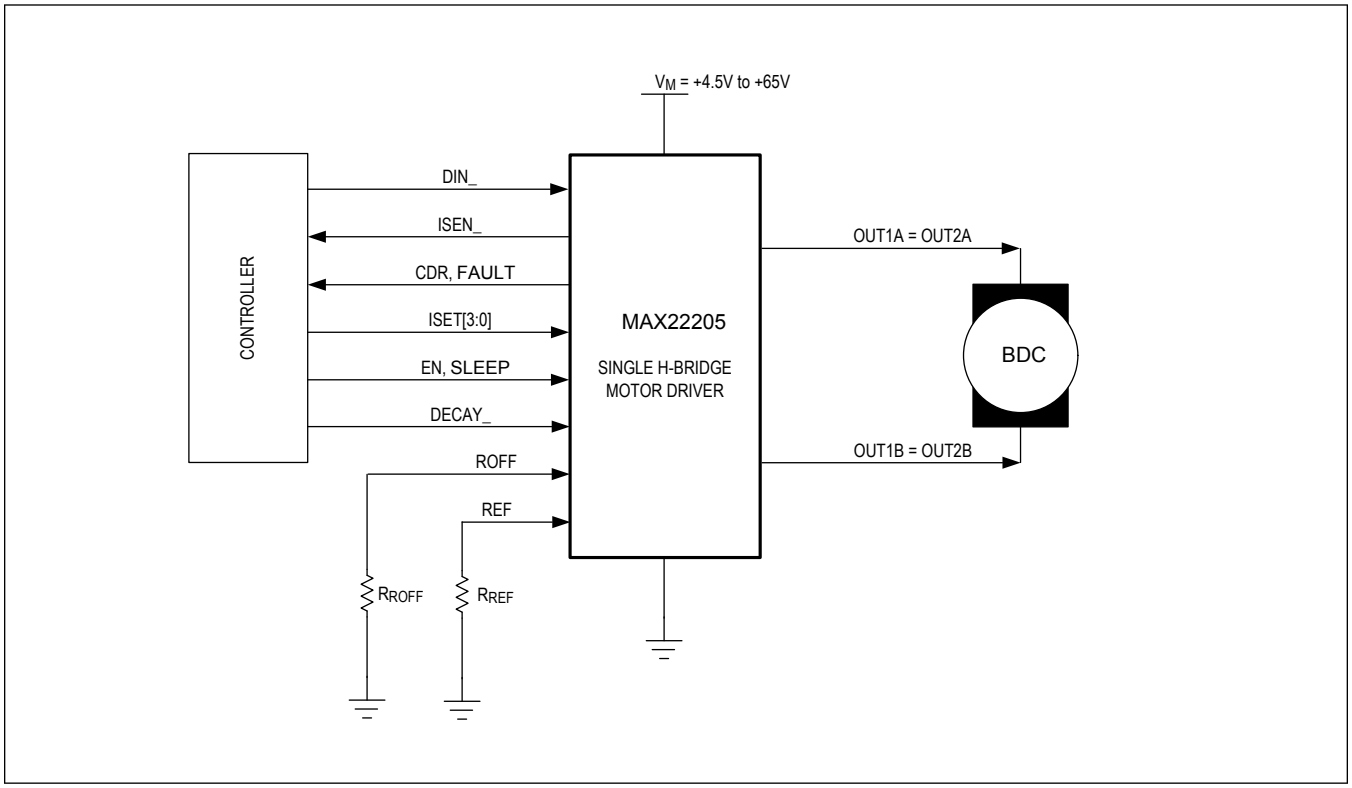
Benefits and Features

- One H-Bridge with +65V Voltage Rating
  - Total $R_{DS(ON)}$ (High-Side + Low-Side): 150mΩ Typical (T_A = 25°C)
- Current Ratings per H-Bridge (Typical at 25°C):
  - I_{MAX} = $7.6A_{MAX}$ (Impulsive Current for Driving Capacitive Loads)
  - I_{FS} = 6A (Max Full Scale Current Setting for Internal Current Drive Regulation)
  - I_{RMS} = $4A_{RMS}$ (T_A = 25°C, V_M = +24V)
- Integrated Current Control
  - Full-Scale DAC Current Configurable with External Resistance
  - Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Current Drive Regulation Monitor Output Pin (CDR Pin)
  - Integrated DAC Sets the Output Current Level among 16 Values
  - Multiple Decay Modes (Slow, Mixed, Fast)
  - Fixed OFF Time Configurable with External Resistance
- Current-Sense Output (Current Monitor)
- Fault Indicator Pin ($\overline{FAULT}$)
- Protections
  - Overcurrent Protection for each Individual Channel (OCP)
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown T_J = 155°C (TSD)
- TQFN38 5mm x 7mm Package (TSSOP38 4.4mm x 9.7mm Available in the Future)

***Ordering Information** appears at end of data sheet.*

19-101140A; Rev 0; 8/21

Simplified Block Diagram



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Absolute Maximum Ratings

V_M to GND ..... -0.3V to +70V
V_{DD} to GND.....-0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND ..... -0.3V to +0.3V
OUT_ ..... -0.3V to V_M + 0.3V
V_{CP} to GND..... V_M - 0.3V to min (+74V, V_M + 6V)
C_{P2} to GND ..... V_M - 0.3V to V_{CP} + 0.3V
C_{P1} to GND ..... -0.3V to V_M + 0.3V
FAULT to GND ..... -0.3V to 6V
CDR to GND..... -0.3V to 6V
ISET_ to GND ..... -0.3V to 6V
REF to GND .....-0.3V to min (+2.2V, V_{DD} + 0.3V)
ROFF to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ISEN_ to GND.....-0.3 to min (+2.2V, V_{DD} + 0.3V)
DIN_ to GND.....-0.3V to 6V
EN to GND .....-0.3V to 6V
DECAY_ to GND.....-0.3V to 6V
SLEEP to GND ..... -0.3V to min (+70V, V_M + 0.3V)
Operating Temperature Range .....-40°C to 125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (Reflow).....260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN 38 - 5mm x 7mm

Package Code	T3857-1C
Outline Number	21-0172
Land Pattern Number	90-0076
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 13kΩ to 60kΩ,

Limits are 100% tested at TA = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

, Typical Values are at V_M = 36V and TA = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_M		4.5		65	V
Sleep Mode Current consumption	I_{VM}	$\overline{SLEEP}$ = logic low			20	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high			5	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = 20mA		1.8		V
V_{DD} Current Limit	$I_{VDD(LIM)}$	V_{DD} shorted to GND	18			mA
Charge Pump Voltage	V_{CP}			V_M + 2.7		V

Electrical Characteristics (continued)

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 13kΩ to 60kΩ,
Limits are 100% tested at TA = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.
, Typical Values are at V_M = 36V and TA = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVEL INPUTS-OUTPUTS						
Input Voltage Level - High	V_{IH}		1.2			V
Input Voltage Level - Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pulldown Current	I_{PD}	Logic supply (V_L) = +3.3V	16	34	60	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.4	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = +3.3V	-1		1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pulldown Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output ON-Resistance Low-Side	RonLS	OUT1A = OUT1B, OUT2A = OUT2B		0.075	0.15	Ω
Output ON-Resistance High-Side	RonHS	OUT1A = OUT1B, OUT2A = OUT2B		0.075	0.15	Ω
Output Leakage	I_{LEAK}	Driver OFF	-20		+20	uA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			300		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	OCP		7.6			A
Overcurrent Protection Blanking Time	t_{OCP}			2.2	3.5	µs
Autoretry OCP Time	t_{RETRY}			3		ms
UVLO Threshold on V_M	UVLO	V_M rising	3.75	4	4.25	V
UVLO Threshold on VM Hysteris	$UVLO_{HYS}$			0.12		V
Thermal Protection Threshold Temperature	T_{SD}			155		°C
Thermal Protection Temperature Hysteresis	T_{SD_HYST}			20		°C
CURRENT REGULATION						
REF Pin Resistor Range	R_{REF}		12		60	kΩ
REF Output Voltage	V_{REF}			900		mV

Electrical Characteristics (continued)

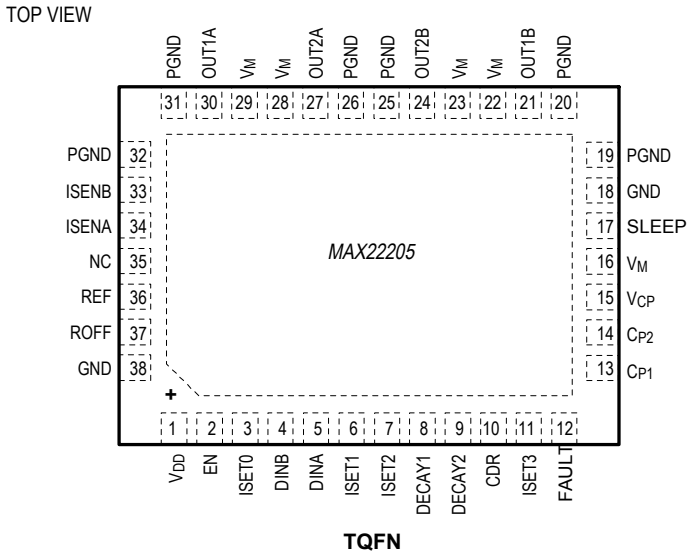
(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ , R_{REF} = from 13kΩ to 60kΩ,
Limits are 100% tested at TA = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.
, Typical Values are at V_M = 36V and TA = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale Current Constant	KIFS				72		KV
Current Trip Regulation Accuracy	DITRIP1	I_{FS} = 6A (Note 1)	I_{TRIP} from 2.2A to 6A	-6		+6	%
	DITRIP2		I_{TRIP} from 1A to 2.2A	-10		+10	
Fixed OFF – Time Internal	t_{OFF}	ROFF shorted to V_{DD}		16	20	24	µs
Fixed OFF – Time Constant	KTOFF	R_{ROFF} from 15KΩ to 120KΩ			0.667		µs/kΩ
PWM Blanking time	t_{BLK}				2.5		µs
CURRENT SENSE MONITOR							
ISEN_ Voltage Range	V_{ISEN}	Voltage Range at Pin ISEN_		0		1.1	V
Current Monitor Scaling Factor	KISEN	See the I_{SEN} Output Current Equation in the Current Sense Output (CSO) - Current Monitor Section.			7500		A/A
Current Monitor Accuracy	$DKISEN_1$	I_{FS} = 6A (Note 1)	I_{TRIP} from 2.2A to 6A	-5		+5	%
	$DKISEN_2$		I_{TRIP} from 1A to 2.2A	-10		+10	
Settling Time	t_S	$I_{FS} = I_{MAX}$			0.5		µs
FUNCTIONAL TIMINGS							
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = 1 to OUT_ tristate			40		µs
Wakeup Time From Sleep	t_{WAKE}	$\overline{SLEEP}$ = 0 to normal operation				2.7	ms

Note 1: Guaranteed by design, not production tested.

Pin Configuration

Pin Configuration



TQFN

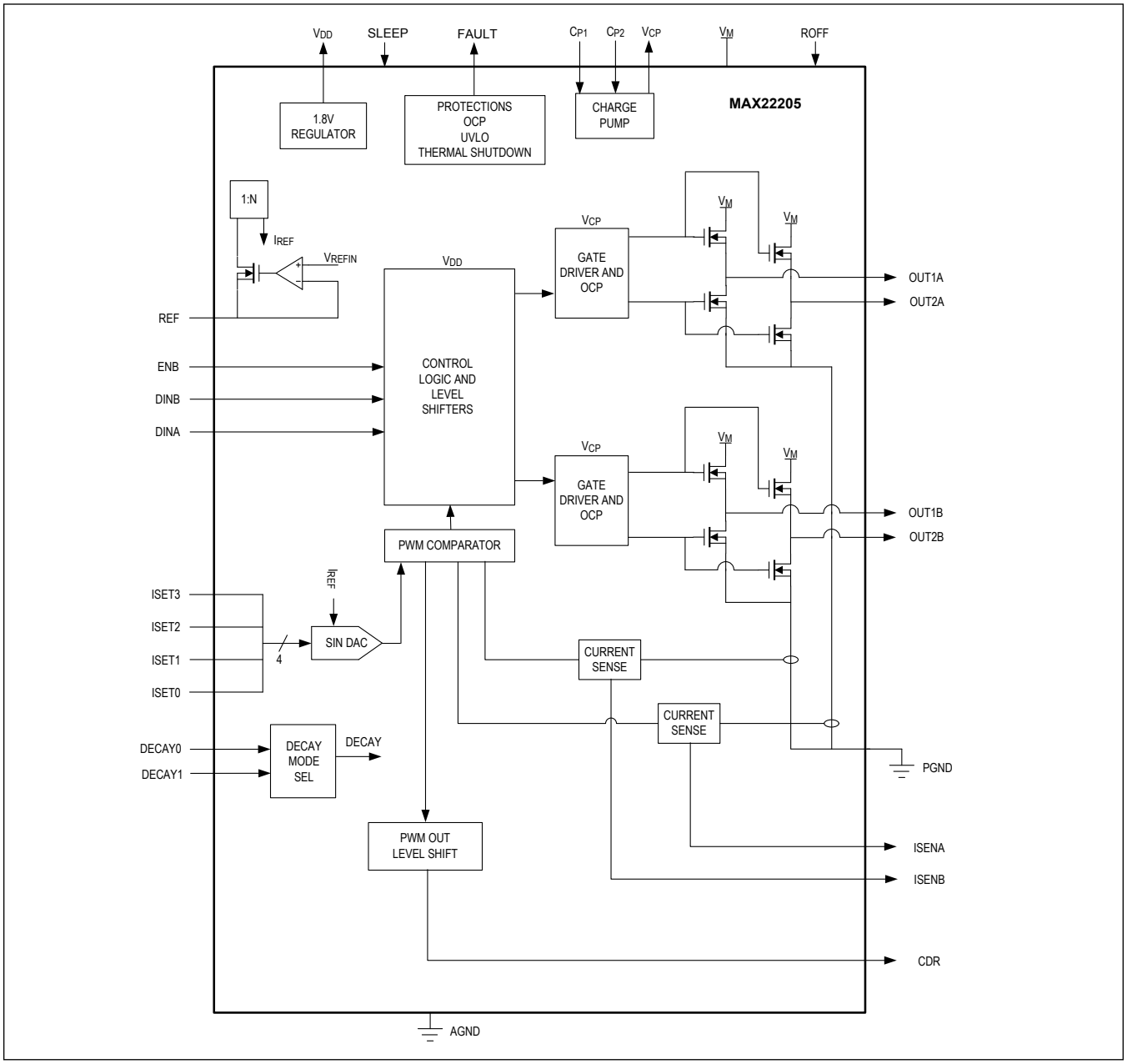
Pin Description

PIN	NAME	FUNCTION	TYPE
16, 22, 23, 28, 29	V_M	Supply Voltage Input. Connect at least 1µF SMD plus 10µF electrolytic bypass capacitors to GND. Higher values can be considered depending on application requirements.	Supply
15	V_{CP}	Charge Pump Output. Connect a 5V, 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
13	C_{P1}	Charge Pump Flying Capacitor Pin1. Connect a V_M-rated 22nF capacitor between C_{P1} and C_{P2} as close as possible to the device.	Output
14	C_{P2}	Charge Pump Flying Capacitor Pin 2. Connect a V_M-rated 22nF capacitor between C_{P1} and C_{P2} as close as possible to the device.	Output
1	V_{DD}	1.8V LDO Output. Connect a 5V, 2.2µF to GND close to the device.	Analog Output
17	$\overline{SLEEP}$	Active Low Sleep Pin	Logic Input
21, 24, 27, 30	OUT_	Driver Output Pins. Connect OUT1A and OUT2A and connect OUT1B and OUT2B together by wide, low-resistance PCB traces.	Output
12	$\overline{FAULT}$	Open-Drain Output Active Low-Fault Indicator. Connect a 2KΩ resistor to the controller supply voltage.	Open Drain Output
33, 34	ISEN_	Current-Sense Output Monitor. Connect a resistor to GND (see the Current-Sense Output section).	Output

Pin Description (continued)

PIN	NAME	FUNCTION	TYPE
2	EN	Logic Input Pin. Enable Pin	Logic Input
4, 5	DIN_	CMOS PWM Input	Logic Input
8, 9	DECAY_	Logic Input. Set the Decay Mode	Logic Input
3, 6, 7, 11	ISET_	Programmable Current Logic Input	Logic Input
10	CDR	Open-Drain Output - Current Drive Regulator. Add a pullup resistor to the controller supply voltage. The pullup resistor value depends on application requirements. Values between 1KΩ to 5KΩ meet the requirements for most applications.	Open Drain Output
36	REF	Programmable Current Analog Input. Connect a resistor from REF to GND to set the full scale current.	Analog Input
37	ROFF	t_{OFF} Programmable Off Time Pin. Connect ROFF to V_{DD} to use the internal fixed t_{OFF} time. Connect a resistor R_{ROFF} from ROFF to GND to set the fixed OFF time to a desired value.	Analog Input
18, 38	GND	Analog Ground. Connect to ground plane.	GND
19, 20, 25, 26, 31, 32	PGND	Power GND. Connect to ground plane.	GND
EP	EP	Exposed PAD. Connect to GND.	GND

Functional Diagrams



Detailed Description

The MAX22205 integrates an high current 65V, $7.6A_{MAX}$ H-Bridge. It can be used to drive one Brushed DC motor or one half Stepper motor. The H-Bridge FETs feature very low impedance, resulting in high driving efficiency and low heat generated. The typical total R_{ON} (high-side + low-side) is 0.15Ω. The H-Bridge can be individually PWM controlled with two logic inputs (DINA, DINB). A third Enable (EN) logic input can be used to configure the outputs to high impedance for coasting the motor.

The MAX22205 features an accurate optional Current Drive Regulation (CDR), which can be used to limit the start-up current of a Brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired threshold current. As soon as the bridge current exceeds the threshold (I_{TRIP}), the device enforces the decay for a fixed OFF-time (t_{OFF}).

The non-dissipative ICS eliminates the bulky external power resistors, which are normally required for this function, resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor. A current proportional to the internally-sensed motor current is output to analog pins (ISENA, ISENB) to monitor the current. Also, one open-drain output (CDR pin) is asserted every time the internal current regulation is taking control of the driver so that the activity of the internal current loop can be monitored.

The maximum output current per H-Bridge is $I_{MAX} = 7.6A_{MAX}$ limited by the Overcurrent Protection (OCP). The device delivers up to $4A_{RMS}$ at V_M = +24V and T_A = 25°C with proper PCB ground plane for thermal dissipation. The current capability depends on the PCB thermal characteristic (PCB ground planes, heatsinks, ventilation, etc.).

The MAX22205 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During Thermal Shutdown and Undervoltage Lockout, all the channels are disabled until normal operating conditions are restored.

The MAX22205 is packaged into a small TQFN38 5mm x 7mm package.

Sleep Mode ($\overline{SLEEP}$ Pin)

Drive this pin low to enter in the lowest power mode. All outputs are tristated and the internal circuits are biased off. The charge pump is also disabled. A pulldown resistor is connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. This mode corresponds to the lowest power consumption possible. Waking up from Sleep mode to Normal mode takes up to 2.7ms maximum.

PWM Control

OUT1A must be externally connected to OUT2A and OUT1B must be externally connected to OUT2B.

When the part is Enabled (EN = Logic High) and the H-Bridge current is below the configured current limit, the average output voltage can be controlled by DINA and DINB logic input pins using PWM techniques. Setting Enable logic low causes the output to enter a high impedance mode and the motor to coast. The Enable input pin frequency must not exceed 1KHz and cannot be used for PWM control.

Table 1 shows the control Truth Table.

Table 1. MAX22205 Truth Table

EN	DINA	DINB	OUT1A = OUT2A	OUT1B = OUT2B	DESCRIPTION
0	X	X	High-Z	High-Z	H-Bridge Disabled. High Impedance (HiZ)
1	0	0	L	L	Brake Low; Slow Decay
1	1	0	H	L	Current from OUT2 to OUT1
1	0	1	L	H	Current from OUT1 to OUT2
1	1	1	H	H	Brake High; Slow Decay

PWM techniques can be used to control the output duty cycle and hence to implement motor speed control. Typically, for brushed DC motor drivers, Slow Decay is preferred as it results in less ripple and higher efficiency. With this approach, during the OFF phase, both the low-side FETs are activated effectively grounding the motor winding terminals. The current built up into the motor winding slowly decays. This decay is often referred to as Slow Decay.

Alternatively, Fast Decay can also be implemented by reversing the bridge during the OFF phase.

Current-Sense Output (CSO) - Current Monitor

Currents proportional to the internally-sensed motor currents are output to pins ISENA, ISENB for half-bridge A (OUT1A = OUT2A) and B (OUT1B = OUT2B) respectively. The current is sensed only when the low side FET is ON and sinks current. During the blanking time, the ISEN current is zero.

The following equation shows the relationship between the current sourced at ISEN and the half-bridge low-side FET current:

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current mirror factor between the output current and its replica at pin ISEN. K_{ISEN} is typically 7500 A/A. For instance, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

ISENA can be externally tied to ISENB to sum up the two half-bridges low-side currents and monitor the full-bridge current. When used in this configuration, the ISEN = ISENA + ISENB current reflects the motor current during the Forward, Reverse, and Slow Decay statuses while it is zeroed during Fast Decay or Coast Status.

Figure Figure 1 shows an idealized behavior of the ISEN = ISENA + ISENB current when Slow or Fast Decay are used. Blanking times, delays, and rise/fall edges are ignored.

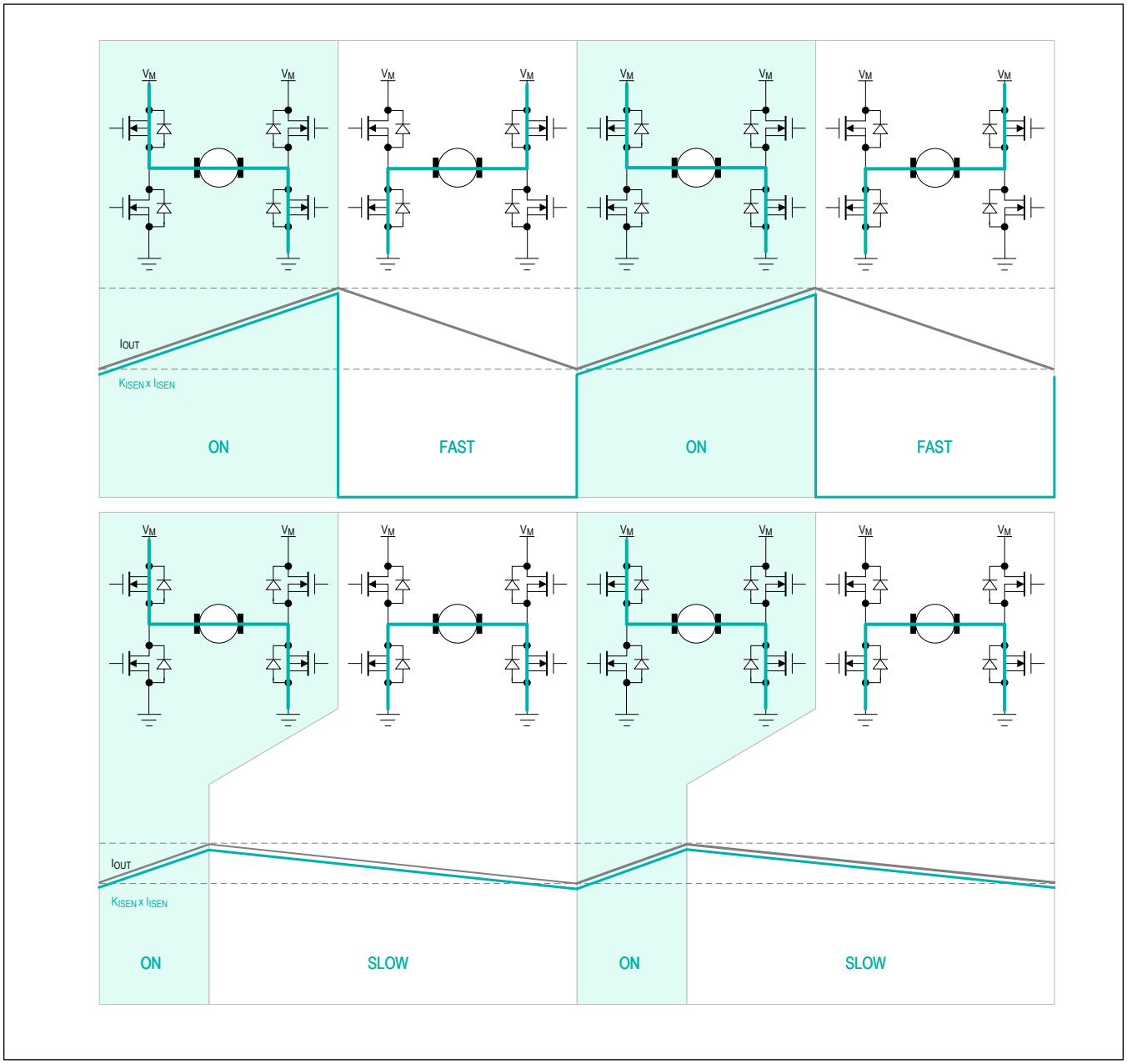


Figure 1. ISEN Current

By connecting an external signal resistor, R_{ISEN}, between ISEN_ and GND, a voltage proportional to the motor current is generated. The voltage built up on R_{ISEN} can be input into the ADC of an external controller in applications in which the motor control algorithm requires the current/torque information. The designer can choose R_{ISEN} value so that the peak voltage meets the ADC full-scale requirement. The following equation shows the design formula to calculate R_{ISEN} once the ADC full scale voltage (V_{FS}) and the maximum operating current (I_{MAX}) are known:

$$R_{ISEN}(\Omega) = K_{ISEN} \times \frac{V_{FS}(V)}{I_{MAX}(A)}$$

Equation - R_{ISEN} Setting

For example, if the ADC operates up to 1V FS and the maximum operating output current is 2A, then R_{ISEN} is 7500 x 1V/2A = 3.75KΩ.

The R_{ISEN} value also sets the output impedance of the Current-Sense Output circuit (ISEN_ output impedance). Normally, the input impedance of the ADC is much higher than R_{ISEN}, enabling a direct connection to the ISEN pin without attenuation. If a low input impedance ADC is used, a preamplifier (buffer) is required.

The Current-Sense Output circuit bandwidth and step response performances (see Specifications) ensure the current monitor tracks the driver current in PWM motor drive application.

Current Drive Regulation

The MAX22205 features embedded Current Drive Regulation (CDR).

The embedded current drive regulation provides an accurate control of the current flowing into the motor windings.

The bridge current is sensed by a non-dissipative Integrated Current Sensing (ICS) circuit and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). The device supports different decay modes as described in the following paragraphs.

Once t_{OFF} elapses, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, on the motor inductance, and on motor speed and load conditions.

The t_{OFF} duration can be configured with an external resistor connected to the ROFF pin.

Integrated Current-Sense (ICS)

A non-dissipative current sensing is integrated. This feature eliminates the bulky external power resistors normally required for this function. This feature results in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

Setting the Full-Scale Current – Pin REF

Connect a resistor from REF to GND to set the full scale chopping current I_{FS}.

The following equation shows the typical I_{FS} current as a function of the R_{REF} shunt resistor connected to pin REF. The proportionality constant K_{IFS} is typically 72KV. The external resistor R_{REF} can range between 12KΩ and 60KΩ, which correspondents to I_{FS} setting ranging from about 6A down to 1.2A.

$$I_{FS} = \frac{K_{IFS(KV)}}{R_{REF(K\Omega)}}$$

Bridge Current Control

Four input pins, ISET[3:0], are used to program the regulated output current. Table 2 shows the bridge current levels for each input combination.

Table 2. H-Bridge ISET Pins Truth Table

ISET3	ISET2	ISET1	ISET0	RELATIVE CURRENT (% OF IFS)
0	0	0	0	100%
0	0	0	1	99.2%
0	0	1	0	97.6%
0	0	1	1	95.3%
0	1	0	0	91.3%
0	1	0	1	86.6%
0	1	1	0	81.1%

Table 2. H-Bridge ISET Pins Truth Table (continued)

0	1	1	1	74.0%
1	0	0	0	66.9%
1	0	0	1	59.1%
1	0	1	0	50.4%
1	0	1	1	40.9%
1	1	0	0	30.7%
1	1	0	1	20.5%
1	1	1	0	10.2%
1	1	1	1	0.0%

Setting the Fixed OFF_TIME (t_{OFF})

The current regulation circuit is based on a constant t_{OFF} PWM control. When the bridge current exceeds the target I_{TRIP} current, an OFF phase begins and Decay modes are activated. The OFF phase has a fixed time duration (t_{OFF}). t_{OFF} can be configured to a desired value by connecting an external resistor (R_{ROFF}) to pin ROFF. When the ROFF pin is shorted to V_{DD}, the t_{OFF} time is internally set at a fixed value (20µs typical).

By connecting an external resistor to the pin ROFF, configure t_{OFF} as shown in the following equation, in which R_{ROFF} is an external resistor connected to the ROFF pin (in KΩ) and KT_{OFF} is an internal constant equal to 0.667µs/KΩ.

$$t_{OFF}(\mu s) = R_{ROFF} \times K_{TOFF}$$

t_{OFF} can be programmed from a range of 10µs to 80µs.

CDR Open-Drain Output

This pin is an active-low open-drain output, which is asserted during the fixed decay time interval (t_{OFF}) enforced by the current drive regulation loop. This way, the external controller can monitor if the integrated current loop has taken control of the driver overwriting the status of the PWM logic inputs (DINA, DINB). The CDR signal can be used by the external controller for several reasons and provides information about the actual load during current regulation. In the use case in which the PWM logic inputs are permanently held in the Forward or Reverse mode and the control is entirely entrusted to the internal Current Drive Regulation loop, the CDR pin status directly reflects the driver output status. In this case, the duty cycle of the CDR can possibly be used to detect stall conditions.

Connect a pullup resistor from the CDR pin to the controller voltage supply. The pullup resistor value depends on the application requirements. Values between 1KΩ to 5KΩ meet the requirements for most applications.

The time diagram in Figure 2 shows the behavior of this function when the motor spins in the forward direction respectively with DINB held firmly high (Case A) or when DINB is toggling (Cases B and C). The CDR output is asserted only when the Slow Decay mode is forced by the internal CDR. Note that any PWM transitions reset the fixed off time of the CDR circuit. In Case B, the actual Slow Decay Interval is longer than t_{OFF}, whereas in Case C, the actual Slow Decay interval is shorter.

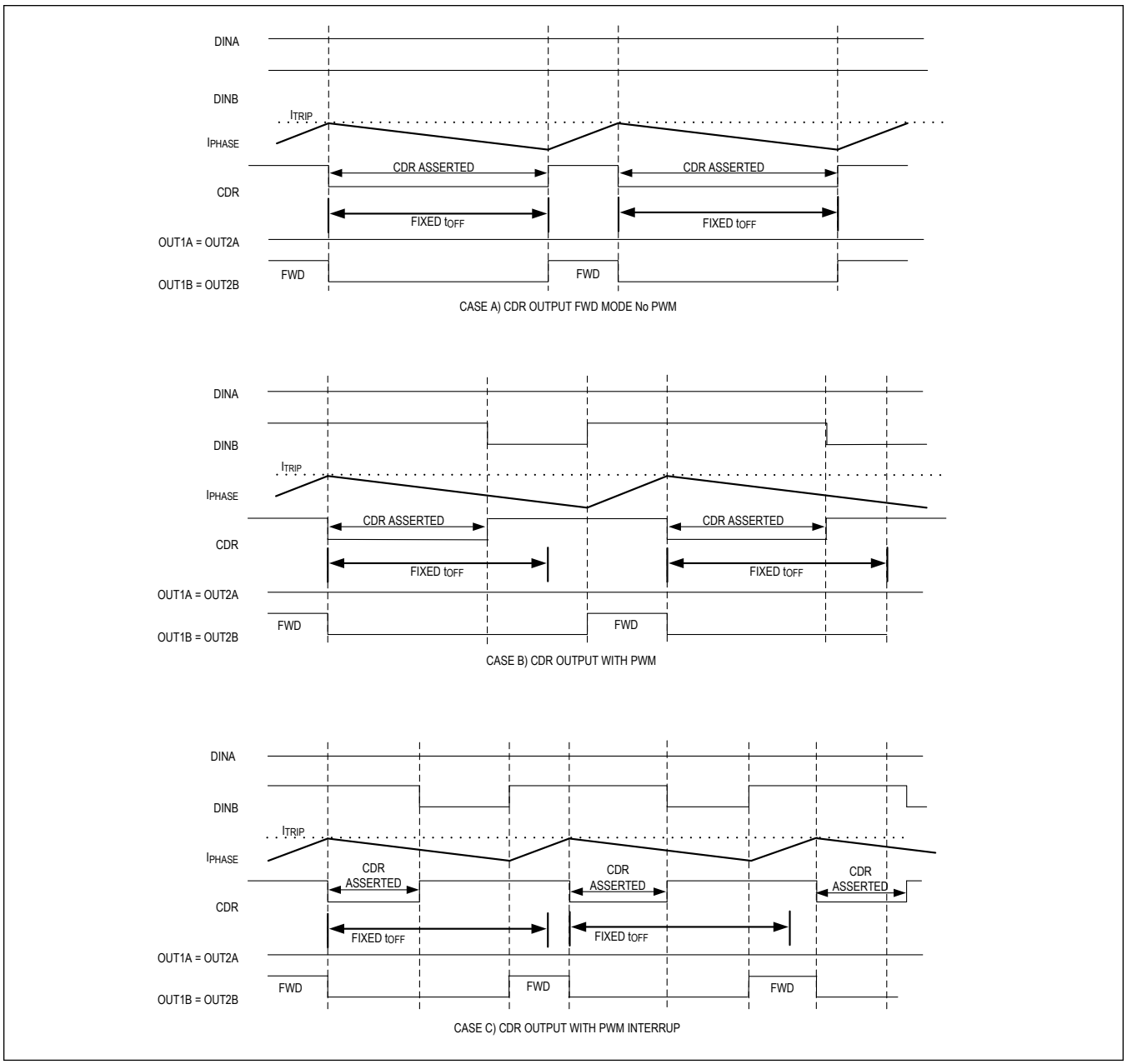


Figure 2. CDR Monitor Timing Diagram

Operating Modes

During PWM chopping, the driver output alternates the Energizing (ON) and Decay phases. The MAX22205 supports different Decay modes. Slow Decay, Fast Decay, and different combinations between Slow and Fast.

Figure 3 shows the current path in the three different modes of operation.

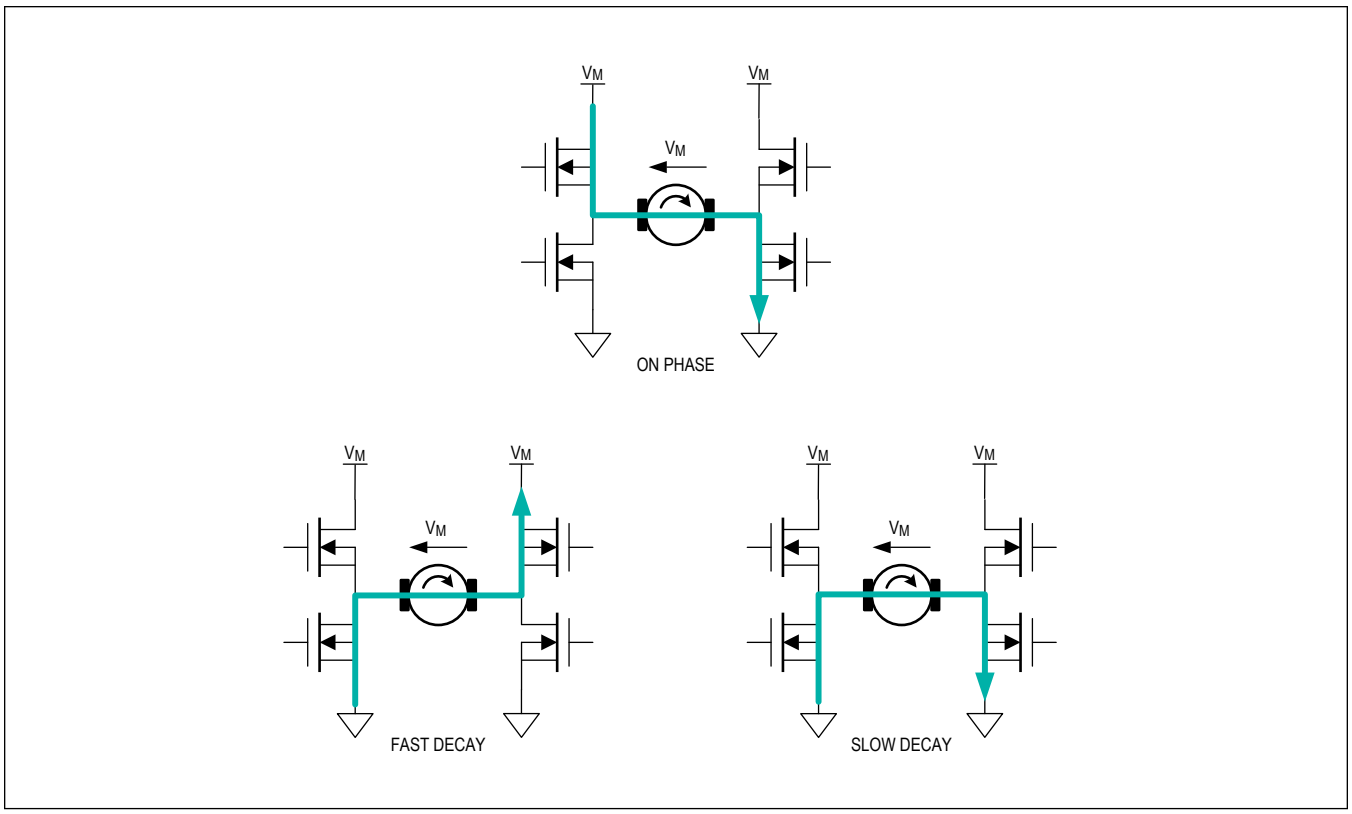


Figure 3. Current Flow During ON and Decay Modes

Setting the Decay Mode

Two logic input pins allow to set the Decay Mode during t_{OFF}. The MAX22205 supports Slow, Fast, and Mixed Decay modes.

Table 3 shows the Truth Table for the Decay selection.

Table 3. Decay Mode Truth Table

DECAY2	DECAY1	DECAY MODE
0	0	SLOW
0	1	MIXED 30% FAST* / 70% SLOW
1	0	MIXED 60% FAST* / 40% SLOW
1	1	FAST*

*To prevent reversal of current during fast decay, outputs go to the high-impedance state as the current approaches 0A.

Protections

Overcurrent Protection – (OCP)

An Overcurrent Protection (OCP) protects the device against short circuits to the rails (supply voltage and ground) and across the load terminals.

The OCP threshold is set at 7.6A minimum. If the output current is greater than the OCP threshold for longer than the Deglitch Time (Blanking Time), then an OCP event is detected.

When an OCP event is detected, the H bridge is immediately disabled, and a fault indication is output on pin $\overline{FAULT}$. The H-Bridge is kept in HiZ mode for 3ms (see t_{RETRY} specification). After that, the H-bridge is re-enabled according to the

current state. If the short circuit is still present, this cycle repeats, otherwise normal operation resumes.

Avoid prolonged operation under the short-circuit failure mode as a prolonged OCP auto-retry could affect the device reliability.

Thermal Shutdown Protection (TSD)

If the die temperature exceeds 155°C (typical value), a fault indication is output on pin $\overline{FAULT}$ and the driver is tristated until the junction temperature drops below 135°C. After that, the driver is re-enabled.

Undervoltage Lockout Protection (UVLO)

The device UVLO on V_M is set at 4.25V maximum. When a UVLO event occurs, a fault indication is output on pin $\overline{FAULT}$ and driver outputs are tristated. Normal operation resumes (and the $\overline{FAULT}$ pin deasserts) as soon as the supply voltages are back in the nominal operating range.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22205ATU+T	-40°C to +125°C	38 TQFN
MAX22205AUU+T*	-40°C to +125°C	38 TSSOP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

** Denotes future product. Contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—