BLM8AD22S-60ABG

LDMOS 2-stage integrated Doherty MMIC

Rev. 2 — 11 April 2019

AMPLEON

Product data sheet

1. Product profile

1.1 General description

The BLM8AD22S-60ABG is a dual section solution using Ampleon's state of the art GEN8 LDMOS technology. It includes a 45 W 2-stage fully integrated Doherty MMIC in section A, and a 15 W, 2-stage MMIC in section B, allowing a 3-way 1:2:1 Doherty when both sections are externally combined. The carrier and peaking devices, input splitter and output combiner, of the 2-stage fully integrated Doherty MMIC of section A are integrated in package. This device is perfectly suited as final stage in massive MIMO or small cell applications in the frequency range from 2100 MHz to 2200 MHz. Available in gull wing.

Table 1. Performance

Typical RF performance at T_{case} = 25 °C; I_{Dq} = 105 mA (driver and final stages); $V_{GS(peak)(A)} = V_{GS(carrier)(A)} - 0.65$ V; $V_{GS(peak)(B)} = V_{GS(carrier)(A)} - 1.25$ V. Single carrier LTE; carrier spacing = 20 MHz; PAR = 7.6 dB at 0.01 % probability on CCDF.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
single carrier LTE 20 MHz	2140	28	10	28.2	46.7	–34.7

1.2 Features and benefits

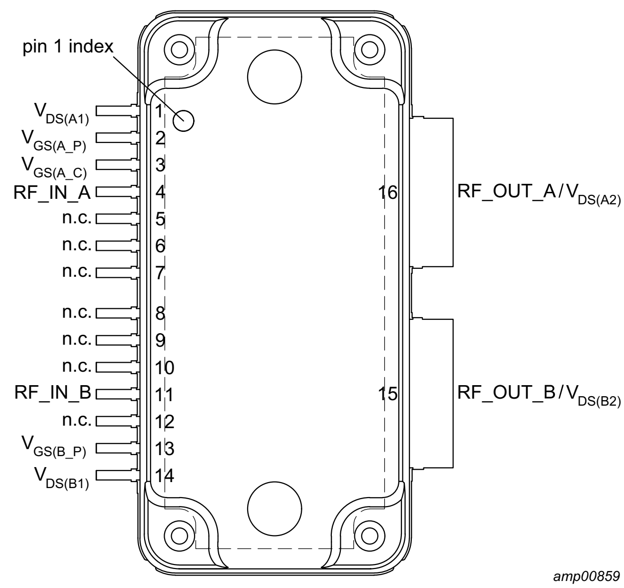
- Integrated input splitter in section A
- Integrated output combiner in section A
- Very high efficiency thanks to 3-way Doherty architecture
- Designed for broadband operation (frequency 2100 MHz to 2200 MHz)
- Integrated temperature compensated bias
- Independent control of carrier and peaking bias
- Integrated ESD protection
- Excellent thermal stability
- Source impedance 50 Ω; high power gain
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard GSM, W-CDMA and LTE base stations in the 2100 MHz to 2200 MHz frequency range

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of driver stages of section A
$V_{GS(A\_P)}$	2	gate-source voltage of peaking A_P
$V_{GS(A\_C)}$	3	gate-source voltage of carrier A_C
RF_IN_A	4	RF input section A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input section B
n.c.	12	not connected
$V_{GS(B\_P)}$	13	gate-source voltage of peaking B_P
$V_{DS(B1)}$	14	drain-source voltage of driver stages of section B

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT_B/$V_{DS(B2)}$	15	RF output section B / drain-source voltage of final stages of section B
RF_OUT_A/$V_{DS(A2)}$	16	RF output section A / drain-source voltage of final stages of section A
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM8AD22S-60ABG	-	plastic, heatsink small outline package; 16 leads	OMP-780-16G-1

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C [1]		
		section A: P_L = 7.08 W	1.86	K/W
		section B: P_L = 2.51 W	3.48	K/W

[1] When operated with a 1-carrier W-CDMA with PAR = 9.9 dB.

6. Characteristics

Table 6. DC characteristics
T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Section A						
Carrier						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 90 mA	1.5	2.2	2.65	V
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Peaking						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 90 mA	1.3	1.7	2.0	V
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
Section B						
Peaking						
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 110 mA	1.5	2.2	2.65	V
I_{GSS}	gate leakage current	V_{GS} = 1 V; V_{DS} = 0 V	-	-	140	nA
Final stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA
Driver stages						
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	μA

Table 7. RF Characteristics
Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; t_p = 100 μs; δ = 10 %; f = 2170 MHz.
Test signal: pulsed CW.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Section A						
I_{Dq} = 90 mA (carrier); $P_{L(AV)}$ = 4 W; $V_{GSq(peaking)}$ = $V_{GSq(carrier)}$ − 0.45 V.						
G_p	power gain		26.8	28.8	30.8	dB
η_D	drain efficiency	P_L = 4 W	33	38	-	%
		P_L = $P_{L(3dB)}$	45	50	-	%
RL_{in}	input return loss		-	−15	−10	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		45	46.1	-	dBm
Section B						
I_{Dq} = 110 mA; $P_{L(AV)}$ = 6.3 W.						
G_p	power gain		30.3	31.8	33.3	dB
η_D	drain efficiency	P_L = 6.3 W	30	35	-	%
		P_L = $P_{L(3dB)}$	43	48	-	%
RL_{in}	input return loss		-	−15	−10	dB
$P_{L(3dB)}$	output power at 3 dB gain compression		40.8	41.4	-	dBm

7. Application information

Table 8. Typical performance

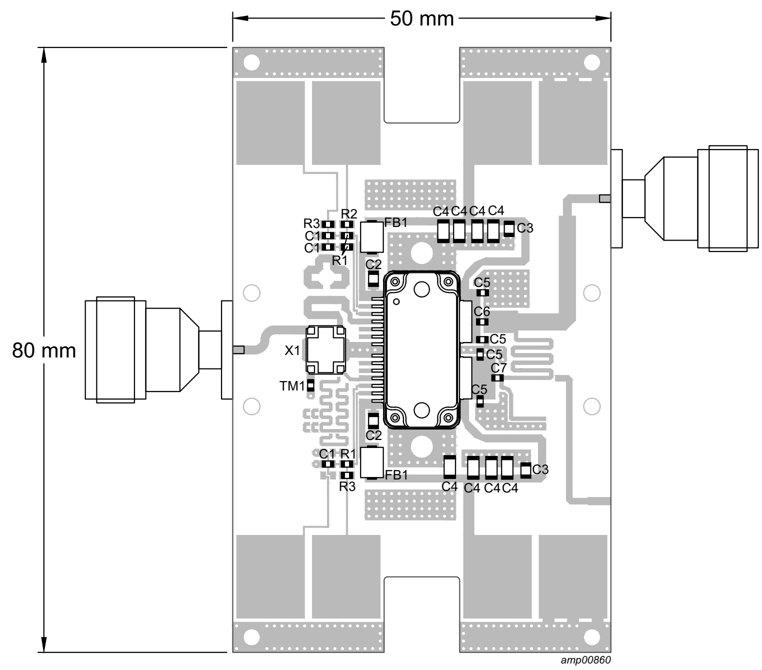
T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 105 mA (driver and final stages). Test signal: 1-carrier LTE; PAR = 7.6 dB; unless otherwise specified, measured in an Ampleon 2110 MHz to 2170 MHz frequency band combined integrated Doherty application circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 2140 MHz [1]	-	47.9	-	dBm
$\varphi_{s21}/\varphi_{s21(norm)}$	normalized phase response	f = 2140 MHz at 3 dB compression point [2]	-	–23.7	-	°
η_D	drain efficiency	8.5 dB OBO ($P_{L(AV)}$ = 40 dBm; $P_{L(M)}$ = 48.5 dBm); f = 2140 MHz	-	46.7	-	%
G_p	power gain	$P_{L(AV)}$ = 40 dBm; f = 2140 MHz	-	28.2	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 38 dBm set to obtain IMD3 = –32 dBc; 2-tone CW; f = 2140 MHz	-	180	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 40 dBm; f = 2110 MHz to 2170 MHz	-	0.2	-	dB
$ACPR_{20M}$	adjacent channel power ratio (20M)	$P_{L(AV)}$ = 40 dBm; f = 2140 MHz	-	–34.7	-	dBc
$\Delta G/\Delta T$	gain variation with temperature	f = 2140 MHz [3]				
		section A	-	0.047	-	dB/°C
		section B	-	0.042	-	dB/°C
K	Rollett stability factor	f = 0.3 GHz to 6 GHz [3]				
		section A: T_{case} = –40 °C	-	>2.5	-	
		section B: T_{case} > 0 °C	-	>1	-	

[1] Pulsed CW power sweep measurement (δ = 10 %; t_p = 100 μs).

[2] 25 ms CW power sweep measurement.

[3] S-parameters measured with dual path broadband demo board.



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

See Table 9 for a list of components.

Fig 2. Component layout

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 μF, 10 V	Murata: SMD 0603
C2	multilayer ceramic chip capacitor	10 μF, 35 V	TDK: SMD 0805
C3	multilayer ceramic chip capacitor	15 pF	Murata: SMD 0805
C4	multilayer ceramic chip capacitor	10 μF, 50 V	Murata: SMD 1206
C5	multilayer ceramic chip capacitor	2.4 pF	Murata: SMD 0603
C6	multilayer ceramic chip capacitor	4.3 pF	Murata: SMD 0805
C7	multilayer ceramic chip capacitor	2.4 pF	Murata: SMD 0805
FB1	resistor	30 Ω	Murata: BLE32PN300SN1L
R1	resistor	5.1 Ω	Multicomp: SMD 0603
R2	resistor	15 kΩ	Multicomp: SMD 0603
R3	resistor	825 Ω	Multicomp: SMD 0603
TM1	resistor	50 Ω	Multicomp: SMD 0603
X1	Hybrid coupler	2 dB	Anaren: X3C20F1-02S

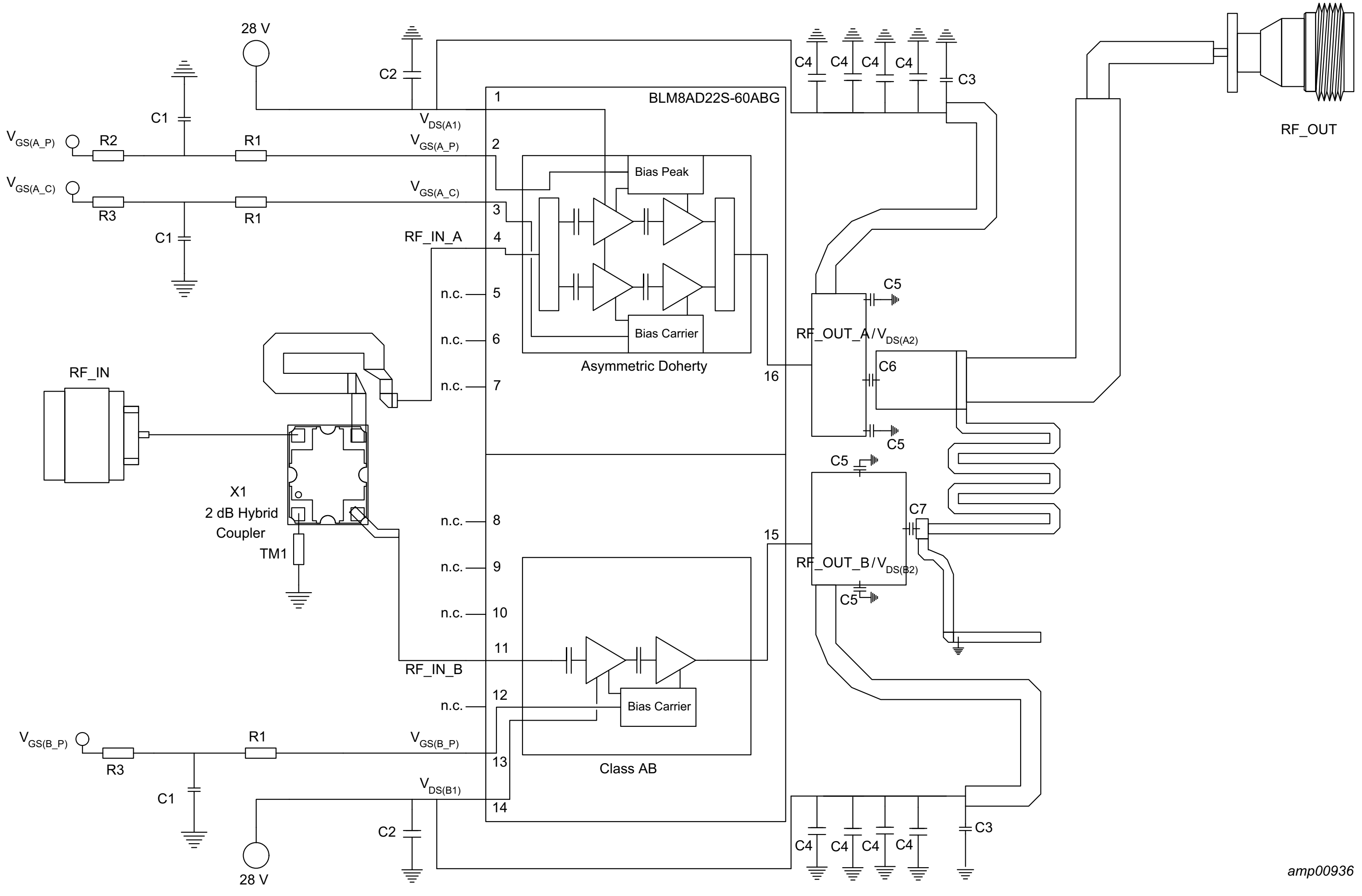


Fig 3. Electrical schematic

7.1 Ruggedness

The BLM8AD22S-60ABG is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 90 mA (carrier section A); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.45$ V (section A); I_{Dq} = 110 mA (section B); P_i corresponding to $P_{L(5dB)}$ OBO under Z_S = 50 Ω load; f = 2170 MHz (1-carrier W-CDMA; PAR = 9.9 dB); T_{case} = 25 °C per section unless otherwise specified.

7.2 Impedance information

Table 10. Typical impedance for optimum Doherty operation (section A)
Measured load-pull data; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 90 mA (carrier); $V_{GSq(peaking)} = V_{GSq(carrier)} - 0.45$ V; Z_S = 50 Ω; t_p = 100 μs; δ = 10 %. Typical values unless otherwise specified.

	tuned for optimum Doherty operation				
f	Z_L	$G_{p(max)}$	P_L	η_{add} [1]	η_{add} [2]
(MHz)	(Ω)	(dB)	(dBm)	(%)	(%)
Section A					
2110	2.70 – j6.46	30.28	46.79	49.7	46.7
2140	2.69 – j6.42	29.85	46.68	50.6	46.5
2170	3.19 – j6.58	29.66	46.50	50.9	46.2

[1] at 3 dB compression point.

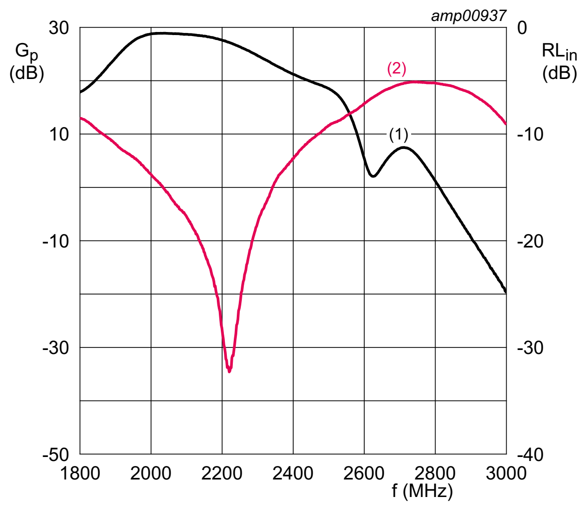
[2] at 38.5 dBm (nearly 8 dB OBO point).

Table 11. Typical impedance (section B)
Measured load-pull data at 3 dB gain compression point; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 110 mA; Z_S = 50 Ω; t_p = 100 μs; δ = 10 %. Typical values unless otherwise specified

f	tuned for maximum output power					tuned for maximum drain efficiency				
	Z_L	$G_{p(max)}$	P_L	η_D	AM/PM [1]	Z_L	$G_{p(max)}$	P_L	η_D	AM/PM [1]
(MHz)	(Ω)	(dB)	(dBm)	(%)	(°)	(Ω)	(dB)	(dBm)	(%)	(°)
Section B										
2110	5.46 – j3.02	33.98	42.31	55	–2.5	3.32 – j1.25	35.85	41.18	61.1	–6.9
2140	6.20 – j3.28	33.48	42.27	53	–1.7	3.87 – j1.43	35.40	41.47	60.4	–5.1
2170	6.25 – j3.27	33.37	42.25	53.1	–1.8	3.30 – j1.22	35.93	40.84	59.7	–5.7

[1] AM/PM conversion.

7.3 Graphs

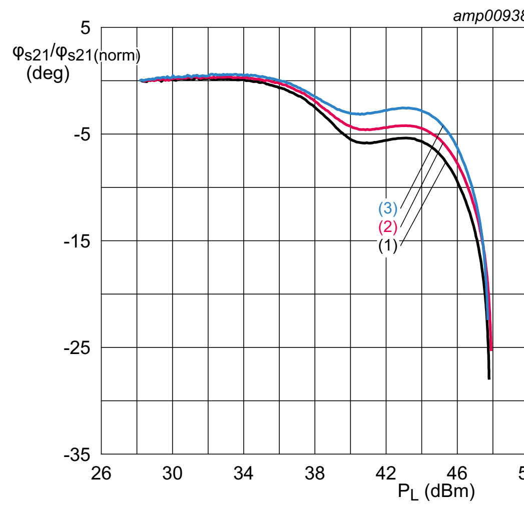


T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
Test signal: CW

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 4. Wideband power gain and input return loss as function of frequency; typical values



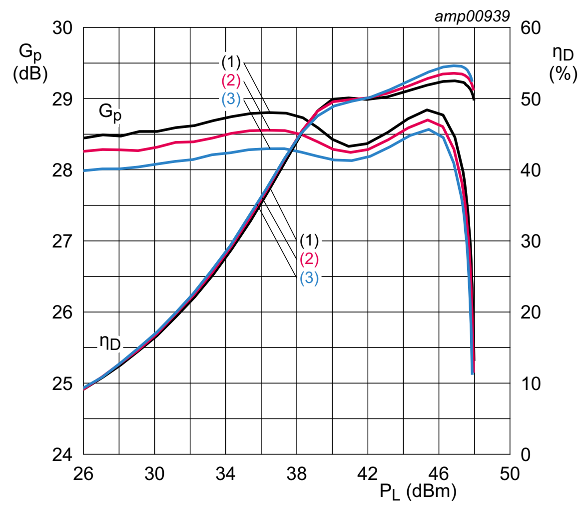
T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
Test signal: 25 ms CW power sweep

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 5. Normalized phase response as a function of output power; typical values



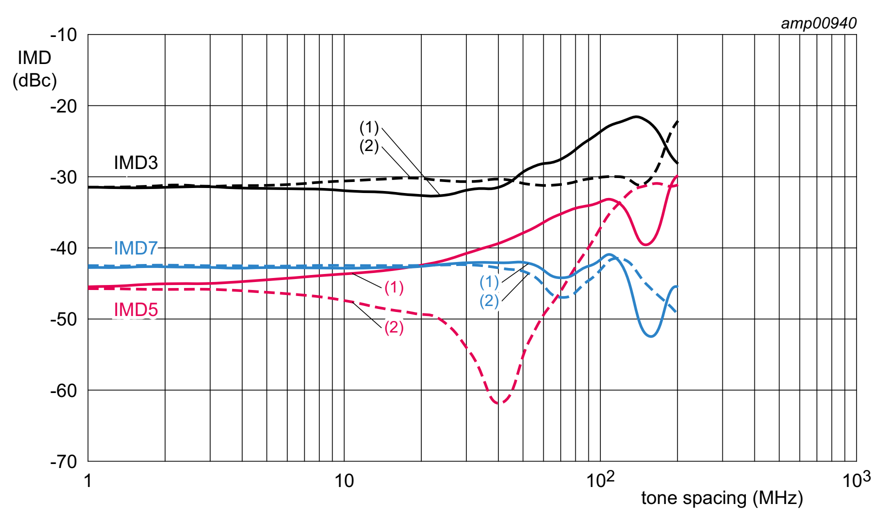
T_{case} = 25 °C; V_{DS} = 28 V;
$I_{Dq1} + I_{Dq2}$ = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
Test signal: pulsed CW power sweep (δ = 10 %; t_p = 100 μs).

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 6. Power gain and drain efficiency as function of output power; typical values

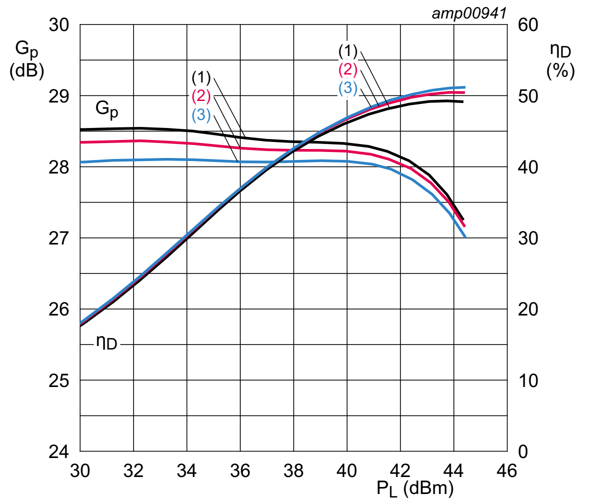


T_{case} = 25 °C; V_{DS} = 28 V; $P_{L(AV)}$ = 6.3 W;
$I_{Dq1} + I_{Dq2}$ = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
Test signal: 2-tone power sweep; f_c = 2140 MHz

(1) IMD low

(2) IMD high

Fig 7. Intermodulation distortion as a function of tone spacing; typical values



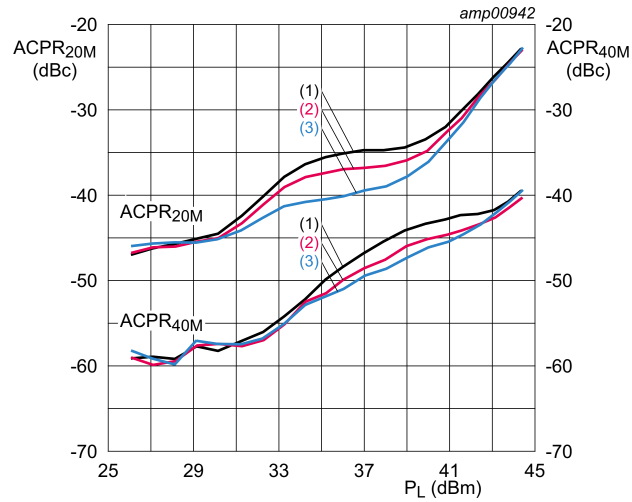
T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
1-carrier LTE; PAR = 7.6 dB at 0.01 % probability CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



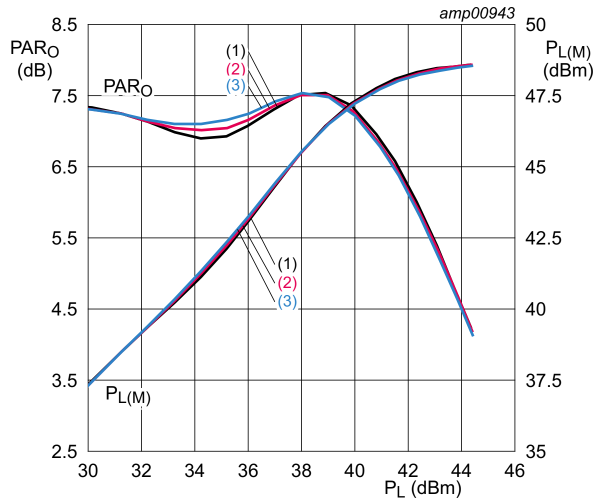
T_{case} = 25 °C; V_{DS} = 28 V;
I_{Dq1} + I_{Dq2} = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
1-carrier LTE; PAR = 7.6 dB at 0.01 % probability CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 9. Adjacent channel power ratio as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 28 V;
$I_{Dq1} + I_{Dq2}$ = 105 mA (carrier and peaking stages);
$V_{GS(carrier)(A)}$ = 2.65 V (carrier stage)
$V_{GS(peak)(A)}$ = 2 V (peaking 1 stage)
$V_{GS(peak)(B)}$ = 1.4 V (peaking 2 stage)
1-carrier LTE; PAR = 7.6 dB at 0.01 % probability CCDF.

(1) f = 2110 MHz

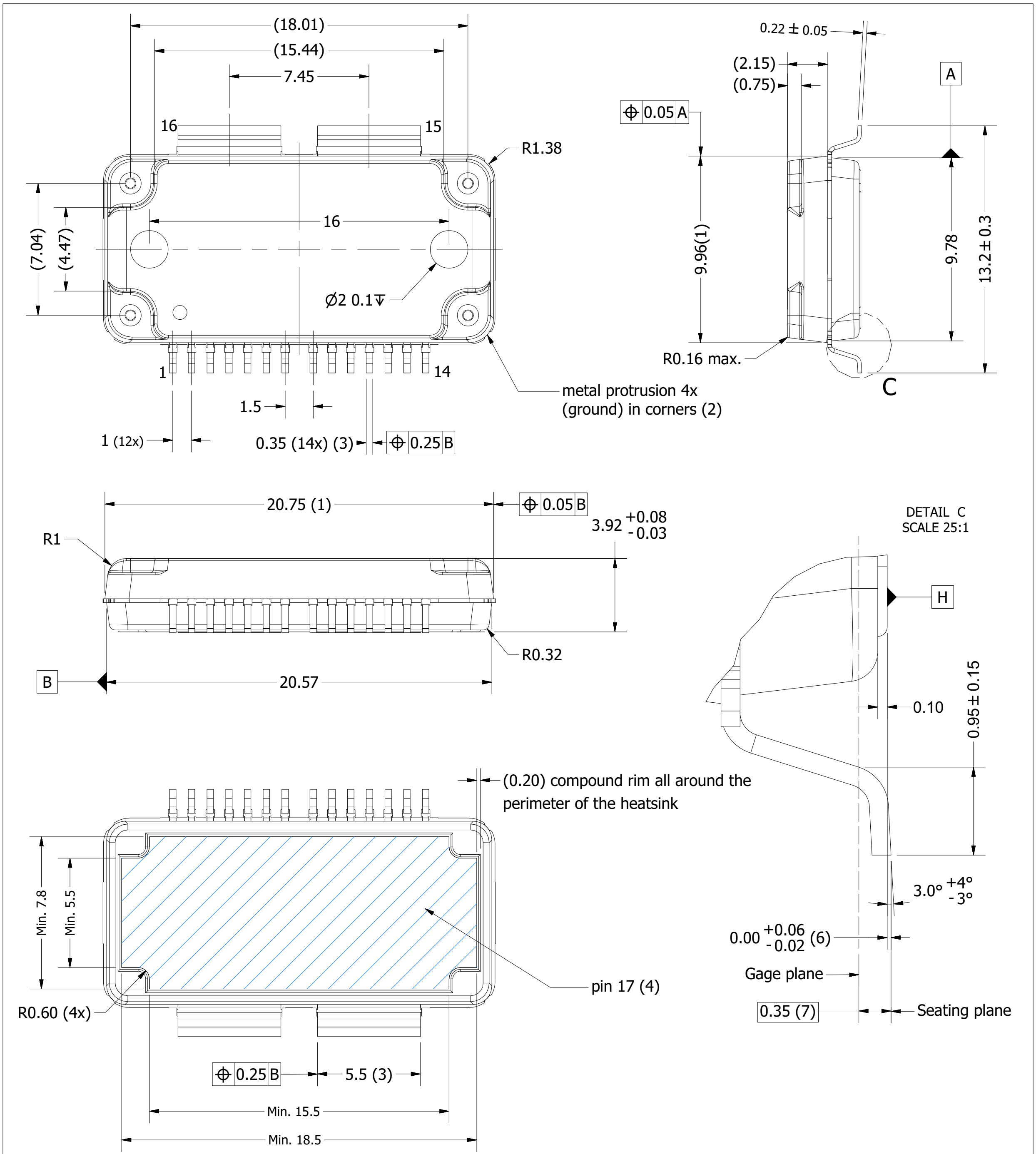
(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 10. Output peak-to-average ratio and peak output power as function of output power; typical values

8. Package outline

OMP-780-16G-1

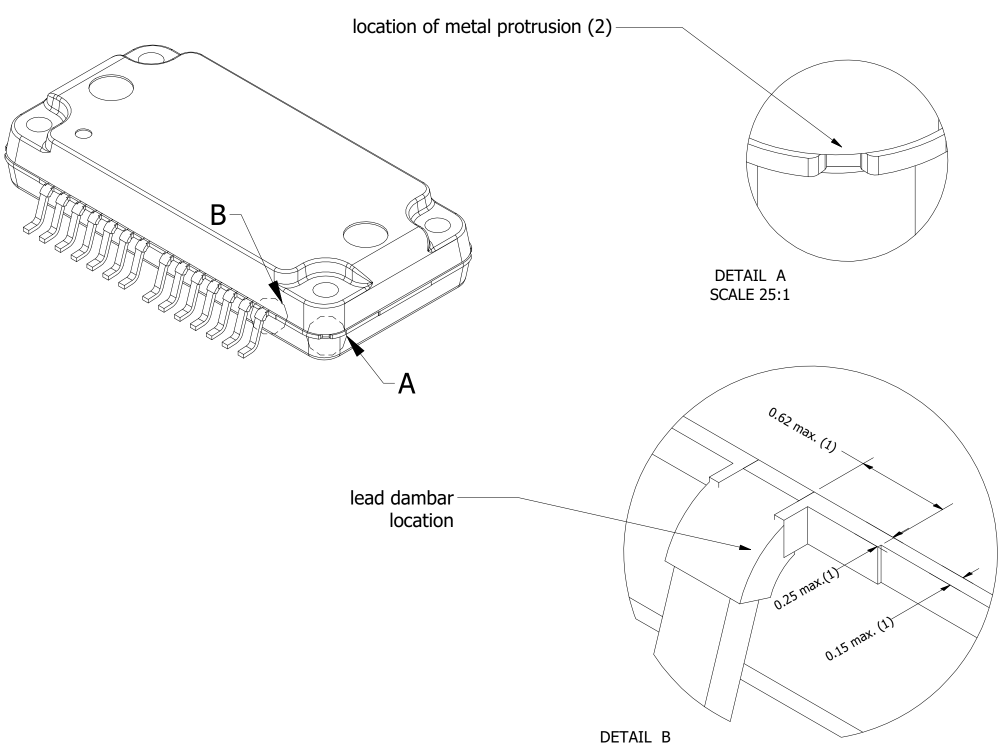


Package outline drawing: OMP-780-16G-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 1 of 2

Fig 11. Package outline OMP-780-16G-1 (sheet 1 of 2)

OMP-780-16G-1

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. In between the 14 leads the protrusion is 0.25 mm max. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The hatched area indicated the exposed heatsink.
(5)	The leads and exposed heatsink are plated with matte Tin (Sn).
(6)	Dimension is measured with respect to the bottom of the heatsink Datum H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.
(7)	Gage plane (foot length) to be measured from the seating plane.



Package outline drawing: OMP-780-16G-1	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 3/1/2018
		Third angle projection	Sheet 2 of 2

Fig 12. Package outline OMP-780-16G-1 (sheet 2 of 2)

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 12. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A [2]

[1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V.

[2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V.

10. Abbreviations

Table 13. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
ESD	ElectroStatic Discharge
GEN8	Eighth Generation
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM8AD22S-60ABG v.2	20190411	Product data sheet	-	BLM8AD22S-60ABG v.1
Modifications	• Table 1 on page 1: table updated • Table 5 on page 3: table updated • Table 6 on page 4: table updated • Table 7 on page 4: table updated • Table 8 on page 5: table updated • Table 9 on page 6: table updated • Figure 3 on page 7: figure added • Section 7.1 on page 8: section title changed • Table 10 on page 8: table updated • Table 11 on page 8: table added • Section 7.3 on page 9: section added			
BLM8AD22S-60ABG v.1	20181214	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Ampleon does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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13. Contact information

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