

# InnoSwitch3-AQ INN3977CQ

CV/CC QR Flyback Switcher IC with Integrated 750 V  
MOSFET and FluxLink Feedback for Automotive Applications

## Product Highlights

### Highly Integrated, Compact Footprint

- Up to 90% efficiency across full load range
- Incorporates a multi-mode Quasi-Resonant (QR) / CCM flyback controller, 750 V MOSFET and secondary-side sensing
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Wide input voltage 30 VDC to 550 VDC
- Wide input voltage 30 VDC to 921 VDC with StackFET
- AEC-Q100 qualified
- Fab, assembly and test site are IATF16949 certified

### EcoSmart™ – Energy Efficient

- Less than 15 mW no-load including line sense
- Easily meets all global energy efficiency regulations
- Low heat dissipation

### Advanced Protection / Safety Features

- Auto-restart fault response for output OVP

### Optional Features

- Auto-restart output UV protection with option for peak power delivery

### Full Safety and Regulatory Compliance

- Reinforced isolation
- Isolation voltage >4000 VAC
- 100% production HIPOT testing
- UL1577 and TUV (EN60950) safety approved
- Excellent noise immunity enables designs that achieve class "A" performance criteria for EN61000-4 suite; EN61000-4-2, 4-3 (30 V/m), 4-4, 4-5, 4-6, 4-8 (100 A/m) and 4-9 (1000 A/m), FMC1278 (RI-115)

### Green Package

- Halogen free and RoHS compliant

### Applications

- Auxiliary, standby and bias power supplies for automotive used in traction inverter, DC-DC converter and on-board charger

### Description

The InnoSwitch™3-AQ family of ICs dramatically simplifies the design and manufacture of flyback power converters, particularly those requiring high efficiency and/or compact size. The InnoSwitch3-AQ family combines primary and secondary controllers and safety-rated feedback into a single IC allowing accurate output voltage regulation even with wide input voltage range of 30 VDC to 550 VDC.

InnoSwitch3-AQ family devices incorporate multiple protection features including line over and undervoltage protection, output overvoltage and over-current limiting, and over-temperature shutdown for automotive applications. Devices are available with standard and peak power delivery options, and commonly used auto-restart protection behaviors.

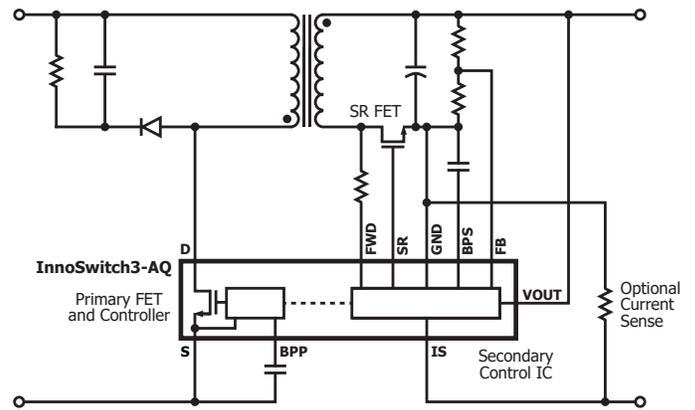


Figure 1. Typical Application Schematic.

PI-8184a-031320



Figure 2. High Creepage, Safety-Compliant InSOP-24D Package.

## Output Power Table

Product <sup>2</sup>	30 VDC <sub>MIN</sub>	60 VDC <sub>MIN</sub>	400 V
	Output Power <sup>1</sup>	Output Power <sup>1</sup>	Output Power <sup>1</sup>
<b>INN3977CQ</b>	10 W	20 W	30 W

Table 1. Output Power Table.

Notes:

1. Max output power is dependent on the design. With condition that package temperature must be < 125 °C.
2. Package: InSOP-24D.

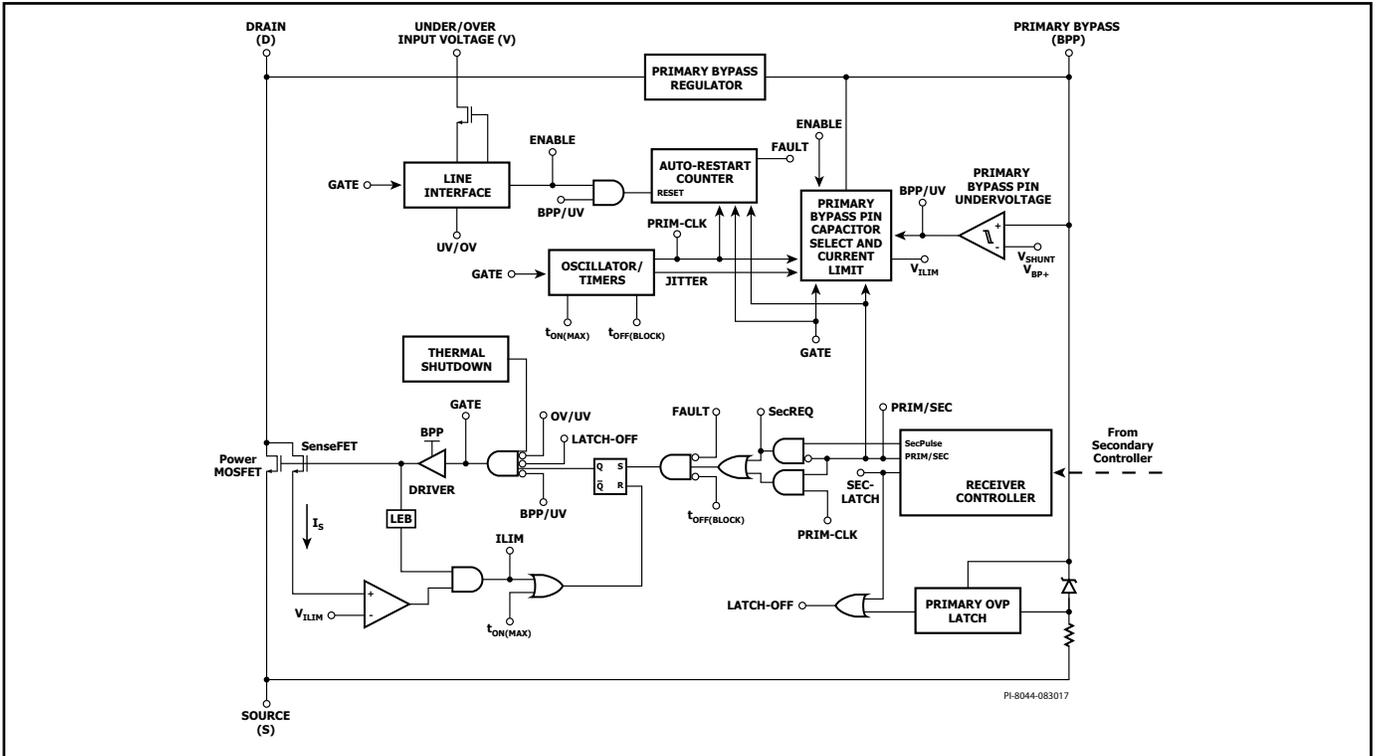


Figure 3. Primary Controller Block Diagram.

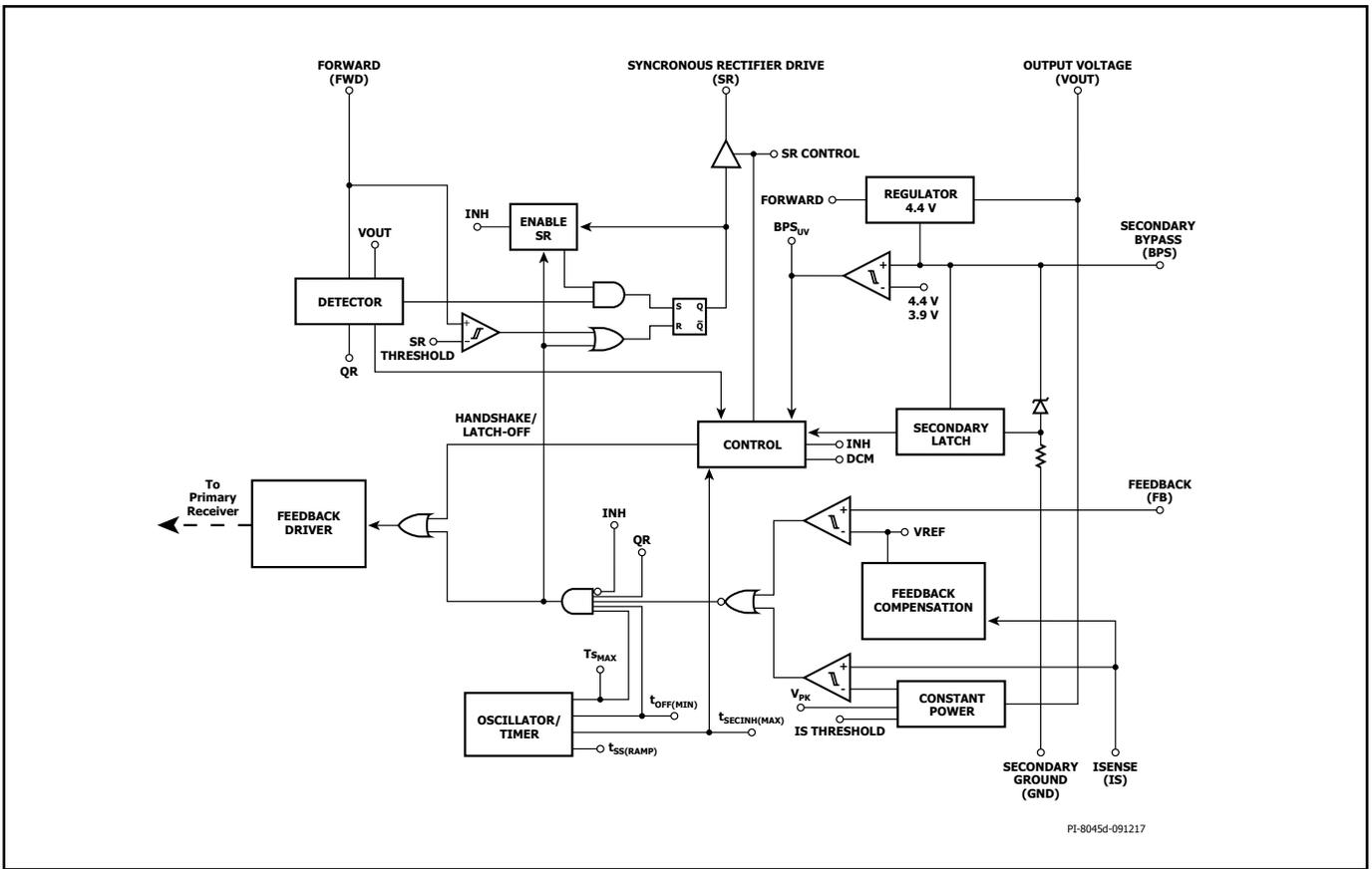


Figure 4. Secondary Controller Block Diagram.

## Pin Functional Description

### Secondary-Side Pins

#### ISENSE (IS) Pin (Pin 1)

Connection to the power supply output terminals. An external current sense resistor should be connected between this and the GND pin. If current regulation is not required, this pin should be tied to the GND pin.

#### SECONDARY GROUND (GND) (Pin 2)

GND for the secondary IC. Note this is not the power supply output GND due to the presence of the sense resistor between this and the ISENSE pin.

#### FEEDBACK (FB) Pin (Pin 3)

Connection to an external resistor divider to set the power supply output voltage.

#### SECONDARY BYPASS (BPS) Pin (Pin 4)

Connection point for an external bypass capacitor for the secondary IC supply.

#### SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 5)

Gate driver for external SR FET. If no SR FET is used connect this pin to GND.

#### OUTPUT VOLTAGE (VOUT) Pin (Pin 6)

Connected directly to the output voltage, to provide current for the controller on the secondary-side and provide secondary protection.

#### FORWARD (FWD) Pin (Pin 7)

The connection point to the switching node of the transformer output winding providing information on primary switch timing. Provides power for the secondary-side controller when  $V_{OUT}$  is below threshold.

#### NC Pin (Pin 8-12)

Leave open. Should not be connected to any other pins.

### Primary-Side Pins

#### UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 13)

A high-voltage pin connected to the high input DC voltage for detecting undervoltage and overvoltage conditions through a series resistors. This pin should be tied to SOURCE pin to disable UV/OV protection.

#### PRIMARY BYPASS (BPP) Pin (Pin 14)

The connection point for an external bypass capacitor for the primary-side supply. This is also the ILIM selection pin for choosing standard ILIM or ILIM+1.

#### NC Pin (Pin 15)

Leave open. Should not be connected to any other pins.

#### SOURCE (S) Pin (Pin 16-19)

This pin is the power MOSFET source connection. Also ground reference for primary BYPASS pin.

#### DRAIN (D) Pin (Pin 24)

Power MOSFET drain connection.

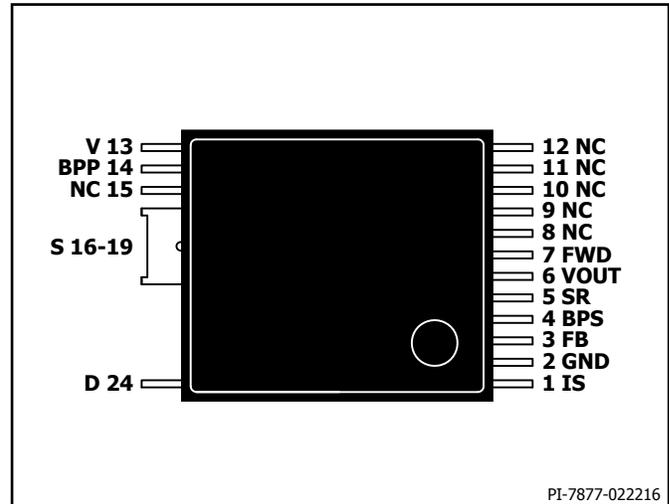


Figure 5. Pin Configuration.

## InnoSwitch3-AQ Functional Description

The InnoSwitch3-AQ combines a high-voltage power MOSFET switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The primary controller on InnoSwitch3-AQ is a Quasi-Resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM), boundary mode (CrM) and discontinuous conduction mode (DCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass overvoltage detection circuit, current limit selection circuitry, over-temperature protection, leading edge blanking and a 750 V power MOSFET.

The InnoSwitch3-AQ secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the SECONDARY BYPASS pin, QR mode circuit, oscillator and timing circuit, and numerous integrated protection features.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller, highlighting the most important features.

## Primary Controller

InnoSwitch3-AQ has variable frequency QR controller plus CCM/CRM/DCM operation for enhanced efficiency and extended output power capability.

### PRIMARY BYPASS Pin Regulator

The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to  $V_{BPP}$  by drawing current from the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to  $V_{SHUNT}$  when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch3-AQ to be powered externally through a bias winding, decreasing the no-load consumption to less than 15 mW.

### Primary Bypass ILIM Programming

InnoSwitch3-AQ ICs allows the user to adjust current limit (ILIM) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes - 0.47  $\mu$ F and 4.7  $\mu$ F for setting standard and increased ILIM settings respectively.

### Primary Bypass Undervoltage Threshold

The PRIMARY BYPASS pin undervoltage circuitry disables the power MOSFET when the PRIMARY BYPASS pin voltage drops below  $\sim 4.5$  V ( $V_{BPP} - V_{BP(H)}$ ) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to  $V_{SHUNT}$  to re-enable turn-on of the power MOSFET.

### Primary Bypass Output Overvoltage Function

The PRIMARY BYPASS pin has a latching OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds  $I_{SD}$ , the device will latch-off or disable the power MOSFET switching for a time  $t_{AR(OFF)}$  after which time the controller will restart and attempt to return to regulation.

VOUT OV protection is also included as an integrated feature on the secondary controller (see Output Voltage Protection).

### Over-Temperature Protection

The thermal shutdown circuitry senses the primary MOSFET die temperature. The threshold is set to  $T_{SD}$  with either a hysteretic or latch-off response.

**Hysteretic response:** If the die temperature rises above the threshold, the power MOSFET is disabled and remains disabled until the die temperature falls by  $T_{SD(H)}$  at which point switching is re-enabled. A large amount of hysteresis is provided to prevent overheating of the PCB due to a continuous fault condition.

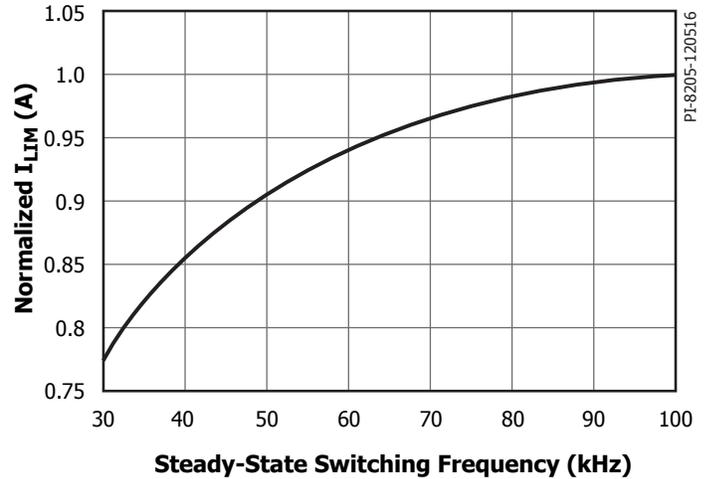


Figure 6. Normalized Primary Current vs. Frequency.

### Current Limit Operation

The primary-side controller has a current limit threshold ramp that is linearly decreasing to the time from the end of the previous primary switching cycle (i.e. from the time the primary MOSFET turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100%  $I_{LIM}$ . This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

### Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of  $f_M$ . This results in a frequency jitter of  $\sim 7$  kHz with average frequency of  $\sim 100$  kHz.

### Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch3-AQ enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below  $\sim 3$  V.

In auto-restart, switching of the power MOSFET is disabled for  $t_{AR(OFF)}$ . There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency  $f_{OVL}$  ( $\sim 110$  kHz) for longer than 82 ms ( $t_{AR}$ ).
2. No requests for switching cycles from the secondary for  $> t_{AR(SK)}$ .

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

**SOA Protection**

In the event that there are two consecutive cycles where the  $I_{LIM}$  is reached within  $\sim 500$  ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or  $\sim 25 \mu s$  (based on full frequency of 100 kHz). This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

**Input Line Voltage Monitoring**

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A 4 MΩ resistor is tied between the high-voltage DC bulk capacitor and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to SOURCE pin.

At power-up, after the primary bypass capacitor is charged and the ILIM state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-in for longer than  $t_{UV,r}$ , the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of an internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time  $t_{OFF}$  is greater than 50 ms, the internal high-voltage MOSFET will disconnect the external 4 MW resistor from the internal IC to eliminate current drawn through the 4 MW resistor. The line sensing function will activate again at the beginning of the next switching cycle.

**Primary-Secondary Handshake**

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time ( $t_{AR}$ ), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards the secondary controls switching.

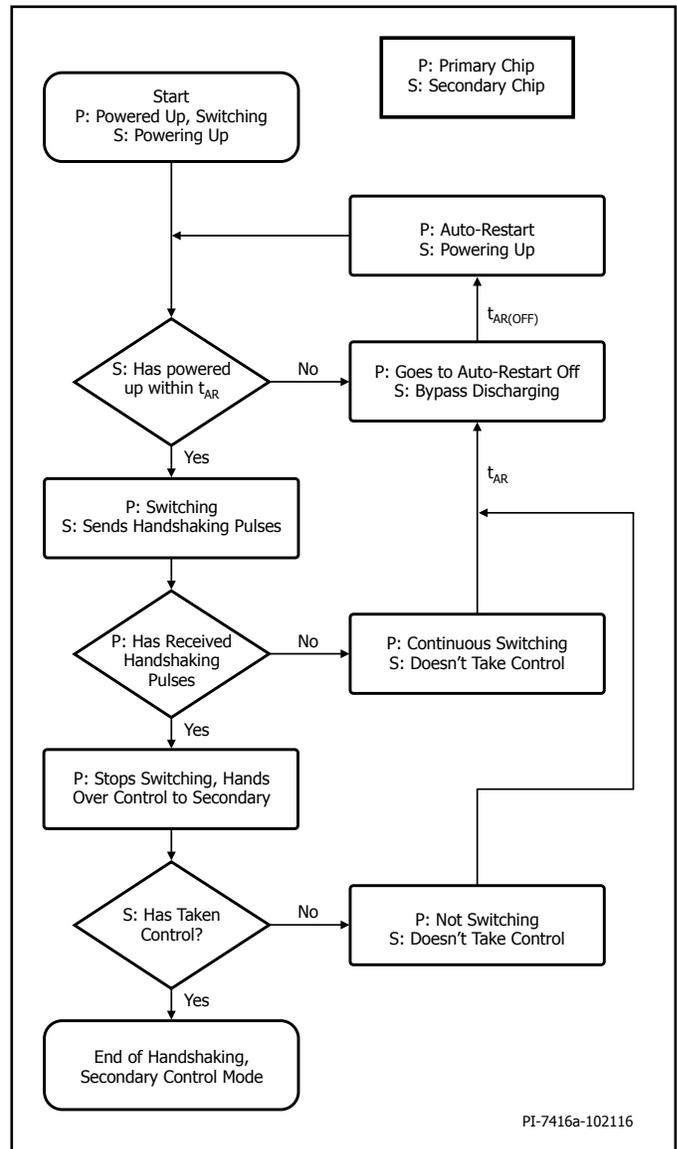


Figure 7. Primary-Secondary Handshake Flowchart.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If the secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

### Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period,  $t_{AR}$  (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30  $\mu$ s, the primary will infer secondary control and begin switching in slave mode. If no pulses occurs during the  $t_{AR}$  "wait" period, the primary will begin switching under primary control until handshake pulses are received.

### Audible Noise Reduction Engine

The InnoSwitch3-AQ features an active audible noise reduction mode whereby the controller (via a "frequency skipping" mode of operation) avoids the resonant band (where the mechanical structure of the power supply is most likely to resonate – increasing noise amplitude) between 7 kHz and 12 kHz - 143  $\mu$ s and 83  $\mu$ s. If a secondary controller switch request occurs within this time window from the last conduction cycle, the gate drive to the power MOSFET is inhibited.

### Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered by a 4.4 V ( $V_{BPS}$ ) regulator which is supplied by either VOUT or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing.

The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is  $V_{FB}$  (1.265 V).

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

### Minimum Off-Time

The secondary controller initiates a cycle request using the inductive-connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of  $t_{OFF(MIN)}$ . This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

### Maximum Switching Frequency

The maximum switch-request frequency of the secondary controller is  $f_{SREQ}$ .

### Frequency Soft-Start

At start-up the primary controller is limited to a maximum switching frequency of  $f_{SW}$  and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

The secondary controller temporarily inhibits the FEEDBACK short protection threshold ( $V_{FB(OFF)}$ ) until the end of the soft-start ( $t_{SS(RAMP)}$ ) time. After hand-shake is completed the secondary controller linearly ramps up the switching frequency from  $f_{SW}$  to  $f_{SREQ}$  over the  $t_{SS(RAMP)}$  time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the  $V_{FB(AR)}$  threshold before the expiration of the soft-start timer ( $t_{SS(RAMP)}$ ) after handshake has occurred.

The secondary controller enables the FEEDBACK pin-short protection mode ( $V_{FB(OFF)}$ ) at the end of the  $t_{SS(RAMP)}$  time period. If the output short maintains the FEEDBACK pin below the short-circuit threshold, the secondary will stop requesting pulses triggering an auto-restart cycle.

If the output voltage reaches regulation within the  $t_{SS(RAMP)}$  time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

### Maximum Secondary Inhibit Period

Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30  $\mu$ s.

### Output Voltage Protection

In the event that the sensed voltage on the FEEDBACK pin is 2% higher than the regulation threshold, a bleed current of ~2.5 mA (3 mA max) is applied on the OUTPUT VOLTAGE pin (weak bleed). This bleed current increases to ~200 mA (strong bleed) in the event that the FEEDBACK pin voltage is raised beyond ~10% of the internal FEEDBACK pin reference voltage. The current sink on the OUTPUT VOLTAGE pin is intended to discharge the output voltage after momentary overshoot events. The secondary does not relinquish control to the primary during this mode of operation.

If the voltage on the FEEDBACK pin is sensed to be 20% higher than the regulation threshold, a command is sent to the primary to either latch-off or begin an auto-restart sequence (see Secondary Fault Response in Feature Code Addendum). This integrated  $V_{OUT}$  OVP can be used independently from the primary sensed OVP or in conjunction.

### FEEDBACK Pin Short Detection

If the sensed FEEDBACK pin voltage is below  $V_{FB(OFF)}$  at start-up, the secondary controller will complete the handshake to take control of the primary complete  $t_{SS(RAMP)}$  and will stop requesting cycles to initiate auto-restart (no cycle requests made to primary for longer than  $t_{AR(SK)}$  second triggers auto-restart).

During normal operation, the secondary will stop requesting pulses from the primary to initiate an auto-restart cycle when the FEEDBACK pin voltage falls below the  $V_{FB(OFF)}$  threshold. The deglitch filter on the protection mode is on for less than  $\sim 10 \mu s$ . By this mechanism, the secondary will relinquish control after detecting that the FEEDBACK pin is shorted to ground.

**Auto-Restart Thresholds**

The OUTPUT VOLTAGE pin includes a comparator to detect when the output voltage falls below  $V_{FB(AR)}$  or  $V_{VO(AR)}$  for a duration exceeding  $t_{FB(AR)}$  or  $t_{VO(AR)}$  respectively. The secondary controller will relinquish control when this fault condition is detected. This threshold is meant to limit the range of constant current (CC) operation and is included to support high power charger applications.

**SECONDARY BYPASS Pin Overvoltage Protection**

The InnoSwitch3-AQ secondary controller features a SECONDARY BYPASS pin OV feature similar to the PRIMARY BYPASS pin OV feature. When the secondary is in control, in the event that the SECONDARY BYPASS pin current exceeds  $I_{BPS(SD)}$  ( $\sim 7 \text{ mA}$ ) the secondary will send a command to the primary to initiate an auto-restart off-time ( $t_{AR(OFF)}$ ).

**Output Constant Current**

The InnoSwitch3-AQ regulates the output current through an external current sense resistor between the ISENSE and SECONDARY GROUND pins and also controls output power in conjunction with the output voltage sensed on the OUTPUT VOLTAGE pin. If constant

current regulation is not required, the ISENSE pin must be tied to the SECONDARY GROUND pin.

**Intelligent Quasi-Resonant Mode Switching**

In order to improve conversion efficiency and reduce switching losses, the InnoSwitch3-AQ features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous-conduction mode (CCM).

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power MOSFET.

Quasi-Resonant (QR) mode is enabled for  $20 \mu s$  after DCM is detected or when ring amplitude (pk-pk)  $> 2 \text{ V}$ . Afterwards, QR switching is disabled, at which point switching may occur at any time a secondary request is initiated.

The secondary controller includes blanking of  $\sim 1 \mu s$  to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground. See Figure 8.

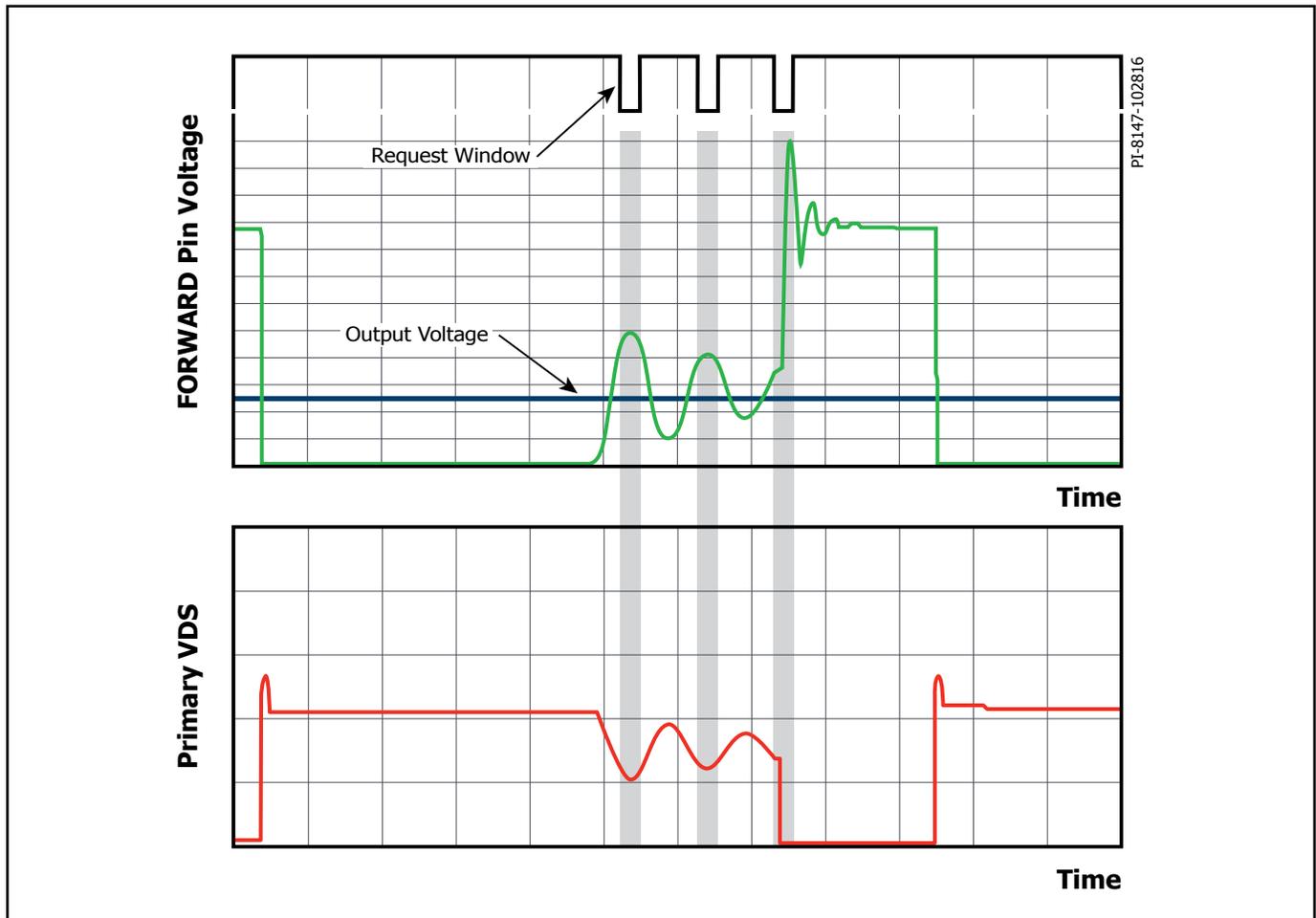


Figure 8. Intelligent Quasi-Resonant Mode Switching.

### **SR Disable Protection**

In each cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

### **SR Static Pull-Down**

To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has a nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

### **Open SR Protection**

In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is

connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below 100 pF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above 100 pF, the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.



## Key Application Considerations

### Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 130 VDC or higher for full power
2. Efficiency assumptions depend on power level. The power level assumes efficiency > 89 %
3. Transformer primary inductance tolerance of  $\pm 10\%$ .
4. Maximum conduction losses is limited to 0.8 W.
5. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 125 °C.
6. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient
7. Below a value of 1,  $K_p$  is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient  $K_p$  limit of  $\geq 0.25$  is recommended. This prevents the initial current limit ( $I_{INT}$ ) from being exceeded at switch turn-on.

### Primary-Side Overvoltage Protection

Primary-side output overvoltage protection provided by the INN3977CQ IC uses an internal protection that is triggered by a threshold current of  $I_{SD}$  into the PRIMARY BYPASS pin. In addition to an internal filter, the PRIMARY BYPASS pin capacitor forms an external filter helping noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and PRIMARY BYPASS pins of the device.

The primary sensed OVP function can be realized by connecting a series combination of a Zener diode, a resistor and a blocking diode from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The rectified and filtered bias winding output voltage may be higher than expected (up to 1.5X or 2X the desired value) due to poor coupling of the bias winding with the output winding and the resulting ringing on the bias winding voltage waveform. It is therefore recommended that the rectified bias winding voltage be measured. This measurement should be ideally done at the lowest input voltage and with highest load on the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. It is recommended that a Zener diode with a clamping voltage approximately 6 V lower than the bias winding rectified voltage at which OVP is expected to be triggered be selected. A forward voltage drop of 1 V can be assumed for the blocking diode. A small signal standard recovery diode is recommended. The blocking diode prevents any reverse current discharging the bias capacitor during start-up. Finally, the value of the series resistor required can be calculated such that a current higher than  $I_{SD}$  will flow into the PRIMARY BYPASS pin during an output overvoltage.

### Reducing No-load Consumption

The InnoSwitch3-AQ IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. Use of a bias winding is however required to provide supply current to the PRIMARY BYPASS pin once the InnoSwitch3-AQ IC has started switching. An auxiliary (bias) winding provided on the transformer serves this purpose. A bias winding driver supply to the PRIMARY BYPASS pin enables design of power supplies with no-load power consumption less than 10 mW. Resistor R4 shown in Figure 9 should be adjusted to achieve the lowest no-load input power.

## Secondary-Side Overvoltage Protection (Auto-Restart Mode)

The secondary-side output overvoltage protection provided by the InnoSwitch3-AQ IC uses an internal auto restart circuit that is triggered by an input current exceeding a threshold of  $IBPS(SD)$  into the SECONDARY BYPASS pin. The direct output sensed OVP function can be realized by connecting a Zener diode from the output to the SECONDARY BYPASS pin. The Zener diode voltage needs to be the difference between  $1.25 \times V_{OUT}$  and 4.4 V - the SECONDARY BYPASS pin voltage. It is necessary to add a low value resistor in series with the OVP Zener diode to limit the maximum current into the SECONDARY BYPASS pin.

## Selection of Components

### Components for InnoSwitch3-AQ Primary-Side Circuit

#### BPP Capacitor

A capacitor connected from the PRIMARY BYPASS pin of the InnoSwitch3-AQ IC to GND provides decoupling for the primary-side controller and also selects current limit. A 0.47  $\mu F$  or 4.7  $\mu F$  capacitor may be used. Though electrolytic capacitors can be used, often surface mount multi-layer ceramic capacitors are preferred for use on double sided boards as they enable placement of capacitors close to the IC. Their small size also makes it ideal for compact power supplies. At least 10 V, 0805 or larger size rated X5R or X7R dielectric capacitors are recommended to ensure that minimum capacitance requirements are met. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC due to this type of SMD ceramic capacitor has very poor voltage and temperature coefficient characteristics.

#### Bias Winding and External Bias Circuit

The internal regulator connected from the DRAIN pin of the switch to the PRIMARY BYPASS pin of the InnoSwitch3-AQ primary-side controller charges the capacitor connected to the PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply at least 1 mA of current to the PRIMARY BYPASS pin. The turns ratio for the bias winding should be selected such that 7 V is developed across the bias winding at the lowest rated output voltage of the power supply at the lowest load condition. If the voltage is lower than this, no-load input power will increase.

The bias current from the external circuit should be set to approximately  $I_{SI(MAX)}$  to achieve lowest no-load power consumption when operating the power supply at 400 VDC input, ( $V_{BPP} > 5 V$ ). A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes. An ceramic capacitor of at least 22  $\mu F$  with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. Highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input DC supply voltage.

#### Primary Sensed OVP (Overvoltage Protection)

The voltage developed across the output of the bias winding tracks the power supply output voltage. Though not precise, a reasonably accurate detection of the amplitude of the output voltage can be

achieved by the primary-side controller using the bias winding voltage. A Zener diode connected from the bias winding output to the PRIMARY BYPASS pin can reliably detect a secondary overvoltage fault and cause the primary-side controller to latch-off/auto-restart depending on H code. It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions (at full load and lowest input voltage) and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will only operate in case of a fault.

**Primary-Side Snubber Clamp**

A snubber circuit should be used on the primary-side as shown in Figure 9. This prevents excess voltage spikes at the drain of the switch at the instant of turn-off of the switch during each switching cycle though conventional RCD clamps can be used. RCDZ clamps offer the highest efficiency. The circuit example shown in Figure 9 uses an RCD clamp with a resistor in series with the clamp diode. This resistor dampens the ringing at the drain and also limits the reverse current through the clamp diode during reverse recovery. Standard recovery glass passivated diodes with low junction capacitance are recommended as these enable partial energy recovery from the clamp thereby improving efficiency.

**Primary side StackFET configuration for high input voltage (>550 VDC)**

The StackFET circuit configuration, shown in Figure 10, can be used to increase the breakdown voltage in the circuit for the application of very high input voltage, higher than 550 VDC. The effective breakdown voltage of the StackFET circuit is the sum of the breakdown voltage of an external MOSFET and the clamp Zener voltage,  $BV_{DSS} = BV_{DSSSTACKFET} + V_{ZCLAMP}$ . The maximum breakdown voltage of TVS diode,  $V_{ZCLAMP}$  will be 600 V, which is 80% of 750 V breakdown voltage of INN3977CQ. If the turn-off voltage  $V_{TURN-OFF}$  which is  $V_{OR} + V_{IN} + V_{LEAKAGE}$  is less than the breakdown voltage of  $V_{ZCLAMP}$  most of the turn-off voltage will be on the internal MOSFET in INN3977CQ. In case of  $V_{TURN-OFF} > V_{BR}$  of  $V_{ZCLAMP}$  the difference of turn-off voltage and breakdown voltage of  $V_{ZCLAMP}$  will be shown across the drain to source of StackFET,  $V_{DSSTACKFET} = V_{TURN-OFF} - V_{BR}$ .

When high DC input voltage applied, the BPP capacitor,  $C_{BPP}$  will be charged by the current through the gate resistor,  $R_{GATE}$  to initiate the switching of INN3977CQ. The source voltage of the StackFET will be low when the MOSFET in the INN3977CQ turns on, and the stackFET starts to conduct due to the potential difference appearing between its gate and source.  $V_{ZGS}$  is a 15 V zener diode, which ensures the maximum gate-source voltage of external MOSFET does not exceed the maximum gate to source voltage of MOSFET. 2 MΩ, 0.5 W resistor is recommended to use for the gate resistor,  $R_{GATE}$  to provide the adequate start up charge for the gate of StackFET and high voltage rating. Once the converter is operating, the StackFET gate is largely driven by the charge stored in the capacitance of  $V_{ZCLAMP}$ . If the junction capacitance of  $V_{ZCLAMP}$  is not large enough to drive the StackFET gate, it is necessary to add a small capacitor, < 30 pF, in parallel with  $V_{ZCLAMP}$  diode. The leakage inductance energy of transformer will be clamped by  $D_{SN}$  with  $R_{SN}$  and  $C_{SN}$ .

**Components for InnoSwitch3-AQ Secondary-Side Circuit**

**SECONDARY BYPASS Pin – Decoupling Capacitor**

A 2.2 uF, 10 V / X7R or X5R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch3-AQ IC. Since the SECONDARY BYPASS Pin voltage needs to be 4.4 V before the output voltage reaches the regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 μF may not enough capacitance, which can cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V is recommended voltage rating to give enough margin from BPS voltage, and 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCC is not recommended for this reason. The ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.4 V. Capacitors with X5R or X7R dielectrics should be used for best results.

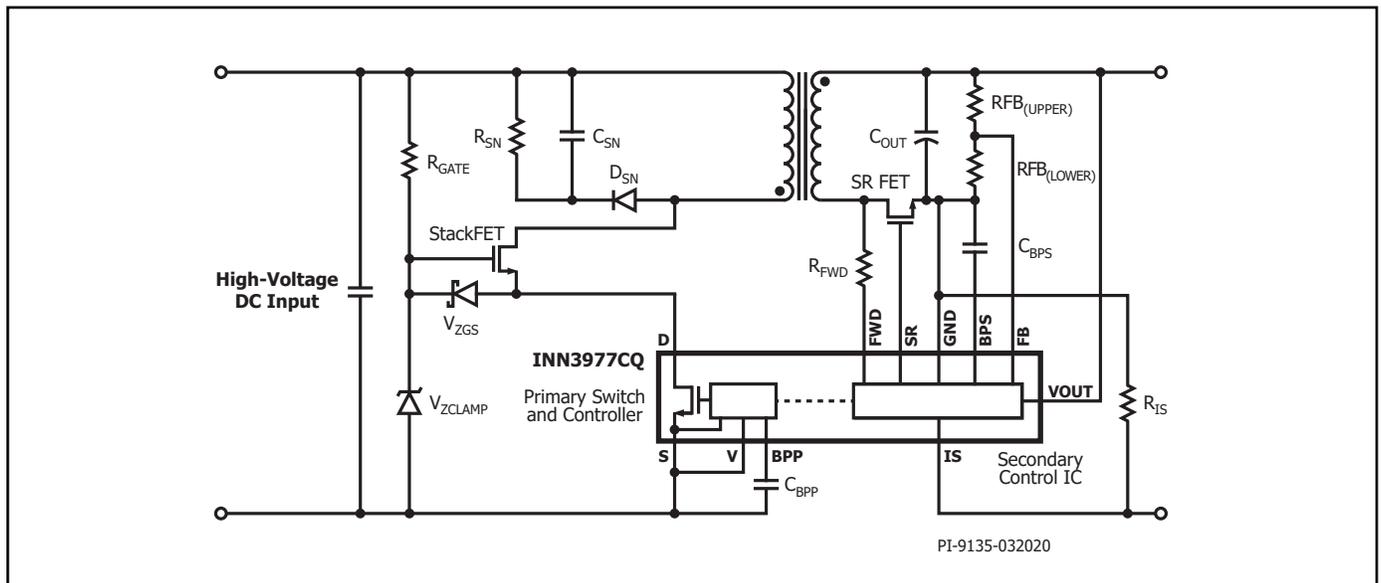


Figure 10. StackFET Circuit Configuration.

## FORWARD Pin Resistor

A resistor in the range of 47 ohms to 100 ohms resistor is recommended to ensure sufficient IC supply current. A higher or lower resistor value should not be used as it can affect device operation such as the timing of the synchronous rectifier drive. Figures 11, 12, 13, and 14 below show examples of unacceptable and acceptable FORWARD pin voltage waveforms.  $V_D$  is forward voltage drop across the SR.

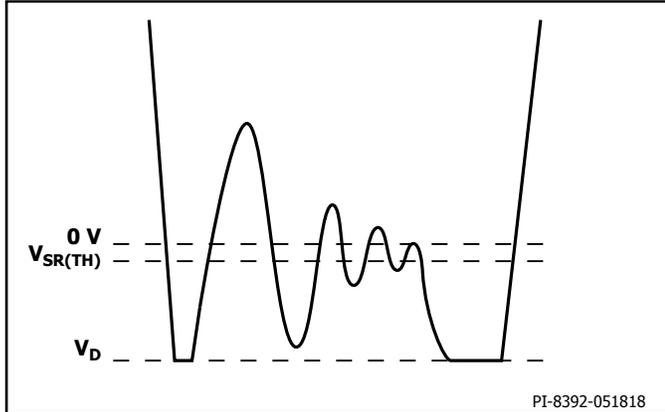


Figure 11. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

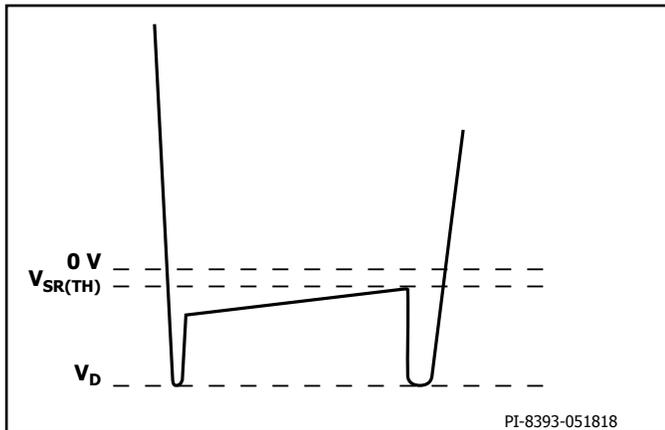


Figure 12. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

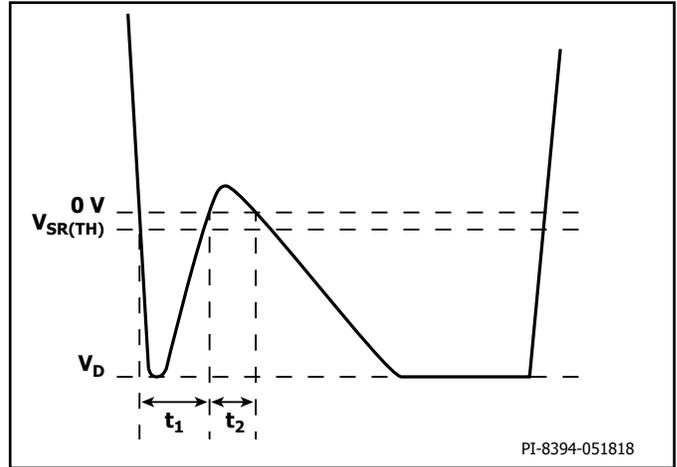


Figure 13. Unacceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

Note:

If  $t_1 + t_2 = 1.5 \mu\text{s} \pm 50 \text{ ns}$ , the controller may fail the handshake and trigger a primary bias winding OVP latch-off/auto-restart.

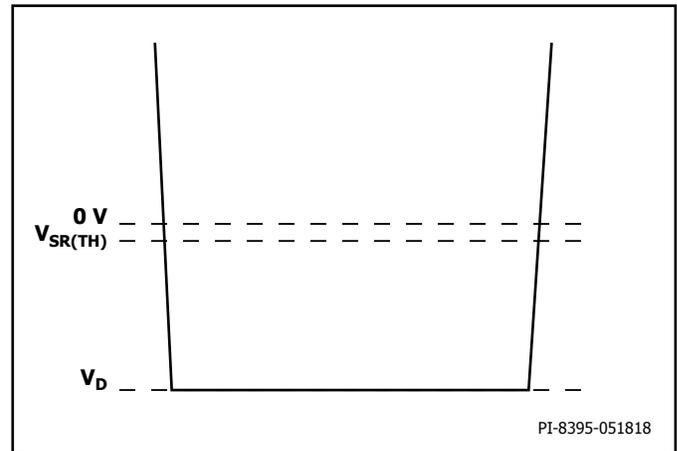


Figure 14. Acceptable FORWARD Pin Waveform before Handshake with Body Diode Conduction During Flyback Cycle.

### SR Switch Operation and Selection

Although a simple diode rectifier and filter works for the output, use of an SR FET enables the significant improvement in operating efficiency. The secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch3-AQ IC (no additional resistors should be connected in the gate circuit of the SR FET). The SR FET is turned off once the voltage  $V_{DS}$  of SR FET reaches 0 V. The SR FET driver uses the SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.4 V. A FET with a high threshold voltage is therefore not suitable. FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although switches with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify  $R_{DS(ON)}$  across temperature for a gate voltage of 4.5 V.

There is a slight delay between the commencement of the flyback cycle and the turn-on of the SR FET. During this time, the body diode of the SR FET conducts. If an external parallel Schottky diode is used, this current mostly flows through the Schottky diode. Once the InnoSwitch3-AQ IC detects end of the flyback cycle, voltage across SR FET  $R_{DS(ON)}$  reaches 0 V, any remaining portion of the flyback cycle is completed with the current commutating to the body diode of the SR FET or the external parallel Schottky diode. Use of the Schottky diode parallel to the SR FET may provide higher efficiency and typically a 1 A surface mount Schottky diode is adequate. The voltage rating of the Schottky diode and the SR FET should be at least 1.4 times the expected peak inverse voltage (PIV) based on the turns ratio used for the transformer. The interaction between the leakage reactance of the output windings and the SR FET capacitance (COSS) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to primary switch turn-on. This ringing can be suppressed using an RC snubber connected across the SR FET. A snubber resistor in the range of 10 ohms to 47 ohms may be used (higher resistance values lead to noticeable drop in efficiency). A capacitance value of 1 nF to 2.2 nF is adequate for most designs.

### Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies. Typically, 200  $\mu$ F to 300  $\mu$ F of aluminum capacitance per ampere of output current is adequate. The other factor that influences choice of the capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin be used.

### Output Voltage Feedback Circuit

The output voltage FEEDBACK pin voltage is 1.265 V [ $V_{FB}$ ]. A voltage divider network should be connected at the output of the power supply to divide the output voltage such that the voltage at the FEEDBACK pin will be 1.265 V when the output is at its desired voltage. The lower feedback divider resistor should be tied to the SECONDARY GROUND pin. A 300 pF (or smaller) decoupling capacitor should be connected at the FEEDBACK pin to the SECONDARY GROUND pin of the InnoSwitch3-AQ IC. This capacitor should be placed close to the InnoSwitch3-AQ IC.

### Recommendations for Circuit Board Layout

See Figure 15 for a recommended circuit board layout for an InnoSwitch3-AQ based power supply.

#### Single-Point Grounding

Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

#### Bypass Capacitors

The PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

#### Primary Loop Area

The area of the primary loop that connects the input filter capacitor, transformer primary and IC should be kept as small as possible.

#### Primary Clamp Circuit

A clamp is used to limit peak voltage on the DRAIN pin at turn-off. This can be achieved by using an RCD clamp or a Zener diode (~200 V) and diode clamp across the primary winding. To reduce EMI, minimize the loop from the clamp components to the transformer and IC.

#### Thermal Considerations

The SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly for the output SR switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR switch. Sufficient copper area should be provided on the board to keep the IC temperature safely below the absolute maximum limits. It is recommended that the copper area provided for the copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

#### Y Capacitor (Optional)

The Y capacitor can be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. This routes high amplitude common mode surge currents away from the IC.

#### Output SR Switch

For best performance, the area of the loop connecting the secondary winding, the output SR switch and the output filter capacitor, should be minimized.

#### Drain Node

The drain switching node is the dominant noise generator. As such, the components connected the drain node should be placed close to the IC and away from sensitive feedback circuits. The clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized. The loop area of the loop comprising of the input rectifier filter capacitor, the primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example

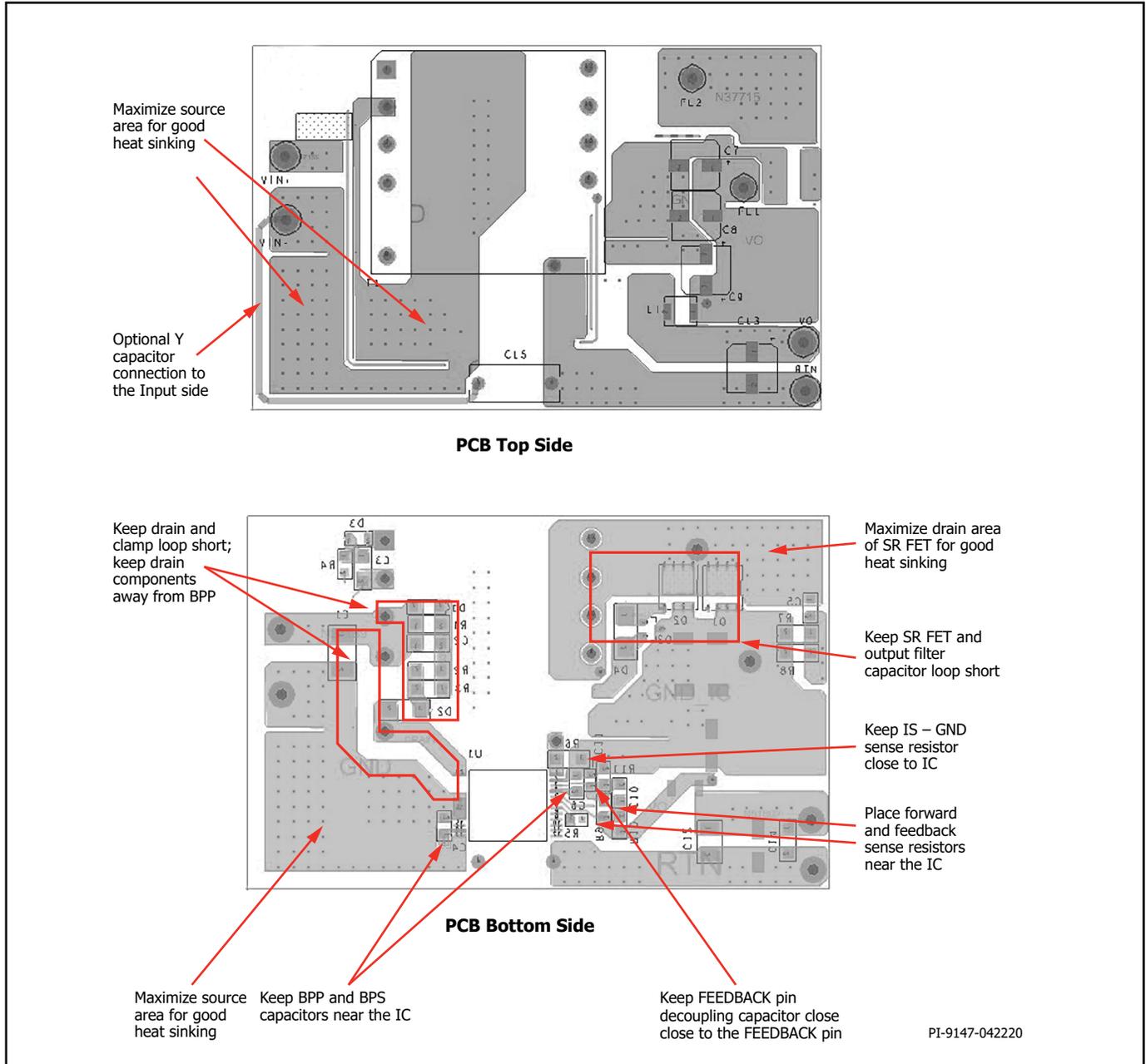


Figure 15. PCB Design.

## Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. A small capacitor in parallel to the clamp diode on the primary-side can help reduce radiated EMI.
3. A resistor in series with the bias winding helps reduce radiated EMI.
4. Shield windings can also be used to improve conducted and radiated EMI margins.
5. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
6. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI
7. A 1  $\mu$ F ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

## Recommendations for Transformer Design

Transformer design must ensure that the power supply delivers the rated power at the lowest input voltage. It is recommended that a  $K_p$  close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-AQ designs. A  $K_p$  value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side switch resulting in higher InnoSwitch3-AQ temperature. The benefits of quasi-resonant switching start to diminish for a further reduction of  $K_p$ .

## Switching Frequency ( $f_{sw}$ )

It is a unique feature in InnoSwitch3-AQ that for full load, the designer can set the switching frequency to between 25 kHz to 95 kHz. For lowest temperature, the switching frequency should be set to around 60 kHz. For a smaller transformer, the full load switching frequency needs to be set to 95 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed 110 kHz which may trigger auto-restart due to overload protection.

## Reflected Output Voltage, $V_{OR}$ (V)

This parameter describes the effect on the primary switch drain voltage of the secondary-winding voltage during diode/SR conduction which is reflected back to the primary through the turns ratio of the transformer. To make full use of QR capability and ensure flattest efficiency over line/load, set reflected output voltage ( $V_{OR}$ ) to maintain  $K_p = 0.8$  at minimum input voltage and  $K_p = 1$  for high input voltage conditions.

Consider the following for design optimization:

1. Higher  $V_{OR}$  allows increased power delivery at  $V_{MIN}$ , which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch3-AQ device.
2. Higher  $V_{OR}$  reduces the voltage stress on the output diodes and SR switches.
3. Higher  $V_{OR}$  increases leakage inductance which reduces power supply efficiency.
4. Higher  $V_{OR}$  increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For output voltages above 15 V,  $V_{OR}$  should be higher to maintain an acceptable PIV across the output synchronous rectifier.

## Ripple to Peak Current Ratio, $K_p$

A  $K_p$  below 1 indicates continuous conduction mode, where  $K_p$  is the ratio of ripple-current to peak-primary-current (Figure 16).

$$K_p = K_{RP} = I_r / I_p$$

A value of  $K_p$  higher than 1, indicates discontinuous conduction mode. In this case  $K_p$  is the ratio of primary switch off-time to the secondary diode conduction-time.

$$K_p = K_{DP} = (1 - D) \times T / t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that a  $K_p$  close to 0.9 at the minimum expected DC bus voltage should be used for most InnoSwitch3-AQ designs. A  $K_p$  value of <1 results in higher transformer efficiency by lowering the primary RMS current but results in higher switching losses in the primary-side switch resulting in higher InnoSwitch3-AQ temperature. The benefits of quasi-resonant switching start to diminish for a further reduction of  $K_p$ . The PIXLs spreadsheet can be used to effectively optimize selection of  $K_p$ , inductance of the primary winding, transformer turns ratio, and the operating frequency while ensuring appropriate design margins.

## Core Type

Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

## Safety Margin, M (mm)

For designs that require safety isolation between primary and secondary that are not using triple insulated wire, the width of the safety margin to be used on each side of the bobbin is important. For high input voltage designs a total margin of 6.2 mm is typically required – 3.1 mm being used on either side of the winding. For vertical bobbins the margin may not be symmetrical. However if a total margin of 6.2 mm is required then the physical margin can be placed on only one side of the bobbin. For designs using triple insulated wire it may still be necessary to add a small margin in order to meet required creepage distances. Many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required. As the margin reduces the available area for the windings, the winding area will disproportionately reduce for small core sizes.

It is recommended that for compact power supply designs using an InnoSwitch3-AQ IC, triple insulated wire should be used.

## Primary Layers, L

Primary layers should be in the range of  $1 \leq L \leq 3$  and in general should be the lowest number that meets the primary current density limit (CMA). A value of  $\geq 200$  Cmil / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. Designs with more than 3 layers are possible but the increased leakage inductance and the physical fit of the windings should be considered. A split primary construction may be helpful for designs where clamp dissipation due to leakage inductance is too high. In split primary construction, half of the primary winding is placed on either side of the secondary (and bias) winding in a sandwich arrangement. This arrangement is often disadvantageous for low power designs as this typically increases common mode noise and adds cost to the input filtering.

**Maximum Operating Flux Density,  $B_M$  (Gauss)**

A maximum value of 3800 gauss at the peak device current limit (at 132 kHz) is recommended to limit the peak flux density at start-up and under output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows the transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch3-AQ IC provide sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

**Transformer Primary Inductance, (LP)**

Once the lowest operating input voltage, switching frequency at full load, and required VOR are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

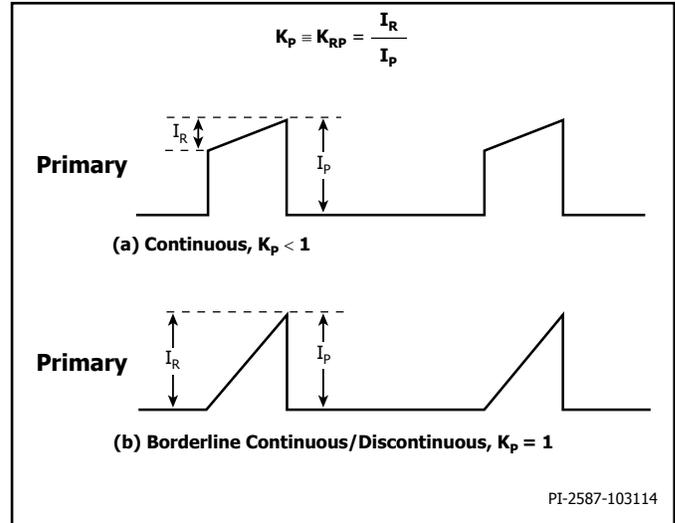


Figure 16. Continuous Conduction Mode Current Waveform,  $K_p < 1$ .

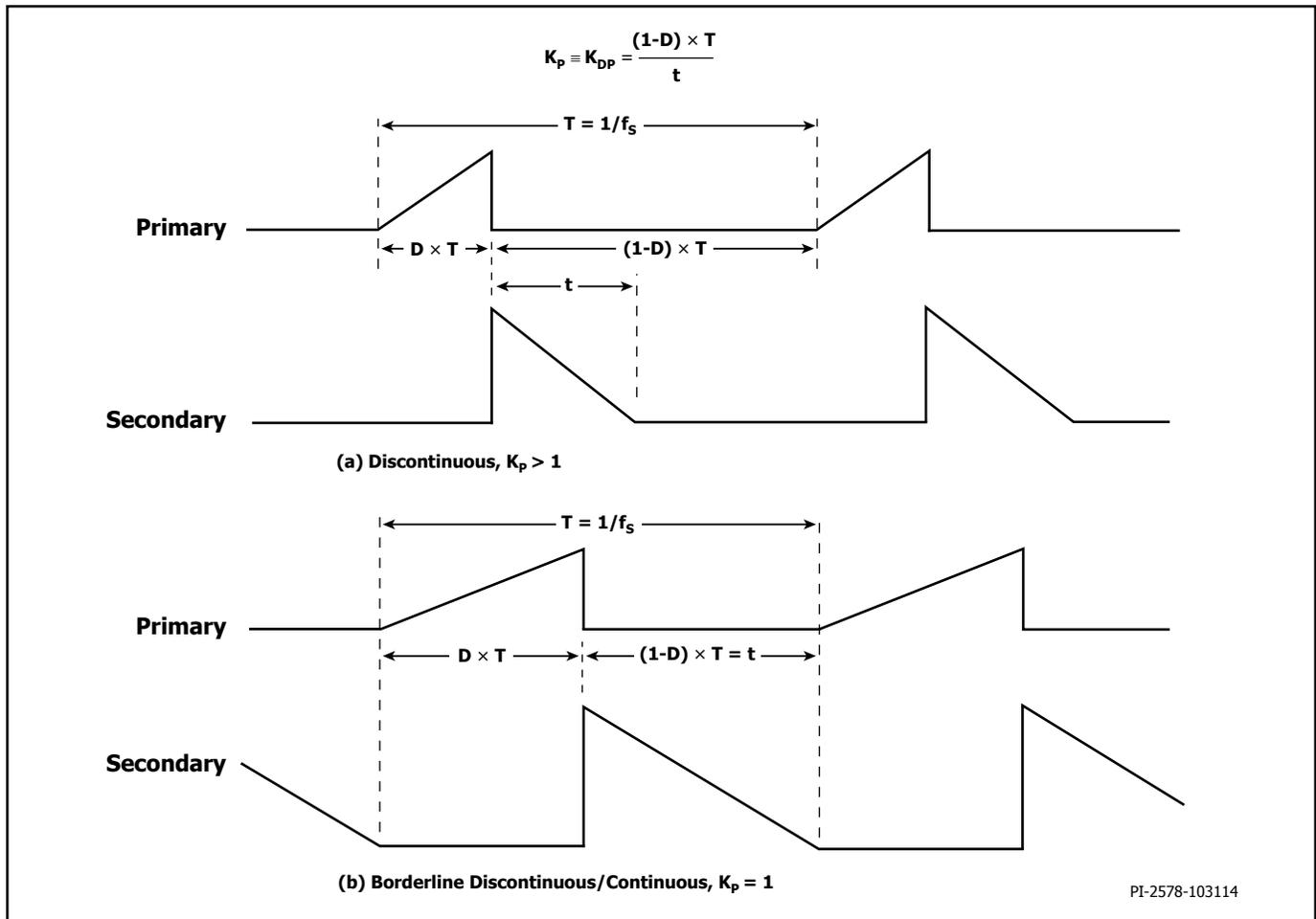


Figure 17. Discontinuous Conduction Mode Current Waveform,  $K_p > 1$ .

## Quick Design Checklist

As with any power supply, the operation of all InnoSwitch3-AQ designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:

1. Maximum Drain Voltage – Verify that  $V_{DS}$  of InnoSwitch3-AQ and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below  $I_{LIMIT(MIN)}$  at the end of  $t_{LEB(MIN)}$ . Under all conditions, the maximum drain current for the primary switch should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch3-AQ IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the  $R_{DS(ON)}$  of the InnoSwitch3-AQ IC.

## Absolute Maximum Ratings<sup>1,2</sup>

DRAIN Pin Voltage	-0.3 V to 750 V
DRAIN Pin Peak Current	5.92 A <sup>3</sup>
BPP/BPS Pin Voltage	-0.3 to 6 V
BPP/BPS Current	100 mA
FWD Pin Voltage	-1.5 V to 150 V
SR, FB Pin Voltage	-0.3 V to 6 V
VOUT Pin Voltage	-0.3 V to 27 V
V Pin Voltage	-0.3 V to 650 V
Storage Temperature	-65 to 150 °C
Operating Junction Temperature <sup>4</sup>	-40 to 150 °C
Ambient Temperature	-40 to 125 °C
Lead Temperature <sup>5</sup>	260 °C

### Notes:

1. All voltages referenced to SOURCE and Secondary GROUND,  $T_A = 25\text{ °C}$ .
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Please refer to Figure 18 about maximum allowable voltage and current conditions.
4. Normally limited by internal circuitry.
5. 1/16" from case for 5 seconds.

## Thermal Resistance

Thermal Resistance:

$(\theta_{JA})$	76 °C/W <sup>1</sup> , 65 °C/W <sup>2</sup>
$(\theta_{JC})$	8 °C/W <sup>3</sup>

### Notes:

1. Soldered to 0.36 sq. inch (232 mm<sup>2</sup>) 2 oz. (610 g/m<sup>2</sup>) copper clad.
2. Soldered to 1 sq. inch (645 mm<sup>2</sup>), 2 oz. (610 g/m<sup>2</sup>) copper clad.
3. The case temperature is measured on the top of the package.

Parameter	Conditions	Rating	Units
<b>Ratings for UL1577</b>			
<b>Primary-Side Current Rating</b>	Current from pin (16-19) to pin 24	1.5	A
<b>Primary-Side Power Rating</b>	$T_{AMB} = 25\text{ °C}$ (Device mounted in socket resulting in $T_{CASE} = 120\text{ °C}$ )	1.35	W
<b>Secondary-Side Power Rating</b>	$T_{AMB} = 25\text{ °C}$ (Device mounted in socket)	0.125	W
<b>Package and Insulation Characteristics</b>			
<b>Clearance</b>		11.7	mm (min)
<b>Creepage</b>		11.2	mm (min)
<b>Distance Through Insulation (DTI)</b>		0.4	mm (min)
<b>Transient Isolation Voltage</b>		6	kV (min)
<b>Comparative Tracking Index (CTI)</b>		600	-

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Package and Insulation Characteristics (cont.)</b>						
<b>Maximum RMS Working Isolation Voltage</b>	$V_{IORM}$			530		$V_{RMS}$
<b>Maximum Repetitive Peak Isolation Voltage</b>	$V_{IORM}$			750		$V_{PEAK}$
<b>Input to Output Test Peak Voltage</b>	$V_{PD}$	Method A, After Environmental Tests Subgroup 1, $V_{PR} = 1.6 \times V_{IORM}$ , $t = 10$ s (qualification) Partial Discharge < 5 pC		1200		$V_{PEAK}$
		Method A, After Input/Output Safety Test Subgroup 2/3, $V_{PR} = 1.2 \times V_{IORM}$ , $t = 10$ s, (qualification) Partial Discharge < 5 pC		300		
		Method B1, 100% Production Test, $V_{PR} = 1.875 \times V_{IORM}$ , $t = 1$ s Partial Discharge < 5 pC		1406		
<b>Maximum Transient Peak Isolation Voltage</b>	$V_{IOTM}$	$V_{TEST} = V_{IOTM}$ , $t = 60$ s (qualification), $t = 1$ s (100% production)		4000	8000	$V_{PEAK}$
<b>Insulation Resistance</b>	$R_S$	$V_{IO} = 500$ V at $T_S$			$>10^9$	$\Omega$
<b>Maximum Case Temperature</b>	$T_S$				150	$^{\circ}\text{C}$
<b>Pollution Degree</b>				2		
<b>Climatic Classification</b>				40/125/21		
<b>RMS Withstanding Isolation Voltage</b>	$V_{ISO}$	$V_{TEST} = V_{ISO}$ , $t = 60$ s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 4800 V_{RMS}$ , $t = 1$ s (100% production)		4000		$V_{RMS}$

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V T <sub>J</sub> = -40 °C to 125 °C (Unless Otherwise Specified)					
<b>Control Functions</b>							
Startup Switching Frequency	f <sub>SW</sub>	T <sub>J</sub> = 25 °C		23	25	27	kHz
				20.5		28.5	
Jitter Frequency	f <sub>M</sub>	f <sub>SW</sub> = 100 kHz T <sub>J</sub> = 25 °C		0.80	1.25	1.70	kHz
Maximum On-Time	t <sub>ON(MAX)</sub>	T <sub>J</sub> = 25 °C		12.4	14.6	16.9	μs
				11.75		17.75	
BPP Supply Current	I <sub>SI</sub>	V <sub>BPP</sub> = V <sub>BPP</sub> + 0.1 V (MOSFET not Switching)	T <sub>J</sub> = 25 °C	145	200	425	μA
				130		489	
	I <sub>S2</sub>	V <sub>BPP</sub> = V <sub>BPP</sub> + 0.1 V (MOSFET Switching at f <sub>SW</sub> )	T <sub>J</sub> = 25 °C	0.90	1.20	1.73	mA
				0.85		2.00	
BPP Pin Charge Current	I <sub>CH1</sub>	V <sub>DS</sub> = 30 VDC	V <sub>BP</sub> = 0 V	T <sub>J</sub> = 25 °C	-1.75	-1.35	μA
						-1.93	
	I <sub>CH2</sub>		V <sub>BP</sub> = 4 V	T <sub>J</sub> = 25 °C	-5.98	-4.65	μA
						-6.87	
BPP Pin Voltage	V <sub>BPP</sub>			4.65	4.90	5.15	V
BPP Pin Voltage Hysteresis	V <sub>BPP(H)</sub>	T <sub>J</sub> = 25 °C		0.22	0.39	0.55	V
				0.2		0.67	
BPP Shunt Voltage	V <sub>SHUNT</sub>	I <sub>BPP</sub> = 2 mA		5.15	5.36	5.65	V
BPP Power-Up Reset Threshold Voltage	V <sub>BPP(RESET)</sub>	T <sub>J</sub> = 25 °C		2.80	3.15	3.50	V
				2.1		4.13	
<b>Line Fault Protection</b>							
VOLTAGE Pin Line Over-voltage Deglitch Filter	t <sub>OV+</sub>	See Note B			3		μs
VOLTAGE Pin Voltage Rating	V <sub>V</sub>	T <sub>J</sub> = 25 °C		650			V
UV/OV Pin Brown-In Threshold	I <sub>UV+</sub>	T <sub>J</sub> = 25 °C		23.9	26.1	28.2	μA
				22.1		30.4	
UV/OV Pin Brown-Out Threshold	I <sub>UV-</sub>	T <sub>J</sub> = 25 °C		21.5	23.7	25.5	μA
				19.7		27	
Brown-Out Delay Time	t <sub>UV-</sub>				32		ms
UV/OV Pin Line Overvoltage Threshold	I <sub>OV+</sub>	T <sub>J</sub> = 25 °C		110	115	122	μA
				98		127	
UV/OV Pin Line Overvoltage Hysteresis	I <sub>OV(H)</sub>	T <sub>J</sub> = 25 °C		6	7	8	μA
				5		9.5	

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V T <sub>J</sub> = -40 °C to 125 °C (Unless Otherwise Specified)					
<b>Circuit Protection</b>							
<b>Standard Current Limit (BPP) Capacitor = 0.47 μF</b> See Note C	I <sub>LIMIT</sub>	di/dt = 300 mA/μs	T <sub>J</sub> = 25 °C	1233	1326	1419	mA
				1150		1482	
<b>Increased Current Limit (BPP) Capacitor = 4.7 μF</b> See Note C	I <sub>LIMIT+1</sub>	di/dt = 300 mA/μs	T <sub>J</sub> = 25 °C	1385	1523	1662	mA
				1300		1715	
<b>Overload Detection Frequency</b>	f <sub>OVL</sub>	See Note A	T <sub>J</sub> = 25 °C	102	110	118	kHz
				96		125	
<b>BYPASS Pin Latching Shutdown Threshold Current</b>	I <sub>SD</sub>	T <sub>J</sub> = 25 °C		6.0	8.9	11.3	mA
				5.7		11.9	
<b>Auto-Restart On-Time</b>	t <sub>AR</sub>	T <sub>J</sub> = 25 °C		75	82	89	ms
				71		94	
<b>Auto-Restart Trigger Skip Time</b>	t <sub>AR(SK)</sub>	See Note A	T <sub>J</sub> = 25 °C		1.3		sec
				1.5		2.4	
<b>Auto-Restart Off-Time</b>	t <sub>AR(OFF)</sub>			1.65		2.11	sec
<b>Short Auto-Restart Off-Time</b>	t <sub>AR(OFF)SH</sub>	T <sub>J</sub> = 25 °C See Note B		0.17	0.20	0.23	sec
<b>Output</b>							
<b>ON-State Resistance</b>	R <sub>DS(ON)</sub>	I <sub>D</sub> = I <sub>LIMIT+1</sub>	T <sub>J</sub> = 25 °C		1.20	1.38	Ω
					1.86	2.3	
<b>OFF-State Drain Leakage Current</b>	I <sub>DSS1</sub>	V <sub>BPP</sub> = V <sub>BPP</sub> + 0.1 V V <sub>DS</sub> = 80% BV <sub>DSS</sub>				200	μA
<b>Breakdown Voltage</b>	BV <sub>DSS</sub>	V <sub>BPP</sub> = V <sub>BPP</sub> + 0.1 V	T <sub>J</sub> = 25 °C	750			V
<b>Drain Supply Voltage</b>		See Note A		30			V
<b>Thermal Shutdown</b>	T <sub>SD</sub>	See Note A		135	142	150	°C
<b>Thermal Shutdown Hysteresis</b>	T <sub>SD(H)</sub>	See Note A			30		°C

Parameter	Symbol	Conditions SOURCE = 0 V T <sub>j</sub> = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
<b>Secondary</b>						
Feedback Pin Voltage	V <sub>FB</sub>	T <sub>j</sub> = 25 °C	1.239	1.265	1.290	V
			1.21		1.31	
Maximum Switching Frequency	f <sub>SREQ</sub>	T <sub>j</sub> = 25 °C	117	132	145	kHz
			106		158	
FEEDBACK Pin Auto-Restart Threshold	V <sub>FB(AR)</sub>			90		%
Output Voltage Pin Auto-Restart Timer	t <sub>FB(AR)</sub> t <sub>IS(AR)</sub>	T <sub>j</sub> = 25 °C		49.5		ms
BPS Pin Current at No-Load	I <sub>SNL</sub>	T <sub>j</sub> = 25 °C		325	485	μA
				335		
BPS Pin Voltage	V <sub>BPS</sub>		4.20	4.40	4.60	V
BPS Pin Undervoltage Threshold	V <sub>BPS(UVLO)(TH)</sub>		3.60	3.80	4.00	V
BPS Pin Undervoltage Hysteresis	V <sub>BPS(UVLO)(H)</sub>			0.65		V
Current Limit Voltage Threshold	I <sub>SV(TH)</sub>	Set By External Resistor	33.94	35.90	38.00	mV
FWD Pin Voltage	V <sub>FWD</sub>		150			V
Minimum Off-Time	t <sub>OFF(MIN)</sub>		2.48	3.38	4.37	μs
Soft-Start Frequency Ramp Time	t <sub>SS(RAMP)</sub>	T <sub>j</sub> = 25 °C	7.50	11.75	16.00	ms
BPS Pin Latch Command Shutdown Threshold Current	I <sub>BPS(SD)</sub>		5.2	8.9		mA
Feedback Pin Short-Circuit	V <sub>FB(OFF)</sub>	T <sub>j</sub> = 25 °C	50	112	135	mV

Parameter	Symbol	Conditions		Min	Typ	Max	Units
		SOURCE = 0 V T <sub>J</sub> = -40 °C to 125 °C (Unless Otherwise Specified)					
<b>Synchronous Rectifier @ T<sub>J</sub> = 25 °C</b>							
SR Pin Drive Voltage	V <sub>SR</sub>				4.4		V
SR Pin Voltage Threshold	V <sub>SR(TH)</sub>				-3.3		mV
SR Pin Pull-Up Current	I <sub>SR(PU)</sub>	T <sub>J</sub> = 25 °C		135	165	195	mA
				100		230	
SR Pin Pull-Down Current	I <sub>SR(PD)</sub>	T <sub>J</sub> = 25 °C		260	298	336	mA
				186		435	
Rise Time	t <sub>R</sub>	T <sub>J</sub> = 25 °C C <sub>LOAD</sub> = 2 nF	10-90% See Note B		40		ns
Fall Time	t <sub>F</sub>	T <sub>J</sub> = 25 °C C <sub>LOAD</sub> = 2 nF	10-90% See Note B		15		ns
Output Pull-Up Resistance	R <sub>PU</sub>	V <sub>BPS</sub> = 4.4 V I <sub>SR</sub> = 10 mA	T <sub>J</sub> = 25 °C	7.4	8.5	9.6	Ω
				5		12.42	
Output Pull-Down Resistance	R <sub>PD</sub>	V <sub>BPS</sub> = 4.4 V I <sub>SR</sub> = 10 mA	T <sub>J</sub> = 25 °C	3.52	3.95	4.39	Ω
				2.35		6.72	

**NOTES:**

- This parameter is derived from characterization.
- This parameter is guaranteed by design.
- To ensure correct current limit it is recommended that nominal 0.47 μF / 4.7 μF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	Tolerance Relative to Nominal Capacitor Value	
	Minimum	Maximum
0.47 μF	-60%	+100%
4.7 μF	-50%	N/A

Typical Performance Curves

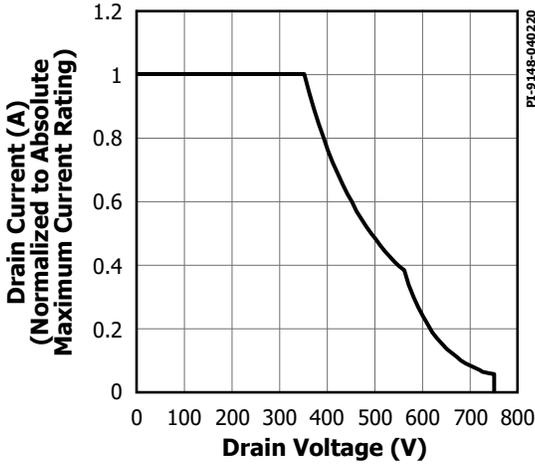


Figure 18. Maximum Allowable Drain Current vs. Drain Voltage.

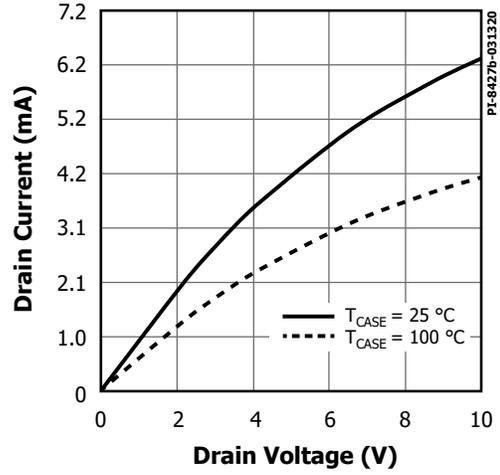


Figure 19. Output Characteristics.

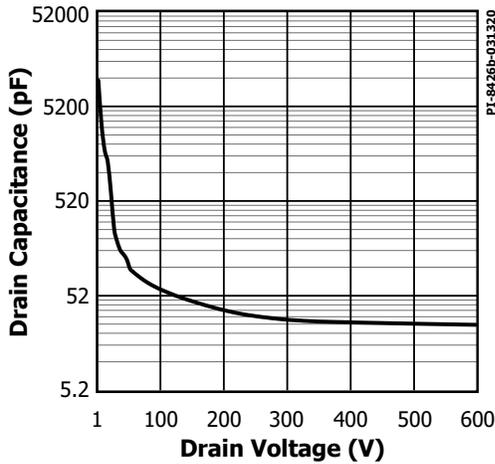


Figure 20.  $C_{OSS}$  vs. Drain Voltage.

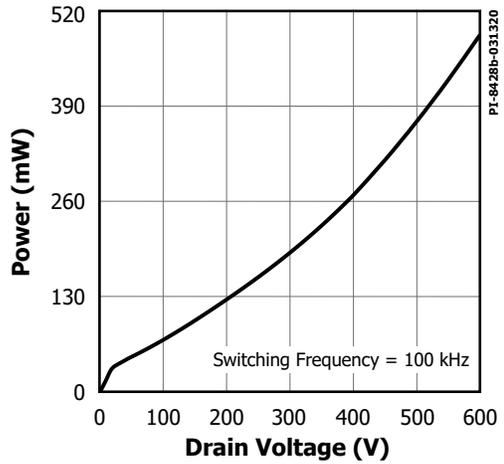


Figure 21. Drain Capacitance Power.

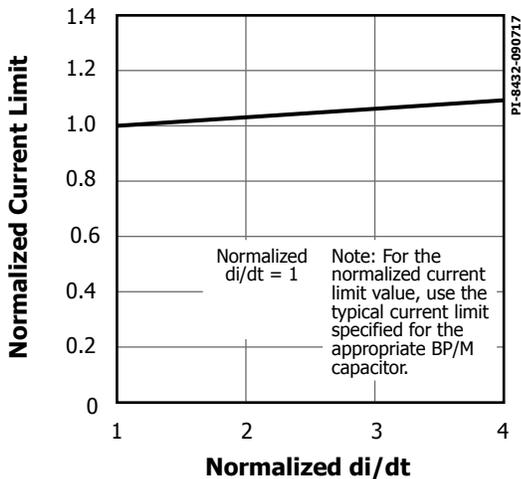


Figure 22. Standard Current Limit vs.  $di/dt$ .

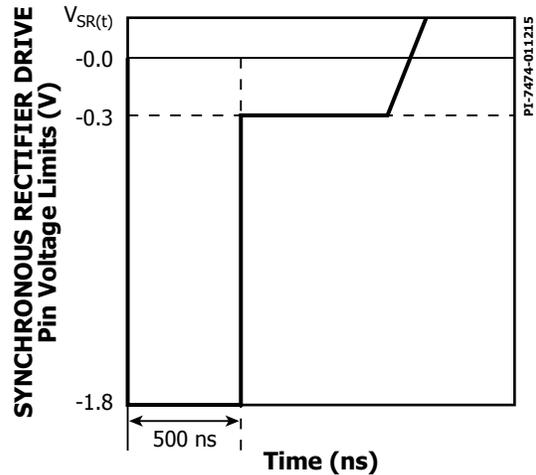


Figure 23. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

Typical Performance Curves

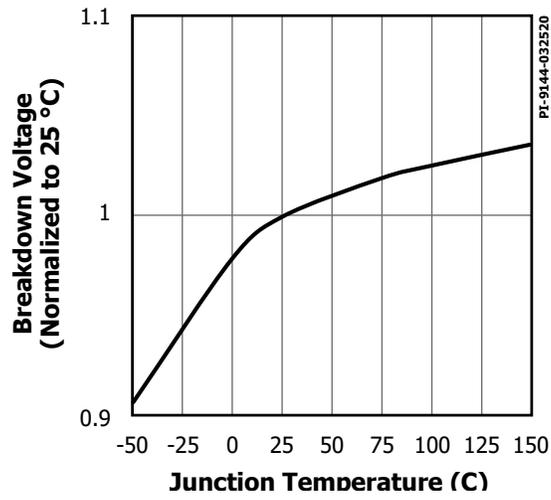
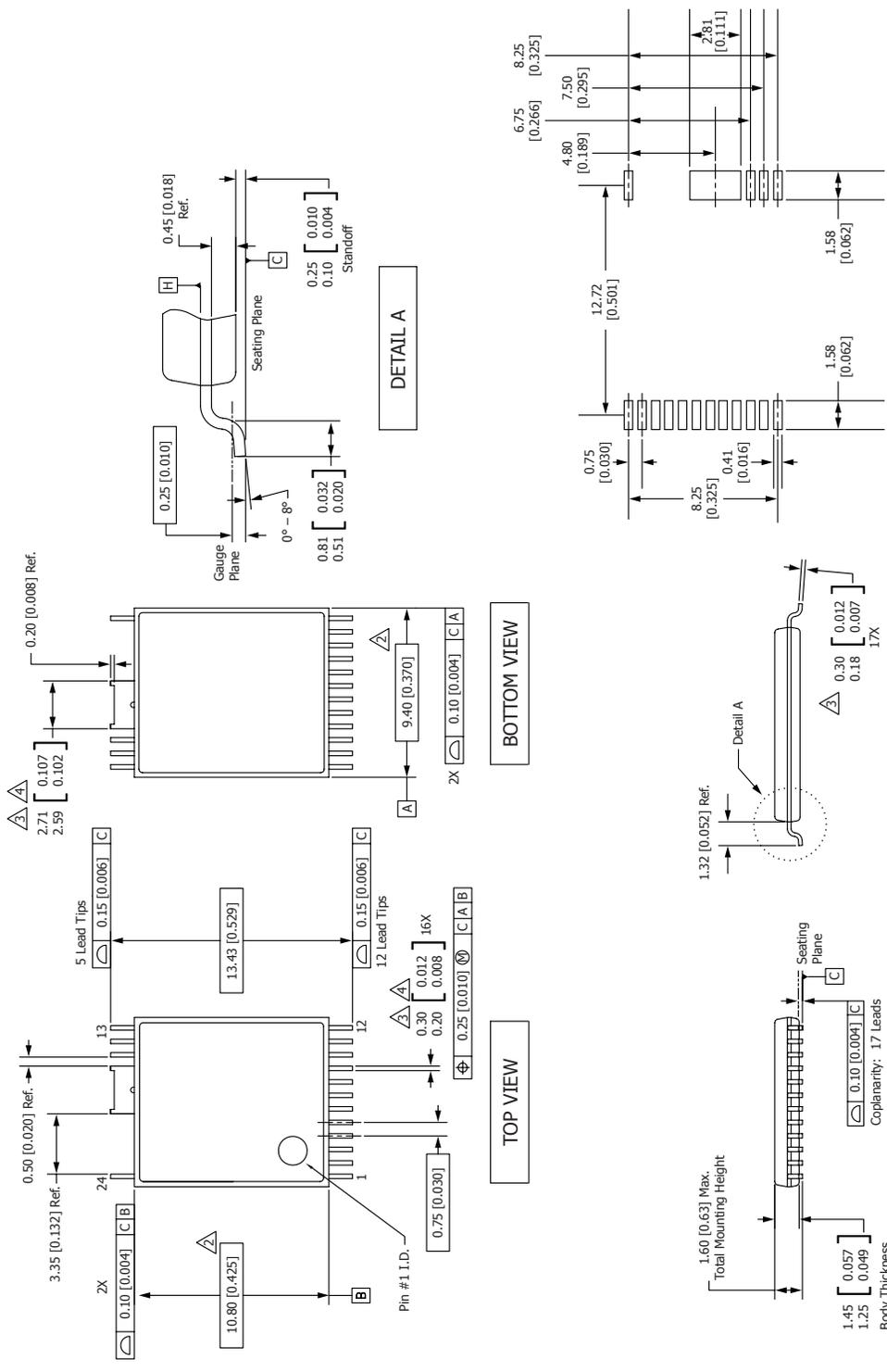


Figure 24. Breakdown Voltage vs. Temperature.

InSOP-24D

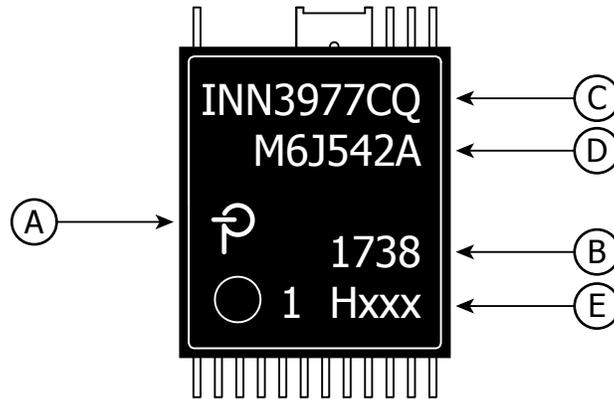


- Notes:
1. Dimensioning and Tolerancing per ASME Y14.5M - 1994.
  2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 [0.007] per side.
  3. Dimensions noted are inclusive of plating thickness.
  4. Does not include inter-lead flash or protrusions.
  5. Controlling dimensions in millimeters [inches].
  6. Datums A & B to be determined at Datum H.

PI-8106-051718  
POD-InSOP-24D Rev B

## PACKAGE MARKING

## InSOP-24D



- A. Power Integrations Registered Trademark
- B. Assembly Date Code (last two digits of year followed by 2-digit work week)
- C. Product Identification (Part #/Package Type)
- D. Lot Identification Code
- E. Test Sublot and Feature Code

PI-8727b-070819

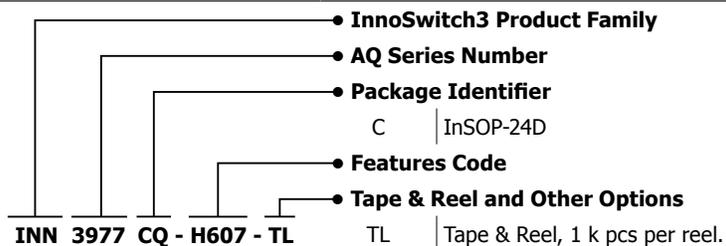
## MSL Table

Part Number	MSL Rating
INN3977CQ	3

## ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	JESD78D	> ±100 mA or > $1.5 \times V_{MAX}$ on all pins
Human Body Model ESD	ANSI/ESDA/JEDEC JS-001-2014	> ±2000 V on all pins
Charge Device Model ESD	ANSI/ESDA/JEDEC JS-002-2014	> ±500 V on all pins

## Part Ordering Information



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# Notes

Revision	Notes	Date
B	Code A release.	04/20

**For the latest updates, visit our website: [www.power.com](http://www.power.com)**

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**Power Integrations Worldwide Sales Support Locations**

**World Headquarters**

5245 Hellyer Avenue  
 San Jose, CA 95138, USA  
 Main: +1-408-414-9200  
 Customer Service:  
 Worldwide: +1-65-635-64480  
 Americas: +1-408-414-9621  
 e-mail: [usasales@power.com](mailto:usasales@power.com)

**China (Shanghai)**

Rm 2410, Charity Plaza, No. 88  
 North Caoxi Road  
 Shanghai, PRC 200030  
 Phone: +86-21-6354-6323  
 e-mail: [chinasales@power.com](mailto:chinasales@power.com)

**China (Shenzhen)**

17/F, Hivac Building, No. 2, Keji Nan  
 8th Road, Nanshan District,  
 Shenzhen, China, 518057  
 Phone: +86-755-8672-8689  
 e-mail: [chinasales@power.com](mailto:chinasales@power.com)

**Germany (AC-DC/LED Sales)**

Einsteinring 24  
 85609 Dornach/Aschheim  
 Germany  
 Tel: +49-89-5527-39100  
 e-mail: [eurosales@power.com](mailto:eurosales@power.com)

**Germany (Gate Driver Sales)**

HellwegForum 1  
 59469 Ense  
 Germany  
 Tel: +49-2938-64-39990  
 e-mail: [igbt-driver.sales@power.com](mailto:igbt-driver.sales@power.com)

**India**

#1, 14th Main Road  
 Vasanthanagar  
 Bangalore-560052 India  
 Phone: +91-80-4113-8020  
 e-mail: [indiasales@power.com](mailto:indiasales@power.com)

**Italy**

Via Milanese 20, 3rd. Fl.  
 20099 Sesto San Giovanni (MI) Italy  
 Phone: +39-024-550-8701  
 e-mail: [eurosales@power.com](mailto:eurosales@power.com)

**Japan**

Yusen Shin-Yokohama 1-chome Bldg.  
 1-7-9, Shin-Yokohama, Kohoku-ku  
 Yokohama-shi,  
 Kanagawa 222-0033 Japan  
 Phone: +81-45-471-1021  
 e-mail: [japansales@power.com](mailto:japansales@power.com)

**Korea**

RM 602, 6FL  
 Korea City Air Terminal B/D, 159-6  
 Samsung-Dong, Kangnam-Gu,  
 Seoul, 135-728, Korea  
 Phone: +82-2-2016-6610  
 e-mail: [koreasales@power.com](mailto:koreasales@power.com)

**Singapore**

51 Newton Road  
 #19-01/05 Goldhill Plaza  
 Singapore, 308900  
 Phone: +65-6358-2160  
 e-mail: [singaporesales@power.com](mailto:singaporesales@power.com)

**Taiwan**

5F, No. 318, Nei Hu Rd., Sec. 1  
 Nei Hu Dist.  
 Taipei 11493, Taiwan R.O.C.  
 Phone: +886-2-2659-4570  
 e-mail: [taiwansales@power.com](mailto:taiwansales@power.com)

**UK**

Building 5, Suite 21  
 The Westbrook Centre  
 Milton Road  
 Cambridge  
 CB4 1YG  
 Phone: +44 (0) 7823-557484  
 e-mail: [eurosales@power.com](mailto:eurosales@power.com)