74ABT16244A

16-bit buffer/line driver; 3-state

Rev. 9 — 5 July 2021

Product data sheet

1. General description

The 74ABT16244A is a 16-bit buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The device features four output enables (1 $\overline{\text{OE}}$, 2 $\overline{\text{OE}}$, 3 $\overline{\text{OE}}$ and 4 $\overline{\text{OE}}$), each controlling four of the 3-state outputs. A HIGH on n $\overline{\text{OE}}$ causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- · Direct interface with TTL levels
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- 3-state buffers
- · Output capability: +64 mA and -32 mA
- · Live insertion and extraction permitted
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - CDM JESD22-C101-C exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

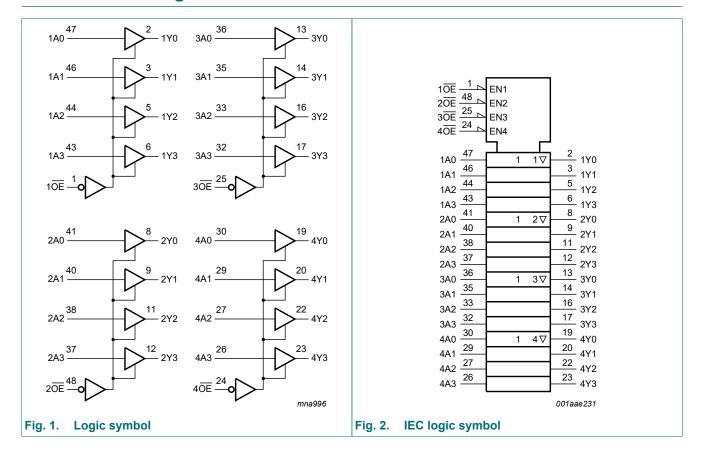
Table 1. Ordering information

Type number	Package						
	Temperature range	Name	Description	Version			
74ABT16244ADGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1			



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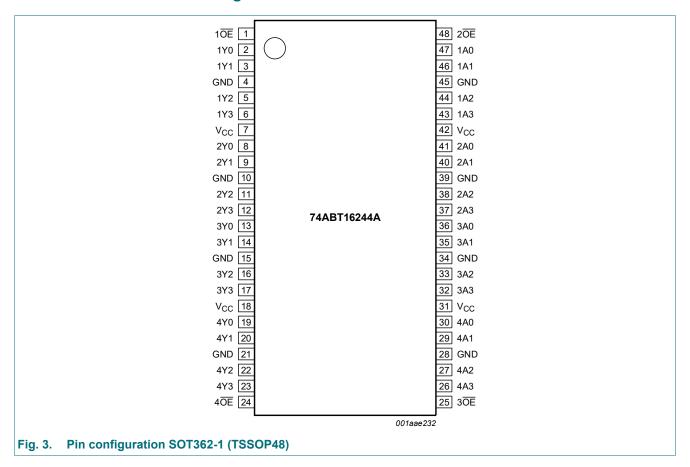
4. Functional diagram



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5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
10E, 20E, 30E, 40E	1, 48, 25, 24	1 to 4 output enable (LOW active)
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	1 data output 0 to output 3
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	2 data output 0 to output 3
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	3 data output 0 to output 3
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	4 data output 0 to output 3
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	4 data input 0 to input 3
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	3 data input 0 to input 3
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	2 data input 0 to input 3
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	1 data input 0 to input 3

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6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don \ t \ care; \ Z = high-impedance \ OFF-state.$

Control	Input	Output
nŌE	nAn	nYn
L	L	L
	Н	Н
Н	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
VI	input voltage		[1]	-1.2	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+5.5	V
I _{IK}	input clamping current	V _I < 0 V		-18	-	mA
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
I _O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	-64	mA
Tj	junction temperature		[2]	-	150	°C
T _{stg}	storage temperature			-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		4.5	-	5.5	V
VI	input voltage		0	-	V _{CC}	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level Input voltage		-	-	0.8	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current		-	-	64	mA
Δt/ΔV	input transition rise and fall rate		-	-	10	ns/V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C

^[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

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9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions			25 °C		-40 °C t	Unit	
				Min	Тур	Max	Min	Max	
V _{IK}	input clamping voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA		-	-0.9	-1.2	-	-1.2	V
V _{OH}	HIGH-level output	V _I = V _{IL} or V _{IH}							
	voltage	V _{CC} = 4.5 V; I _{OH} = -3 mA		2.5	2.9	-	2.5	-	V
		V _{CC} = 5.0 V; I _{OH} = -3 mA		3.0	3.4	-	3.0	-	V
		V _{CC} = 4.5 V; I _{OH} = -32 mA		2.0	2.4	-	2.0	-	V
V _{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	0.42	0.55	-	0.55	V
l _l	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND		-	±0.01	±1.0	-	±1.0	μΑ
I _{OFF}	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} \le 4.5 \text{ V}$		-	±5.0	±100	-	±100	μΑ
I _{O(pu/pd)}	power-up/power- down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC} ; $n\overline{OE}$ = HIGH	[1]	-	±5.0	±50	-	±50	μΑ
loz	OFF-state output	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
	current	output HIGH-state at V _O = 5.5 V		-	0.1	10	-	10	μΑ
		output LOW-state at V _O = 0 V		-	-0.1	-10	-	-10	μΑ
I _{CEX}	output high leakage current	HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND or } V_{CC}$		-	5.0	50	-	50	μA
Io	output current	V _{CC} = 5.5 V; V _O = 2.5 V	[2]	-50	-100	-180	-50	-180	mA
I _{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	0.45	1.0	-	1.0	mA
		outputs LOW-state		-	10	19	-	19	mA
		outputs 3-state		-	0.45	1.0	-	1.0	mA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 5.5 V; one input at 3.4V and other inputs at V _{CC} or GND	[3] [4]	-	100	250	-	250	μA
Cı	input capacitance	V _I = 0 V or V _{CC}		-	4	-	-	-	pF
C _{I/O}	input/output capacitance	outputs disabled; $V_O = 0 \text{ V or } V_{CC}$		-	7	-	-	-	pF

^[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 μ s is permitted.

^[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

^[3] This is the increase in supply current for each input at 3.4 V.

^[4] This data sheet limit may vary among suppliers.

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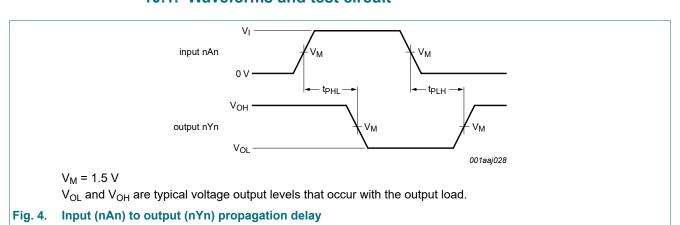
10. Dynamic characteristics

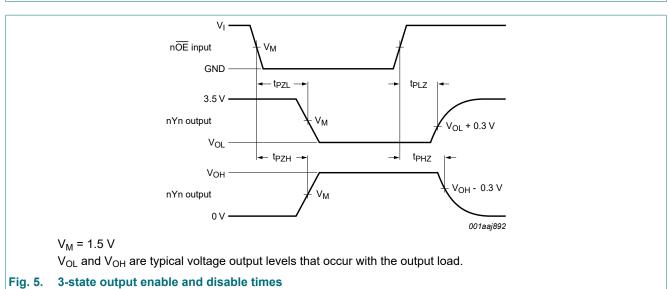
Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 6.

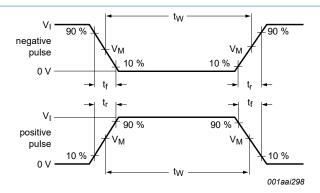
Symbol	Parameter	Conditions	25 °C	25 °C; V _{CC} = 5.0 V			-40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V		
			Min	Тур	Max	Min	Max		
t _{PLH}	LOW to HIGH propagation delay	nAn to nYn, see Fig. 4	1.1	1.7	2.6	1.1	2.8	ns	
t _{PHL}	HIGH to LOW propagation delay	nAn to nYn, see Fig. 4	1.3	2.1	2.9	1.3	3.4	ns	
t _{PZH}	OFF-state to HIGH propagation delay	nOE to nYn; see Fig. 5	1.6	2.7	3.7	1.6	4.5	ns	
t _{PZL}	OFF-state to LOW propagation delay	nOE to nYn; see Fig. 5	2.3	3.5	4.0	2.3	4.8	ns	
t _{PHZ}	HIGH to OFF-state propagation delay	nOE to nYn; see Fig. 5	1.5	3.0	4.0	1.5	4.6	ns	
t _{PLZ}	LOW to OFF-state propagation delay	nOE to nYn; see Fig. 5	1.6	2.4	3.2	1.6	4.1	ns	

10.1. Waveforms and test circuit



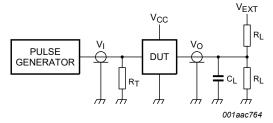


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a. Input pulse definition

 $V_{M} = 1.5 V$



b. Test circuit for 3-state outputs

Test data is given in Table 8.

Definitions test circuit:

R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator.

Fig. 6. Test circuit for measuring switching times

Table 8. Test data

Input		Load V _{EXT}						
V_{I}	fi	t _W	t _r , t _f	CL	R_L	t _{PHZ} , t _{PZH}	t _{PLZ} , t _{PZL}	t _{PLH} , t _{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

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11. Package outline

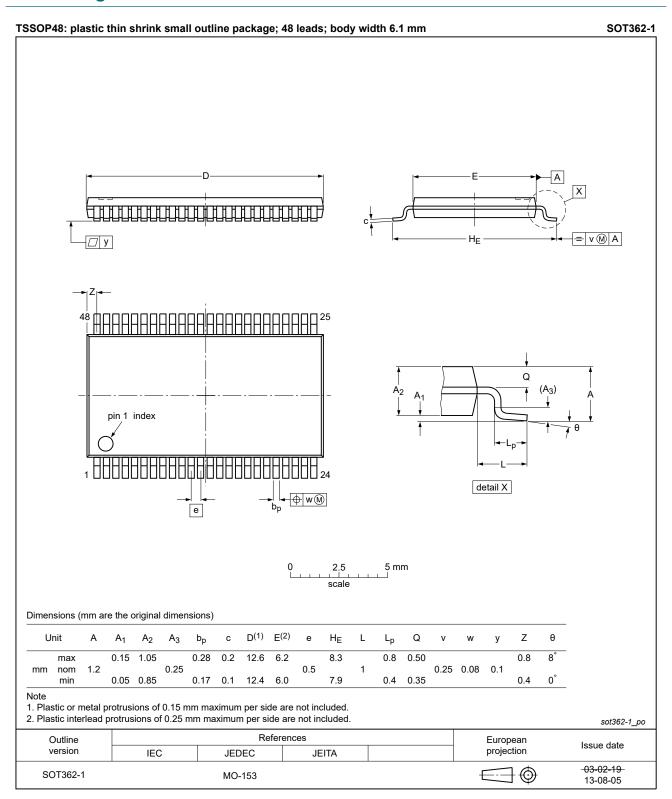


Fig. 7. Package outline SOT362-1 (TSSOP48)

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12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes			
74ABT16244A v.9	20210705	Product data sheet	-	74ABT16244A v.8			
Modifications:	The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 7: Package outline drawing SOT362-1 (TSSOP48) updated. Type number 74ABT162244ADL (SOT370-1/SSOP48) removed. Section 1 and Section 2 updated.						
74ABT16244A v.8	20111103	Product data sheet	-	74ABT16244A v.7			
Modifications:	Legal pages u	pdated					
74ABT16244A v.7	20100525	Product data sheet	-	74ABT16244A v.6			
74ABT16244A v.6	20090323	Product data sheet	-	74ABT16244A v.5			
74ABT16244A v.5	20060210	Product data sheet	-	74ABT_H16244A v.4			
74ABT_H16244A v.4	19981007	Product specification	-	74ABT_H16244A v.3			
74ABT H16244A v.3	19980225	Product specification	-	74ABT_H16244A v.2			

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13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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