ADS58J64 Quad-Channel, 14-Bit, 1-GSPS Telecom Receiver Device

1 Features

- Quad Channel
- 14-Bit Resolution
- Maximum Sampling Rate: 1 GSPS
- Maximum Output Sample Rate: 500 MSPS
- Analog Input Buffer With High-Impedance Input
- Input 3-dB Bandwidth: 1 GHz
- Output Options:
  - Rx: Decimate-by-2 and -4 Options With Low-Pass Filter
  - 200-MHz Complex Bandwidth or 100-MHz Real Bandwidth Support
  - DPD FB: 2x Decimation With 14-Bit Burst Mode Output
- 1.1-V_{PP} Differential Full-Scale Input
- JESD204B Interface:
  - Subclass 1 Support
  - 1 Lane per ADC Up to 10 Gbps
  - Dedicated SYNC Pin for Pair of Channels
- Support for Multi-Chip Synchronization
- 72-Pin VQFN Package (10 mm × 10 mm)
- Power Dissipation: 625 mW/Ch
- Spectral Performance (Burst Mode, High Resolution):
  - f_{IN} = 190 MHz IF at –1 dBFS:
    - SNR: 69 dBFS
    - NSD: –153 dBFS/Hz
    - SFDR: 86 dBc (HD2, HD3), 95 dBFS (Non HD2, HD3)
  - f_{IN} = 370 MHz IF at –3 dBFS:
    - SNR: 68.5 dBFS
    - NSD: –152.5 dBFS/Hz
    - SFDR: 80 dBc (HD2, HD3), 86 dBFS (Non HD2, HD3)

2 Applications

- Multi-Carrier GSM Cellular Infrastructure Base Stations
- Multi-Carrier Multi-Mode Cellular Infrastructure Base Stations
- Telecommunications Receivers
- Telecom DPD Observation Receivers

3 Description

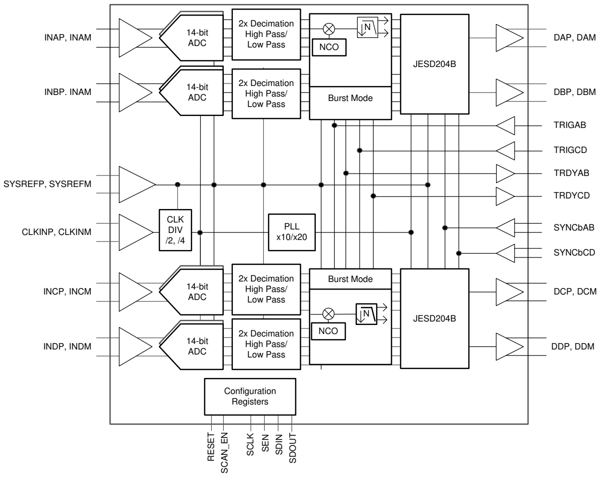
The ADS58J64 is a low-power, wide-bandwidth, 14-bit, 1-GSPS, quad-channel, telecom receiver device. The ADS58J64 supports a JESD204B serial interface with data rates up to 10 Gbps with one lane per channel. The buffered analog input provides uniform input impedance across a wide frequency range and minimizes sample-and-hold glitch energy. The ADS58J64 provides excellent spurious-free dynamic range (SFDR) over a large input frequency range with very low power consumption. The digital signal processing block includes complex mixers followed by low-pass filters with decimate-by-2 and -4 options supporting up to a 200-MHz receive bandwidth. The ADS58J64 also supports a 14-bit, 500-MSPS output in burst mode, making the device suitable for a digital pre-distortion (DPD) observation receiver.

The JESD204B interface reduces the number of interface lines, thus allowing high system integration density. An internal phase-locked loop (PLL) multiplies the incoming analog-to-digital converter (ADC) sampling clock to derive the bit clock that is used to serialize the 14-bit data from each channel.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS58J64	VQFN (72)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2017) to Revision B (December 2021) Page

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Added RHH (VQFN) package option....3
- Changed description for GAINWORD....62
- Added the text *Also need to enable OVR_ON_LSB bit in DIGTOP page* to register 3 and 1 of Register 27h in CHX page....62

Changes from Revision * (January 2017) to Revision A (January 2017) Page

- Changed *Sample* to *Sampling* in third *Features* bullet....1
- Changed *Bandwitdth: 250 MHz* to *Sample Rate: 500 MSPS* in fourth *Features* bullet....1
- Added *Input 3-dB Bandwidth* bullet to *Features* section....1
- Changed plot and SNR and SFDR conditions of Figure 9....12
- Added *for loading trims* to description of bit 1 in *Register 64h Field Descriptions*....44
- Changed *select* to *set* in description of bits 7-0 in *Register 8Dh Field Descriptions* and *Register 8Eh Field Descriptions*....44
- Changed *select* to *set* in description of bits 7-0 in *Register 8Fh Field Descriptions* and *Register 90h Field Descriptions*....45
- Added *Others: Do not use* to Description column of *Register 71h Field Descriptions* and *Register 72h Field Descriptions*....49
- Changed *Others: Do not use* to Description column of *Register 93h Field Descriptions* and *Register 94h Field Descriptions*....50
- Added *Valid only when CTRL_LID = 1* to description of bits 7-4 in *Register 2Dh Field Descriptions*....57
- Changed Description column of *Register 41h Field Descriptions*....61
- Changed *1 :* to *3 :* and added *Others: Do not use* to Description column of *Register 42h Field Descriptions*....61
- Changed description of bits 7-0 in *Register 07h Field Descriptions*....65
- Changed description of bits 7-0 in *Register 08h Field Descriptions*....65

5 Pin Configuration and Functions

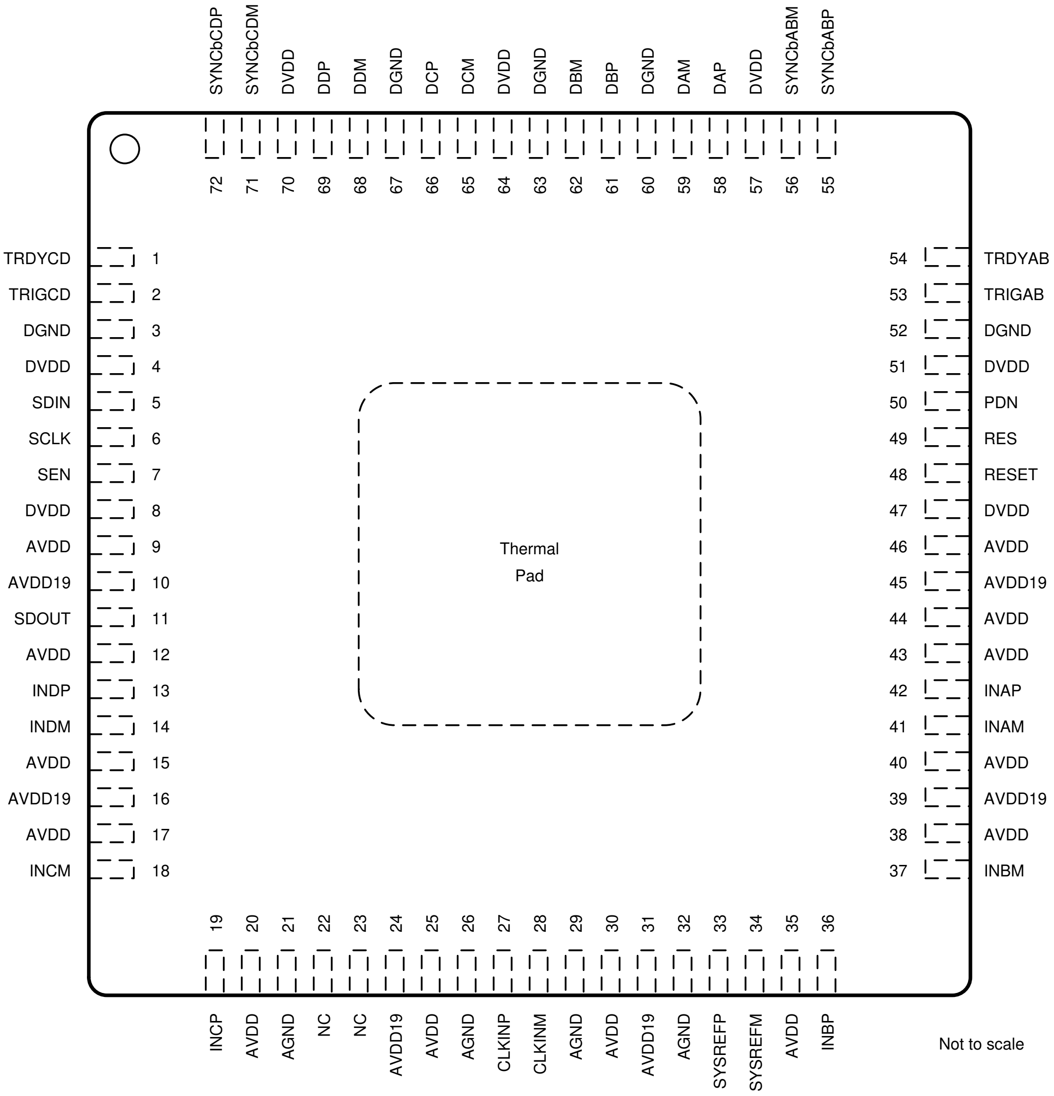


Figure 5-1. RMP or RHH Package 72-Pin VQFN Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
INPUT, REFERENCE			
INAM	41	I	Differential analog input pin for channel A, internal bias via a 2-kΩ resistor to V_{CM}
INAP	42		
INBM	37	I	Differential analog input pin for channel B, internal bias via a 2-kΩ resistor to V_{CM}
INBP	36		
INCM	18	I	Differential analog input pin for channel C, internal bias via a 2-kΩ resistor to V_{CM}
INCP	19		
INPUT, REFERENCE (continued)			
INDM	14	I	Differential analog input pin for channel D, internal bias via a 2-kΩ resistor to V_{CM}
INDP	13		
CLOCK, SYNC			
CLKINM	28	I	Differential clock input pin for the ADC with internal 100-Ω differential termination, requires external ac coupling
CLKINP	27		

Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SYSREFM	34	I	External SYSREF input, requires dc coupling and external termination
SYSREFP	33		
CONTROL, SERIAL			
NC	22, 23	—	No connection
PDN	50	I/O	Power down. This pin can be configured via an SPI register setting. This pin has an internal 10-kΩ pulldown resistor.
RES	49	—	Reserved pin, connect to GND
RESET	48	I	Hardware reset; active high. This pin has an internal 10-kΩ pulldown resistor.
SCLK	6	I	Serial interface clock input. This pin has an internal 10-kΩ pulldown resistor.
SDIN	5	I	Serial interface data input. This pin has an internal 10-kΩ pulldown resistor.
SDOUT	11	O	1.8-V logic serial interface data output
SEN	7	I	Serial interface enable. This pin has an internal 10-kΩ pullup resistor to DVDD.
TRDYAB	54	O	Trigger-ready output for burst mode for channels A and B. This pin can be configured via SPI to a TRDY signal for all four channels in burst mode, and can be left open if not used.
TRDYCD	1	O	Trigger-ready output for burst mode for channels C and D. This pin can be configured via SPI to a TRDY signal for all four channels in burst mode, and can be left open if not used.
TRIGAB	53	I	Manual burst mode trigger input for channels A and B. This pin can be configured via SPI to a manual trigger input signal for all four channels in burst mode, and can be connected to GND if not used. This pin has an internal 10-kΩ pulldown resistor.
TRIGCD	2	I	Manual burst mode trigger input for channels C and D. This pin can be configured via SPI to a manual trigger input signal for all four channels in burst mode, and can be connected to GND if not used. This pin has an internal 10-kΩ pulldown resistor.
DATA INTERFACE			
DAM	59	O	JESD204B serial data output pin for channel A
DAP	58		
DBM	62	O	JESD204B serial data output pin for channel B
DBP	61		
DCM	65	O	JESD204B serial data output pin for channel C
DCP	66		
DDM	68	O	JESD204B serial data output pin for channel D
DDP	69		
SYNCbABM	56	I	Synchronization input pin for JESD204B port channels A and B. This pin can be configured via SPI to a SYNCb signal for all four channels. This pin has an internal differential termination of 100 Ω.
SYNCbABP	55		
SYNCbCDM	71	I	Synchronization input pin for JESD204B port channels C and D. This pin can be configured via SPI to a SYNCb signal for all four channels. This pin has an internal differential termination of 100 Ω..
SYNCbCDP	72		
POWER SUPPLY			
AGND	21, 26, 29, 32	I	Analog ground
AVDD	9, 12, 15, 17, 20, 25, 30, 35, 38, 40, 43, 44, 46	I	Analog 1.15-V power supply
AVDD19	10, 16, 24, 31, 39, 45	I	Analog 1.9-V supply for analog buffer
DGND	3, 52, 60, 63, 67	I	Digital ground
DVDD	4, 8, 47,51, 57, 64, 70	I	Digital 1.15-V power supply
Thermal pad		—	Connect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVDD19	–0.3	2.1	V
	AVDD	–0.3	1.4	
	DVDD	–0.3	1.4	
	IOVDD	–0.2	1.4	
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INAP, INBP, INAM, INBM, INCP, INDP, INCM, INDM	–0.3	2.1	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	
	SYSREFP, SYSREFM, TRIGAB, TRIGCD	–0.3	AVDD + 0.3	
	SCLK, SEN, SDIN, RESET, SYNCbABP, SYNCbABM, SYNCbCDP, SYNCbCDM, PDN	–0.2	AVDD19 + 0.3	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage range	AVDD19		1.8	1.9	2	V
	AVDD		1.1	1.15	1.2	
	DVDD		1.1	1.15	1.2	
	IOVDD		1.1	1.15	1.2	
Analog inputs	Differential input voltage range			1.1		V_{PP}
	Input common-mode voltage (VCM)			1.3		V
Clock inputs	Input clock frequency, device clock frequency		400		1000	MHz
	Input clock amplitude differential ($V_{CLKP} – V_{CLKM}$)	Sine wave, ac-coupled		1.5		V_{PP}
		LVPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
	Input device clock duty cycle, default after reset		45%	50%	55%	
Temperature	Operating free-air, T_A		–40		100(3)	°C
	Operating junction, T_J			105	125(1)	
	Specified maximum, measured at the device footprint thermal pad on the printed circuit board, $T_{P\text{-}MAX}$				104.5(2)	

(1) Prolonged use above this junction temperature can increase the device failure-in-time (FIT) rate.
(2) The recommended maximum temperature at the PCB footprint thermal pad assumes the junction-to-package bottom thermal resistance, $R_{\theta JC(bot)}$ = 0.2°C/W, the thermal resistance of the device thermal pad connection to the PCB footprint is negligible, and the device power consumption is 2.5 W.
(3) Assumes system thermal design meets the T_J specification.

6.4 Thermal Information

THERMAL METRIC(1)		ADS58J64		UNIT
		RMP (VQFNP)	RHH (VQFN)	
		72 PINS	72 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	22.3	18.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (3)	5.1	5.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (3)	2.4	4.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter (4)	0.1	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter (5)	2.3	4.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (6)	0.2	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψJT, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψJB, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θJA , using a procedure described in JESD51-2a (sections 6 and 7).

6.5 Electrical Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, input clock frequency = 1 GHz, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
ADC sampling rate					1	GSPS
Resolution			14			Bits
POWER SUPPLY						
AVDD19	1.9-V analog supply		1.85	1.9	1.95	V
AVDD	1.15-V analog supply		1.1	1.15	1.2	V
DVDD	1.15-V digital supply		1.1	1.15	1.2	V
I_{AVDD19}	1.9-V analog supply current	100-MHz, full-scale input on all four channels		618		mA
I_{AVDD}	1.15-V analog supply current	100-MHz, full-scale input on all four channels		415		mA
I_{DVDD}	1.15-V digital supply current	Mode 8, 100 MHz, full-scale input on all four channels		629		mA
		Mode 3, 100 MHz, full-scale input on all four channels		730		
		Mode 0 and 2, 100 MHz, full-scale input on all four channels		674		
		Mode 1, 4, 6, and 7, 100 MHz, full-scale input on all four channels		703		
Pdis	Total power dissipation	Mode 8, 100 MHz, full-scale input on all four channels		2.37		W
		Mode 3, 100 MHz, full-scale input on all four channels		2.49		
		Mode 0 and 2, 100 MHz, full-scale input on all four channels		2.42		
		Mode 1, 4, 6, and 7, 100 MHz, full-scale input on all four channels		2.46		
	Global power-down power dissipation	Full-scale input on all four channels		120		mW
ANALOG INPUTS						
	Differential input full-scale voltage			1.1		V_{PP}
	Input common-mode voltage			1.3		V
	Differential input resistance	At f_{IN} = dc		4		kΩ
	Differential input capacitance			2.5		pF
	Analog input bandwidth (3 dB)			1000		MHz
ISOLATION						
	Crosstalk(1) isolation between near channels (channels A and B are near to each other, channels C and D are near to each other)	f_{IN} = 10 MHz		75		dBFS
		f_{IN} = 100 MHz		75		
		f_{IN} = 170 MHz		74		
		f_{IN} = 270 MHz		72		
		f_{IN} = 370 MHz		71		
		f_{IN} = 470 MHz		70		

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, input clock frequency = 1 GHz, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crosstalk(1) isolation between far channels (channels A and B are far from channels C and D)	f_{IN} = 10 MHz		110		dBFS
	f_{IN} = 100 MHz		110		
	f_{IN} = 170 MHz		110		
	f_{IN} = 270 MHz		110		
	f_{IN} = 370 MHz		110		
	f_{IN} = 470 MHz		110		
CLOCK INPUT					
Internal clock biasing	CLKINP and CLKINM pins are connected to the internal biasing voltage through a 5-kΩ resistor		0.7		V

(1) Crosstalk is measured with a –1-dBFS input signal on aggressor channel and no input on the victim channel.

6.6 AC Performance

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, input clock frequency = 1 GHz, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	14-BIT BURST MODE (DDC Mode 8)			DECIMATE-BY-4 (DDC Mode 2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		69.9			72.2		dBFS
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		69.6			71.8		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		69.2			71.8		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS	66.5	69.6			71		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		69.3			71.7		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS		68.7			71.3		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		68.4			69.8		
NSD	Noise spectral density	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		–153.9			–153.2		dBFS/Hz
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		–153.6			–152.8		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		–153.2			–152.7		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS	–150.5	–153.6			–153.2		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		–152.8			–152.7		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS		–152.5			–152.2		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		–151.5			–151		
SFDR(1)	Spurious-free dynamic range	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		83			83		dBc
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		81			100		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		87			100		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS	78	88			98		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		79			98		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS, input clock frequency = 983.04 MHz		82			70		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		78			76		
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		68.5			70.6		dBFS
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		68.5			70.6		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		68.2			72.2		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS		68.5			73		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		68.9			72.3		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS		68			68.2		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		68			69		

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, input clock frequency = 1 GHz, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	14-BIT BURST MODE (DDC Mode 8)			DECIMATE-BY-4 (DDC Mode 2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2(1)	Second-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		–83			–90		dBc
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		–82			–100		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		–85			–98		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS	–78	–86			–100		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		–82			–100		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS input clock frequency = 983.04 MHz		–82			–69		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		–100			–94		
HD3(1)	Third-order harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		–83			–85		dBc
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		–81			–100		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		–92			–100		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS	–78	–92			–100		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		–90			–100		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS		–90			–100		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		–80			–79		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		95			–100		dBFS
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		95			–92		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		95			–100		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS	87	95			–98		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		95			–100		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS		95			–100		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		93			–100		
THD(1)	Total harmonic distortion	f_{IN} = 10 MHz, A_{IN} = –1 dBFS		–81			–83		dBc
		f_{IN} = 70 MHz, A_{IN} = –1 dBFS		–79			–100		
		f_{IN} = 190 MHz, A_{IN} = –1 dBFS		–83			–100		
		f_{IN} = 190 MHz, A_{IN} = –3 dBFS		–85			–100		
		f_{IN} = 300 MHz, A_{IN} = –3 dBFS		–81			–100		
		f_{IN} = 370 MHz, A_{IN} = –3 dBFS		–76			–68		
		f_{IN} = 470 MHz, A_{IN} = –3 dBFS		–82			–80		
IMD3	Two-tone, third-order intermodulation distortion	f_1 = 185 MHz, f_2 = 190 MHz, A_{IN} = –10 dBFS		–90			–87		dBFS
		f_1 = 365 MHz, f_2 = 370 MHz, A_{IN} = –10 dBFS		–90			–94		
		f_1 = 465 MHz, f_2 = 470 MHz, A_{IN} = –10 dBFS		–85			–85		

(1) Harmonic distortion performance can be significantly improved by using the frequency planning explained in the *Section 8.1.3* section.

6.7 Digital Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, input clock frequency = 1 GHz, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SEN, SDIN, PDN, TRIGAB, TRIGCD)[1]						
V_{IH}	High-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels	0.8			V
V_{IL}	Low-level input voltage	All digital inputs support 1.2-V and 1.8-V logic levels			0.4	V
I_{IH}	High-level input current	SEN		0		μA
		RESET, SCLK, SDIN, PDN, TRIGAB, TRIGCD		50		
I_{IL}	Low-level input current	SEN		50		μA
		RESET, SCLK, SDIN, PDN, TRIGAB, TRIGCD		0		
	Input capacitance			4		pF
DIGITAL INPUTS						
V_D	Differential input voltage	SYSREFP, SYSREFM	0.35	0.45	0.55	V
		SYNCbABM, SYNCbABP, SYNCbCDM, SYNCbCDP	0.35		1.3	
$V_{(CM\_DIG)}$	Common-mode voltage for SYSREF	SYSREFP, SYSREFM	0.9	1.2	1.4	V
		SYNCbABM, SYNCbABP, SYNCbCDM, SYNCbCDP		1.2		
DIGITAL OUTPUTS (SDOUT, TRDYAB, TRDYCD)						
V_{OH}	High-level output voltage	100-μA current	AVDD19 – 0.2			V
V_{OL}	Low-level output voltage	100-μA current			0.2	V
DIGITAL OUTPUTS (JESD204B Interface: DxP, DxM)[2]						
V_{OD}	Output differential voltage	With default swing setting		700		mV_{PP}
V_{OC}	Output common-mode voltage			450		mV
	Transmitter short-circuit current	Transmitter pins shorted to any voltage between –0.25 V and 1.45 V	–100		100	mA
z_{os}	Single-ended output impedance			50		Ω
	Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) The RESET, SCLK, SDIN, and PDN pins have a 20-kΩ (typical) internal pulldown resistor to ground, and the SEN pin has a 20-kΩ (typical) pullup resistor to IOVDD.
(2) 50-Ω, single-ended external termination to IOVDD.

6.8 Timing Characteristics

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, input clock frequency = 1 GHz, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

			MIN	TYP	MAX	UNITS
SAMPLE TIMING CHARACTERISTICS						
	Aperture delay		0.55		0.92	ns
	Aperture delay matching between two channels on the same device			±100		ps
	Aperture delay matching between two devices at the same temperature and supply voltage			±100		ps
	Aperture jitter			100		f_S rms
	Wake-up time	Global power-down		10		ms
		Pin power-down (fast power-down)		5		µs
	Data latency: ADC sample to digital output	Burst mode		116		Input clock cycles
		DDC mode 0		204		
t_{SU_SYSREF}	Setup time for SYSREF, referenced to input clock rising edge		350		900	ps
t_{H_SYSREF}	Hold time for SYSREF, referenced to input clock rising edge		100			ps
JESD OUTPUT INTERFACE TIMING CHARACTERISTICS						
	Unit interval		100			ps
	Serial output data rate				10	Gbps
	Total jitter for BER of 1E-15 and lane rate = 10 Gbps			24		ps
	Random jitter for BER of 1E-15 and lane rate = 10 Gbps			0.95		ps rms
	Deterministic jitter for BER of 1E-15 and lane rate = 10 Gbps			8.8		ps, pk-pk
t_R, t_F	Data rise time, data fall time: rise and fall times measured from 20% to 80%, differential output waveform, 2.5 Gbps ≤ bit rate ≤ 10 Gbps			35		ps

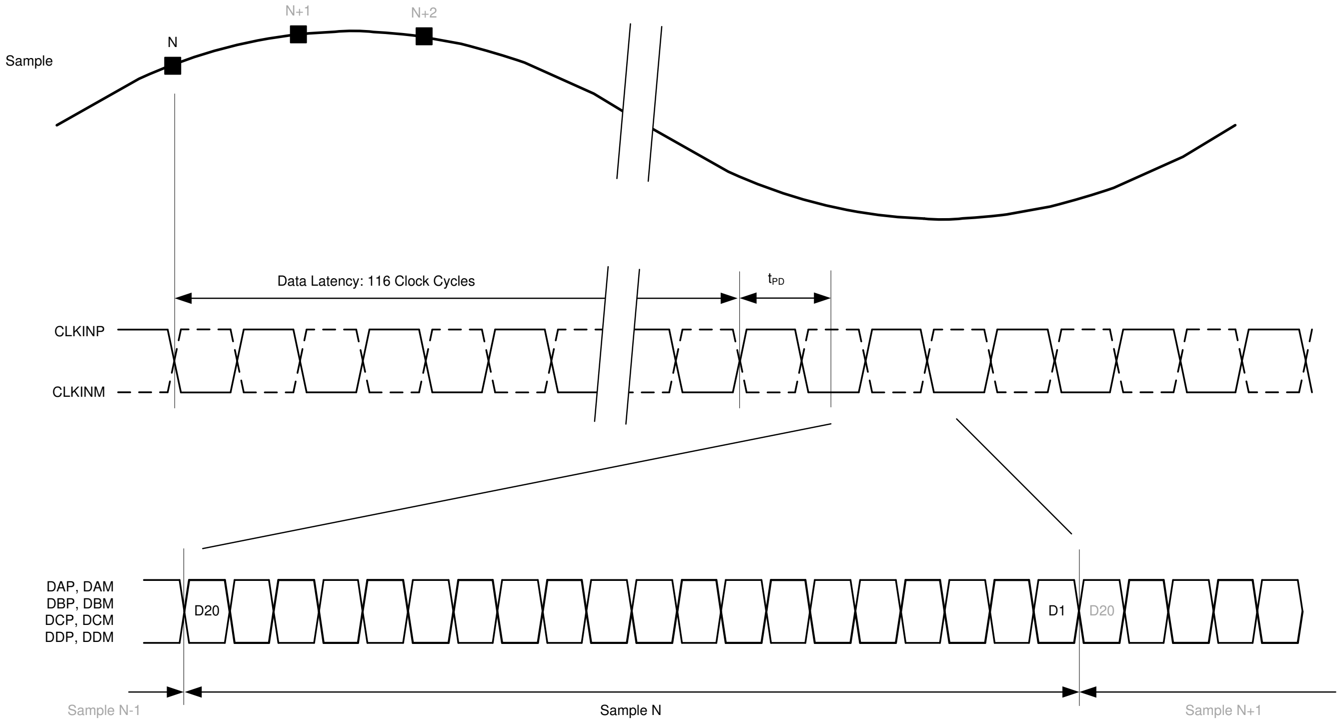
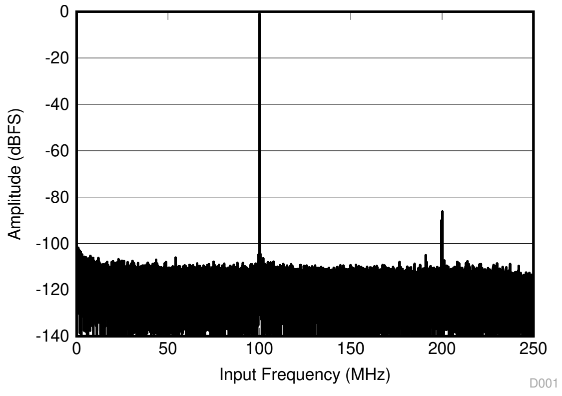


Figure 6-1. Latency Timing Diagram in Burst Mode

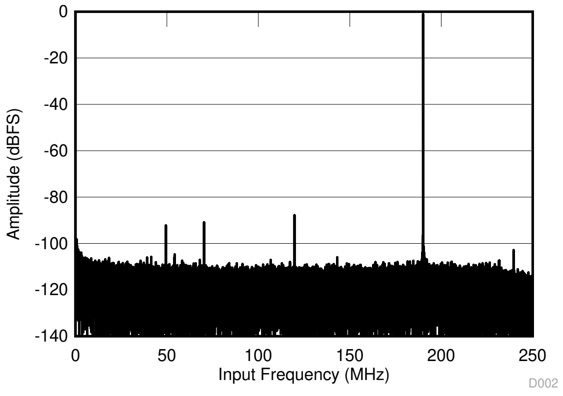
6.9 Typical Characteristics: 14-Bit Burst Mode

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)



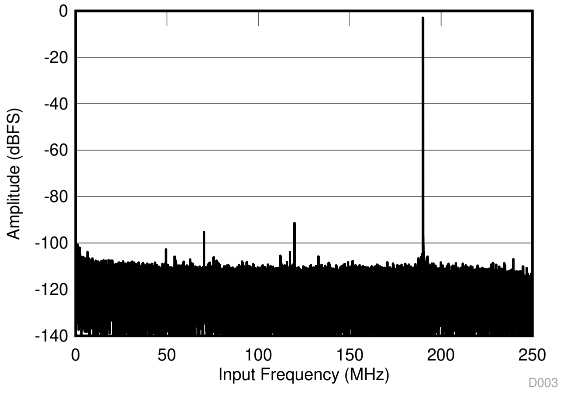
f_{IN} = 100 MHz, A_{IN} = –1 dBFS, SNR = 69.57 dBFS, SFDR = 85.23 dBc, SFDR = 102.09 dBc (non 23)

Figure 6-2. FFT for 100-MHz Input Signal



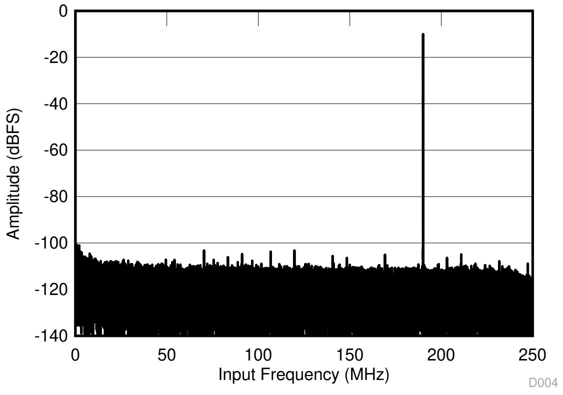
f_{IN} = 190 MHz, A_{IN} = –1 dBFS, SNR = 69.23 dBFS, SFDR = 86.83 dBc, SFDR = 91.23 dBc (non 23)

Figure 6-3. FFT for 190-MHz Input Signal



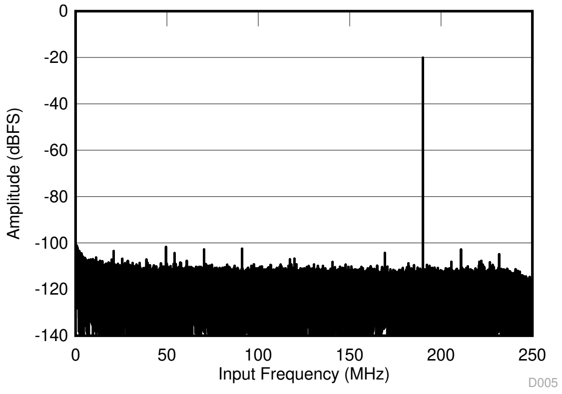
f_{IN} = 190 MHz, A_{IN} = –3 dBFS, SNR = 69.60 dBFS, SFDR = 88.45 dBc, SFDR = 99.78 dBc (non 23)

Figure 6-4. FFT for 190-MHz Input Signal



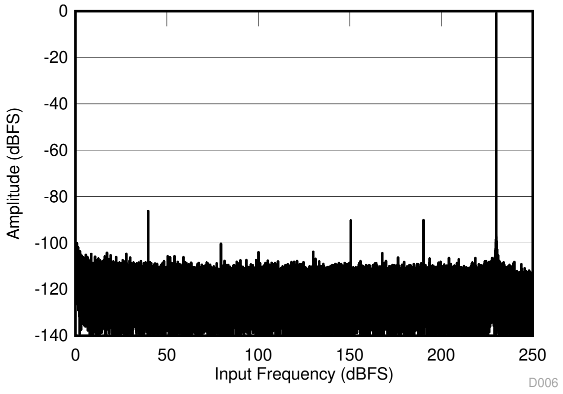
f_{IN} = 190 MHz, A_{IN} = –10 dBFS, SNR = 70.05 dBFS, SFDR = 93.27 dBc, SFDR = 97.26 dBc (non 23)

Figure 6-5. FFT for 190-MHz Input Signal



f_{IN} = 190 MHz, A_{IN} = –20 dBFS, SNR = 70.23 dBFS, SFDR = 81.71 dBc, SFDR = 81.71 dBc (non 23)

Figure 6-6. FFT for 190-MHz Input Signal

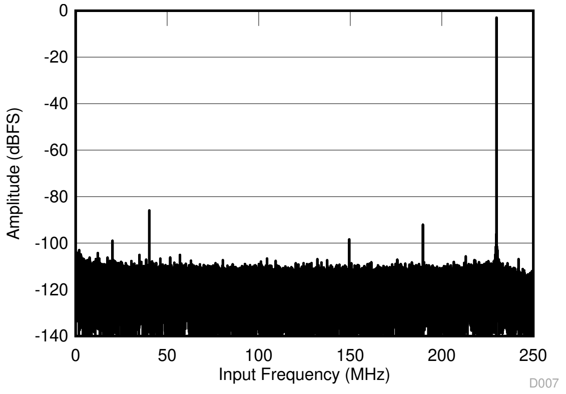


f_{IN} = 230 MHz, A_{IN} = –1 dBFS, SNR = 69.17 dBFS, SFDR = 85.29 dBc, SFDR = 89.30 dBc (non 23)

Figure 6-7. FFT for 230-MHz Input Signal

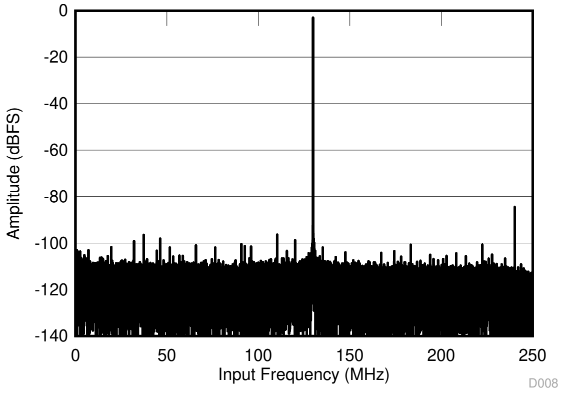
6.9 Typical Characteristics: 14-Bit Burst Mode (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)



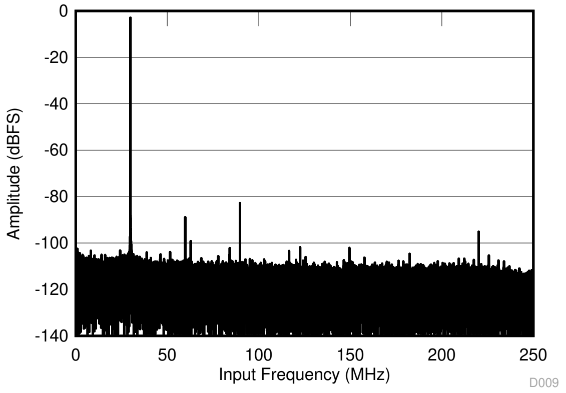
f_{IN} = 270 MHz, A_{IN} = –3 dBFS, SNR = 69.27 dBFS, SFDR = 82.98 dBc, SFDR = 95.4 dBc (non 23)

Figure 6-8. FFT for 270-MHz Input Signal



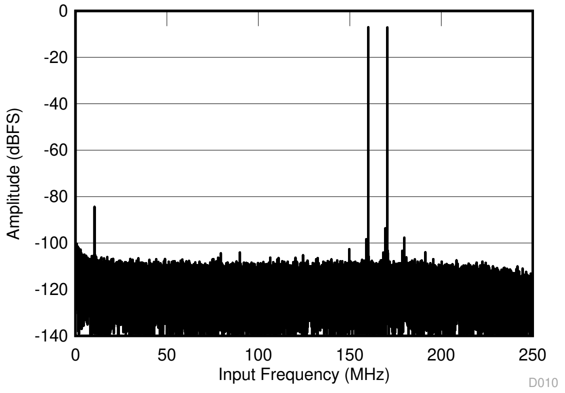
f_{IN} = 370 MHz, A_{IN} = –3 dBFS, SNR = 68.36 dBFS, SFDR = 81.37 dBc, SFDR = 97.28 dBc (non 23)

Figure 6-9. FFT for 370-MHz Input Signal



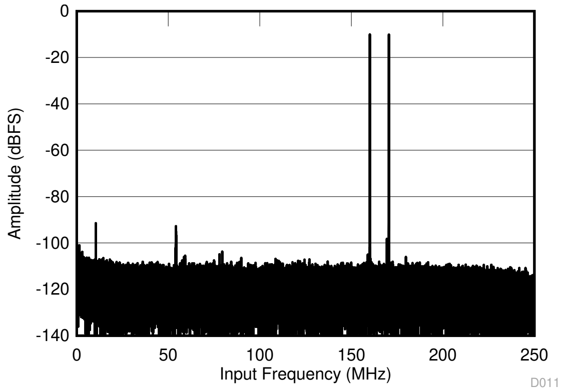
f_{IN} = 470 MHz, A_{IN} = –3 dBFS, SNR = 68.21 dBFS, SFDR = 79.85 dBc, SFDR = 99.12 dBc (non 23)

Figure 6-10. FFT for 470-MHz Input Signal



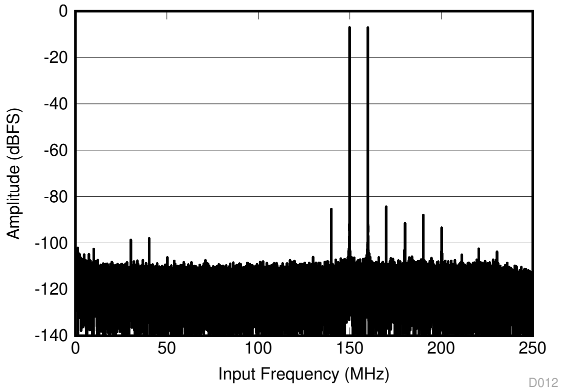
f_{IN1} = 160 MHz, f_{IN2} = 170 MHz, IMD = 102.68 dBFS, each tone at –7 dBFS

Figure 6-11. FFT for Two-Tone Input Signal



f_{IN1} = 160 MHz, f_{IN2} = 170 MHz, IMD = 103.44 dBFS, each tone at –10 dBFS

Figure 6-12. FFT for Two-Tone Input Signal

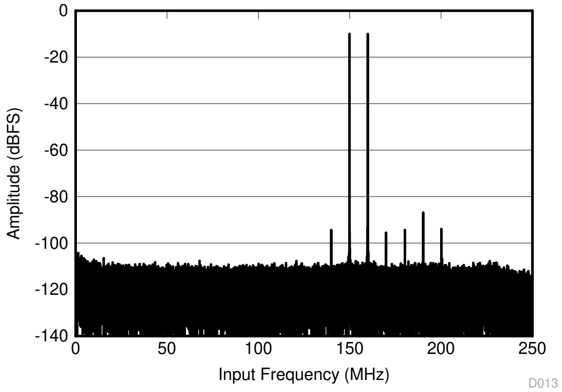


f_{IN1} = 340 MHz, f_{IN2} = 350 MHz, IMD = 84.34 dBFS, each tone at –7 dBFS

Figure 6-13. FFT for Two-Tone Input Signal

6.9 Typical Characteristics: 14-Bit Burst Mode (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)



f_{IN1} = 340 MHz, f_{IN2} = 350 MHz, IMD = 95.08 dBFS, each tone at –10 dBFS

Figure 6-14. FFT for Two-Tone Input Signal

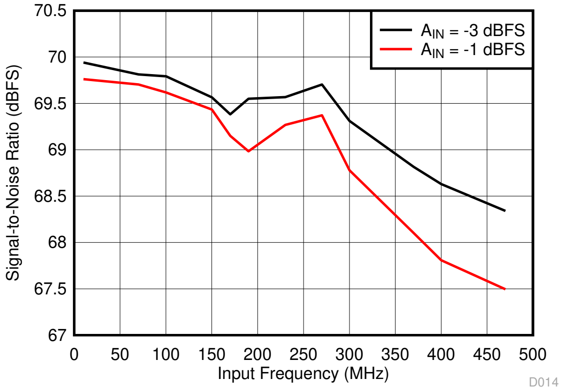


Figure 6-15. SNR vs Input Frequency

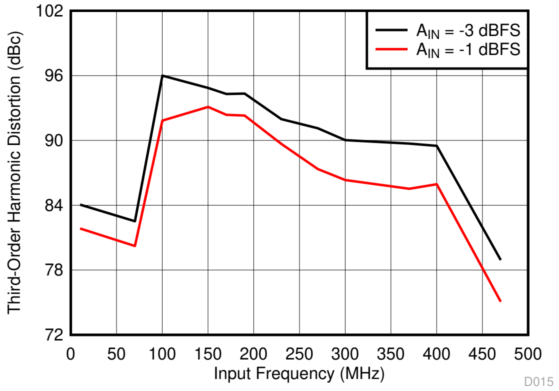


Figure 6-16. HD3 vs Input Frequency

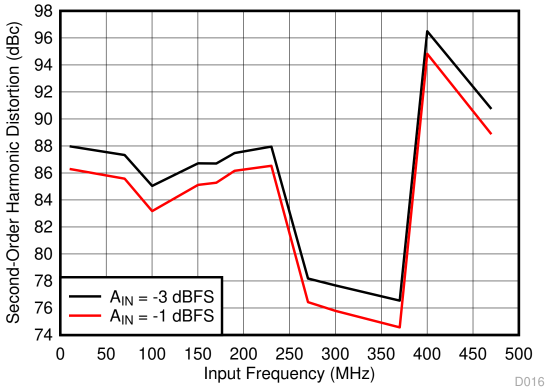


Figure 6-17. HD2 vs Input Frequency

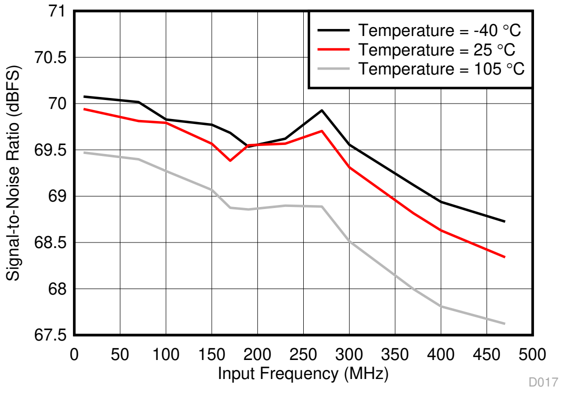


Figure 6-18. SNR vs Input Frequency and Temperature

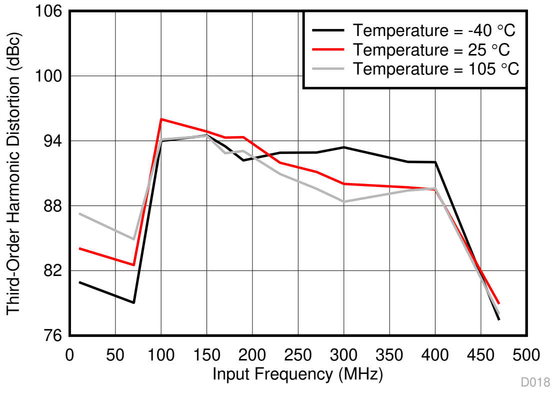


Figure 6-19. HD3 vs Input Frequency and Temperature

6.9 Typical Characteristics: 14-Bit Burst Mode (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

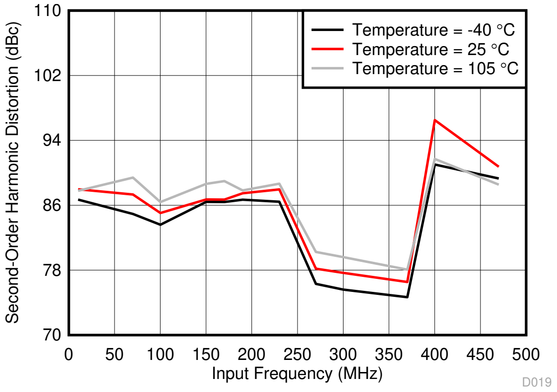


Figure 6-20. HD2 vs Input Frequency and Temperature

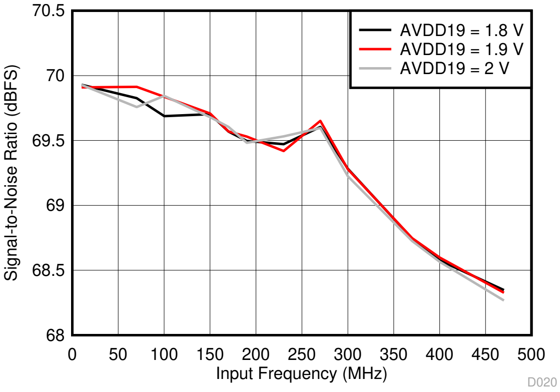


Figure 6-21. SNR vs Input Frequency and AVDD19 Supply

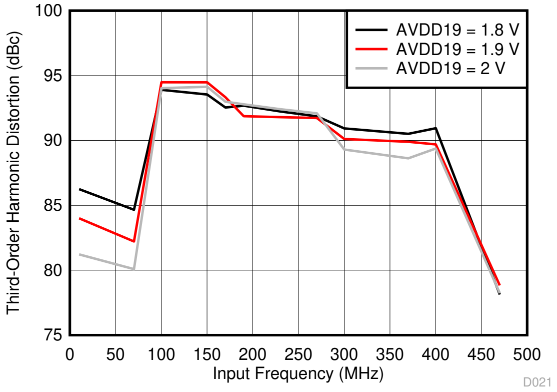


Figure 6-22. HD3 vs Input Frequency and AVDD19 Supply

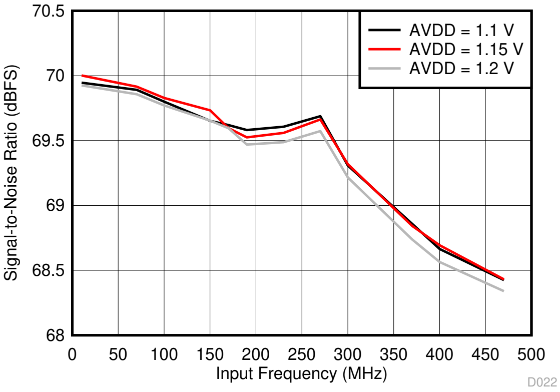


Figure 6-23. SNR vs Input Frequency and AVDD Supply

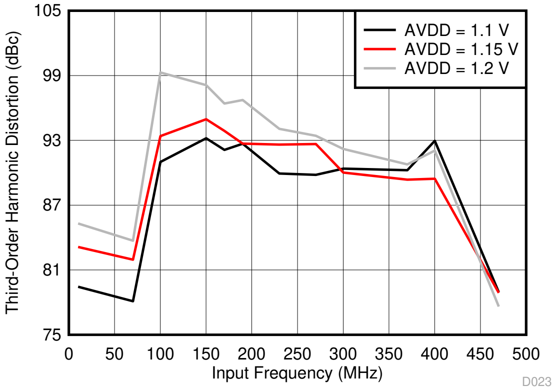


Figure 6-24. HD3 vs Input Frequency and AVDD Supply

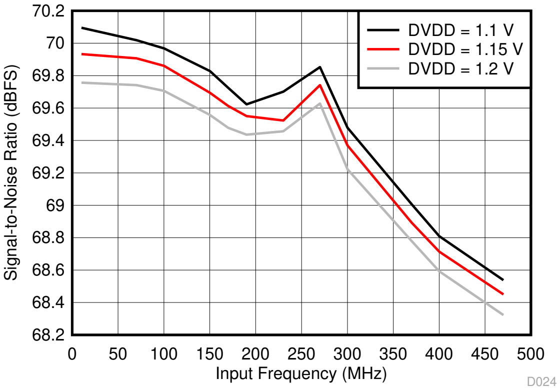


Figure 6-25. SNR vs Input Frequency and DVDD Supply

6.9 Typical Characteristics: 14-Bit Burst Mode (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)

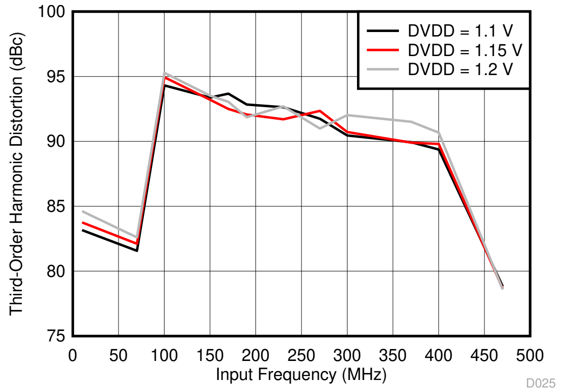
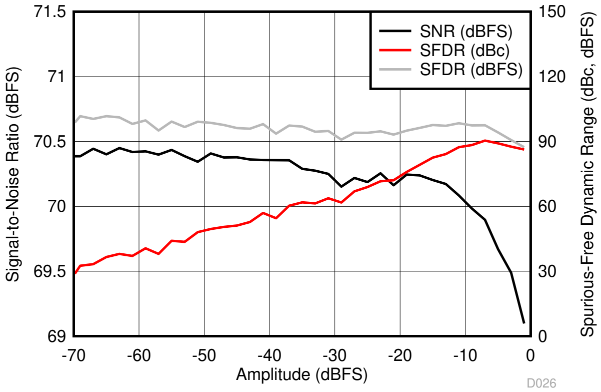
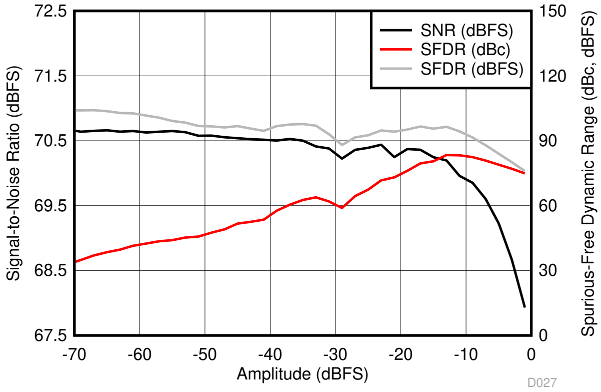


Figure 6-26. HD3 vs Input Frequency and DVDD Supply



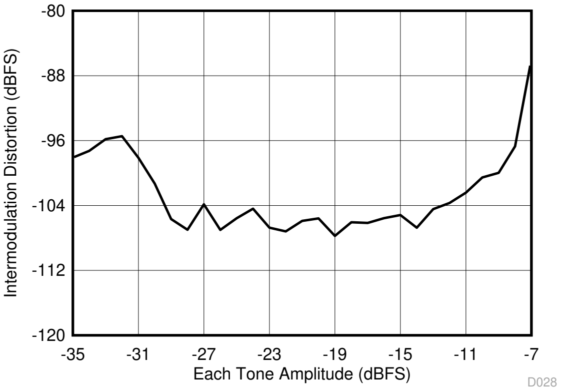
f_{IN} = 190 MHz

Figure 6-27. Performance vs Input Signal Amplitude



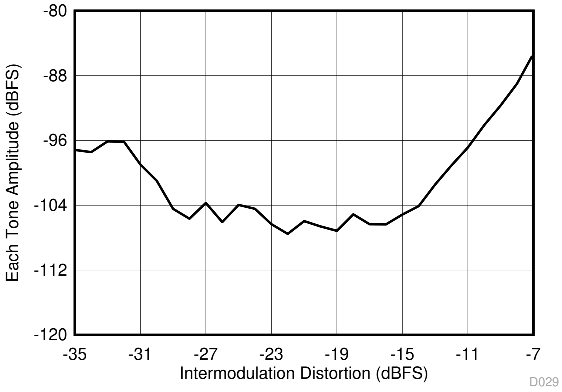
f_{IN} = 370 MHz

Figure 6-28. Performance vs Input Signal Amplitude



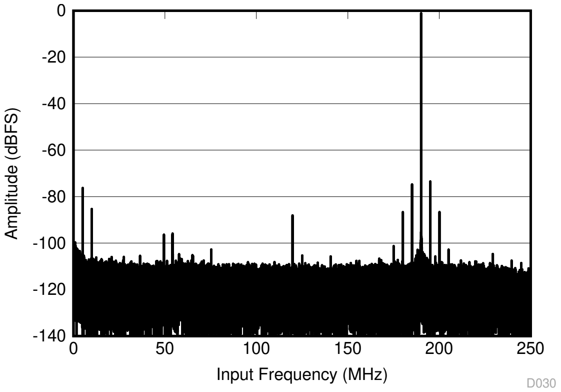
f_{IN1} = 160 MHz, f_{IN2} = 170 MHz

Figure 6-29. IMD vs Input Amplitude



f_{IN1} = 340 MHz, f_{IN2} = 350 MHz

Figure 6-30. IMD vs Input Amplitude

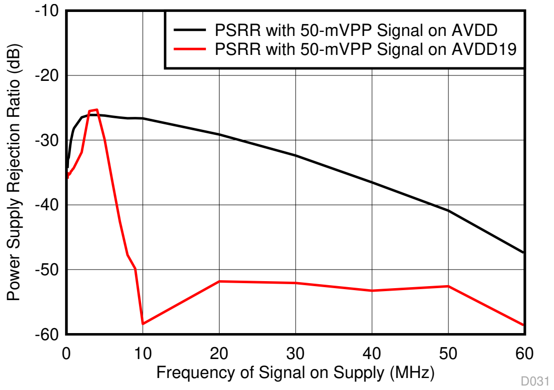


f_{IN} = 190 MHz, A_{IN} = –1 dBFS, f_{Noise} = 5 MHz, A_{Noise} = 50 mV_{PP}, SFDR = 73.5 dBFS

Figure 6-31. Power-Supply Rejection Ratio FFT for 50-mV Noise on AVDD Supply

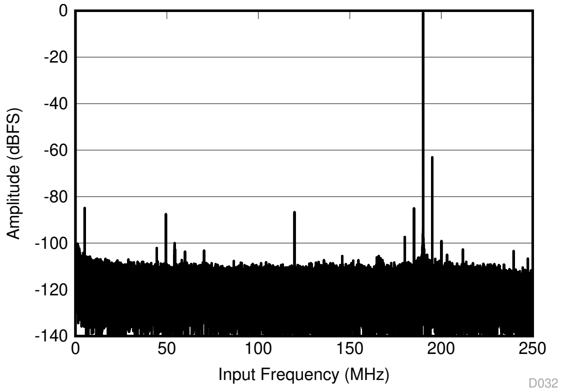
6.9 Typical Characteristics: 14-Bit Burst Mode (continued)

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)



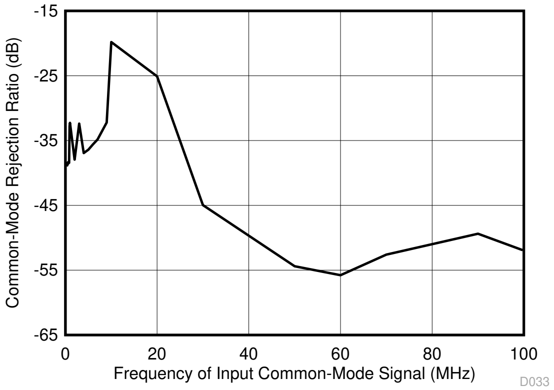
f_{IN} = 190 MHz, A_{IN} = –1 dBFS, f_{Noise} = 5 MHz, A_{Noise} = 50 mV_{PP}

Figure 6-32. PSRR vs Power Supplies



f_{IN} = 190 MHz, A_{IN} = –1 dBFS, f_{Noise} = 5 MHz, A_{Noise} = 50 mV_{PP}, SFDR = 63.12 dBFS

Figure 6-33. Common-Mode Rejection Ratio FFT



f_{IN} = 190 MHz, A_{IN} = –1 dBFS, f_{Noise} = 5 MHz, A_{Noise} = 50 mV_{PP}

Figure 6-34. CMRR vs Noise Frequency

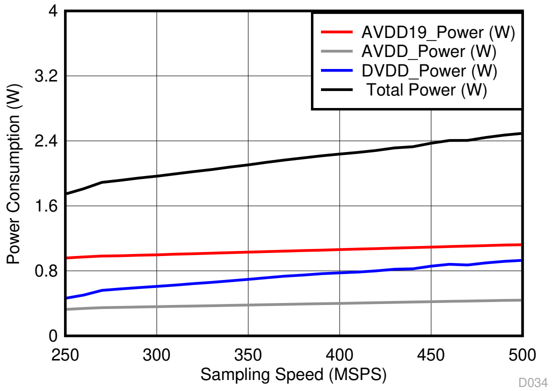
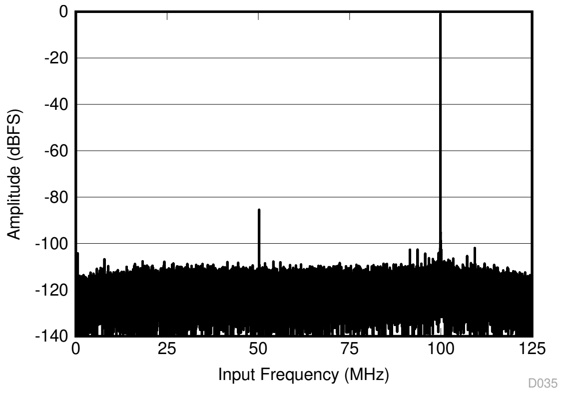


Figure 6-35. Power Consumption vs Input Clock Rate

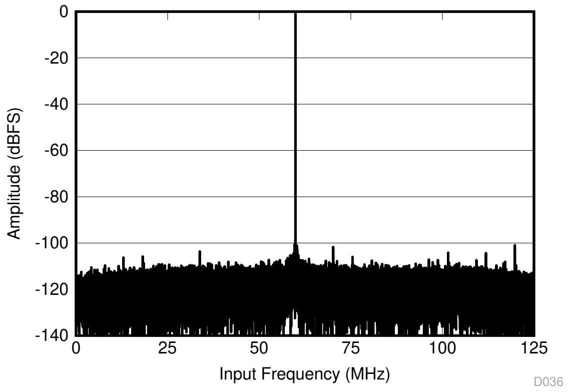
6.10 Typical Characteristics: Mode 2

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +100°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)



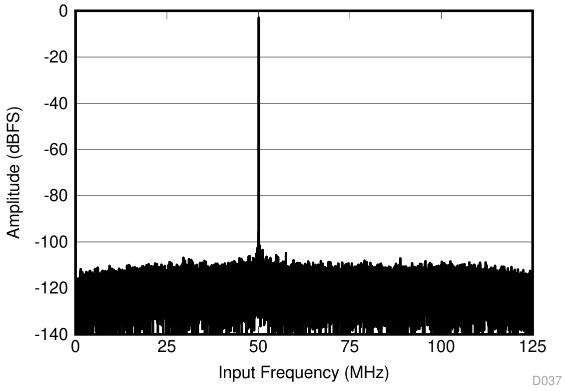
f_{IN} = 150 MHz, A_{IN}= –1 dBFS, SNR = 72.85 dBFS, SFDR = 84.41 dBc, SFDR = 100.99 dBc (non 23)

Figure 6-36. FFT for 150-MHz Input Signal



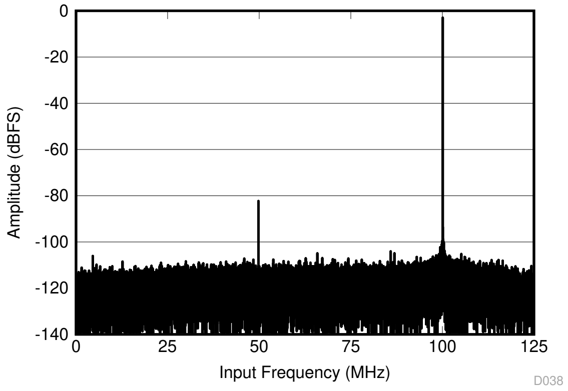
f_{IN} = 190 MHz, A_{IN}= –1 dBFS, SNR = 72.37 dBFS, SFDR = 99.95 dBc, SFDR = 100.76 dBc (non 23)

Figure 6-37. FFT for 190-MHz Input Signal



f_{IN} = 300 MHz, A_{IN}= –3 dBFS, SNR = 72.3 dBFS, SFDR = 100.31 dBc, SFDR = 100.75 dBc (non 23)

Figure 6-38. FFT for 300-MHz Input Signal

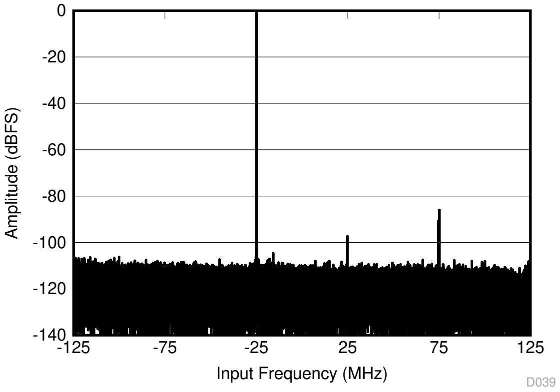


f_{IN} = 350 MHz, A_{IN}= –3 dBFS, SNR = 72.02 dBFS, SFDR = 79.23 dBc, SFDR = 96.42 dBc (non 23)

Figure 6-39. FFT for 350-MHz Input Signal

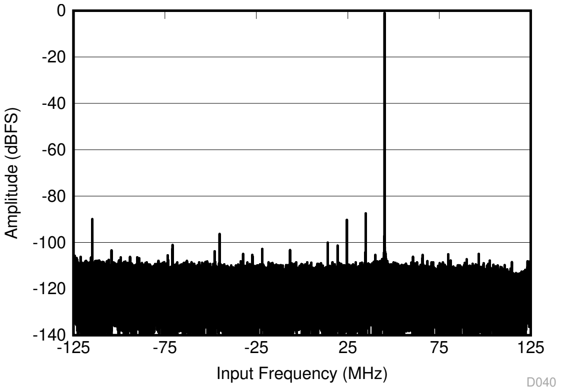
6.11 Typical Characteristics: Mode 0

typical values are at T_A = 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = +85°C, device sampling frequency = 1 GSPS, mode 8: 2x decimation with burst mode output, 50% clock duty cycle, AVDD19 = 1.9 V, AVDD = DVDD = 1.15 V, –1-dBFS differential input, and f_{IN} = 190 MHz (unless otherwise noted)



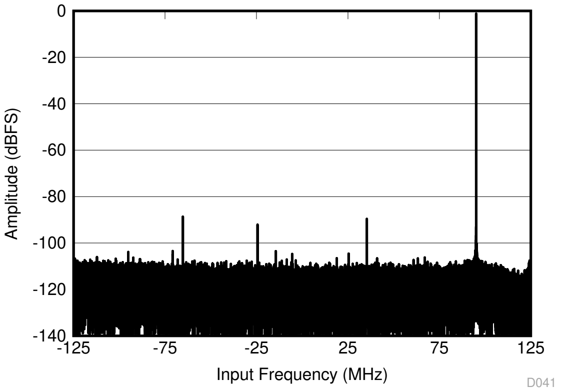
f_{IN} = 100 MHz, A_{IN}= –1 dBFS, SNR = 70.16 dBFS, SFDR = 84.95 dBc, SFDR = 95.41 dBc (non 23)

Figure 6-40. FFT for 100-MHz Input Signal



f_{IN} = 170 MHz, A_{IN}= –1 dBFS, SNR = 69.35 dBFS, SFDR = 86.46 dBc, SFDR = 89.27 dBc (non 23)

Figure 6-41. FFT for 170-MHz Input Signal



f_{IN} = 220 MHz, A_{IN}= –1 dBFS, SNR = 69.27 dBFS, SFDR = 87.66 dBc, SFDR = 91.04 dBc (non 23)

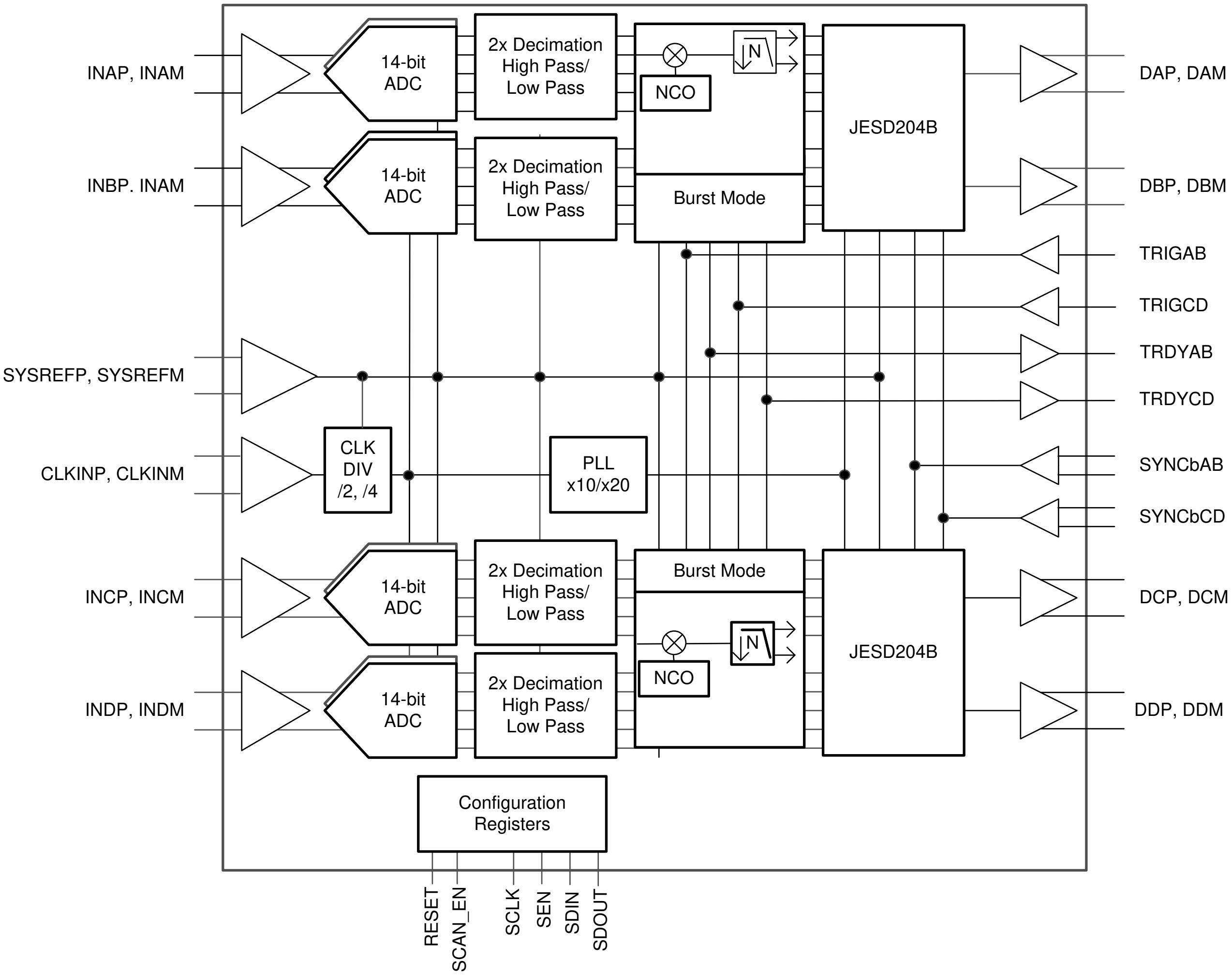
Figure 6-42. FFT for 220-MHz Input Signal

7 Detailed Description

7.1 Overview

The ADS58J64 is a quad-channel device with a complex digital down-converter (DDC) and digital decimation to allow flexible signal processing to suit different usage cases. Each channel is composed of two interleaved analog-to-digital converters (ADCs) sampling at half the input clock rate. The 2x interleaved data are decimated by 2 to provide a processing gain of 3 dB. The decimation filter can be configured as low pass (default) or high pass. The half-rate (with regards to the input clock) data are available on the output, in burst mode (DDC mode = 8) as a stream of high (14-bit) and low (9-bit) resolution samples. Burst mode can be enabled by device programming along with other options (such as the number of high- and low-resolution samples, and trigger mode as either automatic or pin-controlled). In default mode, the device operates in DDC mode 0, where the input is mixed with a constant frequency of $-f_S$ / 4 and is given out as complex IQ. The different operational modes modes of the ADS58J64 are listed in Table 7-1.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Inputs

The ADS58J64 analog signal inputs are designed to be driven differentially. The analog input pins have internal analog buffers that drive the sampling circuit. As a result of the analog buffer, the input pins present a high-impedance input across a very wide frequency range to the external driving source that enables great flexibility in the external analog filter design as well as excellent 50-Ω matching for RF applications. The buffer also helps isolate the external driving circuit from the internal switching currents of the sampling circuit, resulting in a more constant SFDR performance across input frequencies. The common-mode voltage of the signal inputs is internally biased to 1.3 V using 2-kΩ resistors to allow for ac-coupling of the input drive network. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.275 V) and (VCM – 0.275 V), resulting in a 1.1-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 1000 MHz.

7.3.2 Recommended Input Circuit

In order to achieve optimum ac performance, the following circuitry (shown in Figure 7-1) is recommended at the analog inputs.

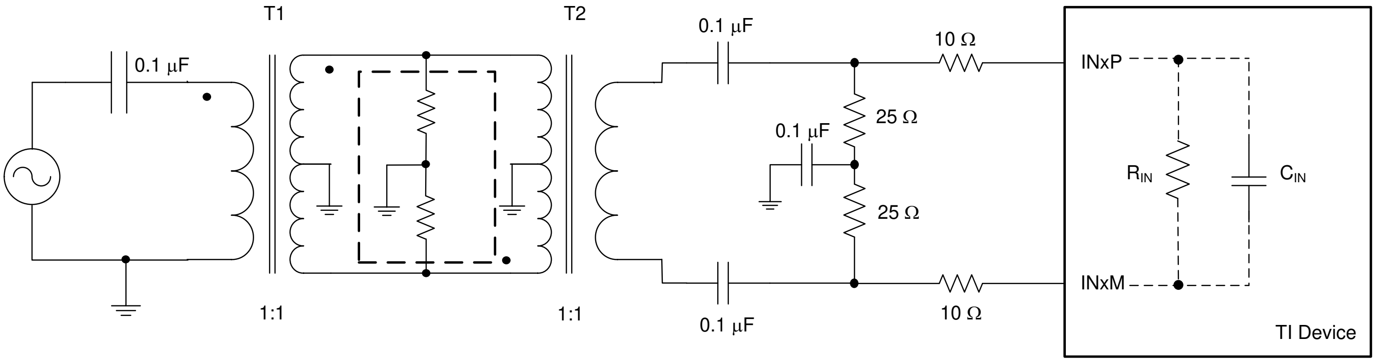


Figure 7-1. Analog Input Driving Circuit

7.3.3 Clock Input

The clock inputs of the ADS58J64 supports LVDS and LVPECL standards. The CLKP, CLKM inputs have an internal termination of 100 Ω. The clock inputs must be ac-coupled because the input pins are self-biased to a common-mode voltage of 0.7 V, as shown in Figure 7-2 and Figure 7-3.

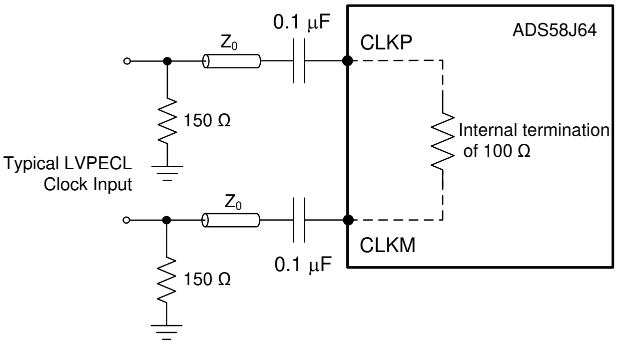


Figure 7-2. LVPECL Clock Driving Circuit

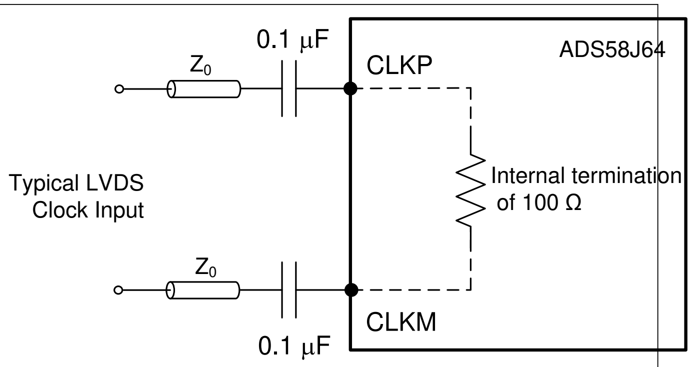


Figure 7-3. LVDS Clock Driving Circuit

7.4 Device Functional Modes

7.4.1 Digital Features

The ADS58J64 has two stages of digital decimation filters, as shown in Figure 7-4. The first stage is mandatory and decimates by 2, and can be configured as either a low-pass or high-pass filter. The second stage decimation supports real to complex quadrature demodulation and decimation by 2 or 4. After decimation, the complex signal can be converter back to a real signal through digital quadrate modulation at a frequency of f_{OUT} / 4, where f_{OUT} is the sample frequency after decimation.

Optionally, a burst mode output can be used to output the decimate-by-2 data directly.

The four channels can be configured as pairs (A, B and C, D) to either burst or decimation mode. If all four channels are in decimation mode, then the decimation setting must be the same decimation for all four channels.

All modes of operation and the maximum bandwidth provided at a sample rate of 491.52 MSPS and 368.64 MSPS are listed in Table 7-1. The first stage decimation filter prior to the 16-bit numerically controlled oscillator (NCO) is a noise suppression filter with 45% pass-band bandwidth relative to the input sample rate, less than 0.2-dB ripple, and approximately 40-dB stop-band attenuation. This filter is only used to reduce the ADC output rate from 1 GSPS to 500 MSPS prior to the second stage decimation filter or burst mode. Some analog filtering of other Nyquist zones after the first stage decimation filter is expected to be required.

The second stage filter has a pass-band bandwidth of 81.4% relative to the output sample rate, supporting a 200-MHz bandwidth with a 245.76-MSPS complex output rate.

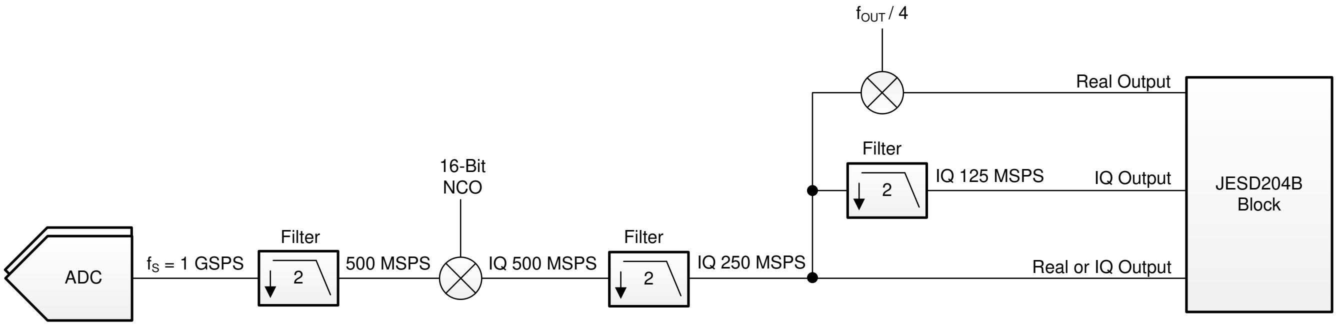


Figure 7-4. ADS58J64 Channel (1 of 4) Block Diagram

Table 7-1. ADS58J64 Operating Modes

OPERATING MODE	DESCRIPTION	1ST STAGE DECIMATION	DIGITAL MIXER	2ND STAGE DECIMATION	BANDWIDTH AT 491.52 MSPS	BANDWIDTH AT 368.64 MSPS	OUTPUT MIXER	OUTPUT FORMAT	MAX OUTPUT RATE
0	Decimation	2	$\pm f_S$ / 4	2	200 MHz	150 MHz	—	Complex	250 MSPS
1		2	16-bit NCO	2	200 MHz	150 MHz	—	Complex	250 MSPS
2		2	—	2	100 MHz (LP, LP or HP, HP), 75 MHz (HP, LP or LP, HP)	75 MHz, 56.25 MHz	—	Real	250 MSPS
3		2	16-bit NCO	Bypass	200 MHz	150 MHz	f_{OUT} / 4	Real	500 MSPS
4		2	16-bit NCO	2	100 MHz	75 MHz	f_{OUT} / 4	Real	250 MSPS
5		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6		2	16-bit NCO	4	100 MHz	75 MHz	—	Complex	125 MSPS
7		2	16-bit NCO	2	100 MHz	75 MHz	f_{OUT} / 4	Real with zero insertion	500 MSPS
8	Burst mode	—	—	—	223 MHz	167 MHz	—	Real	500 MSPS

7.4.1.1 Numerically Controlled Oscillators (NCOs) and Mixers

The ADS58J64 is equipped with a complex numerically-controlled oscillator. The oscillator generates a complex exponential sequence: $x[n] = e^{j\omega n}$. The frequency (ω) is specified by the 16-bit register setting. The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier down to 0 Hz.

The NCO frequency setting is set by the 16-bit register value, NCO_FREQ[n]:

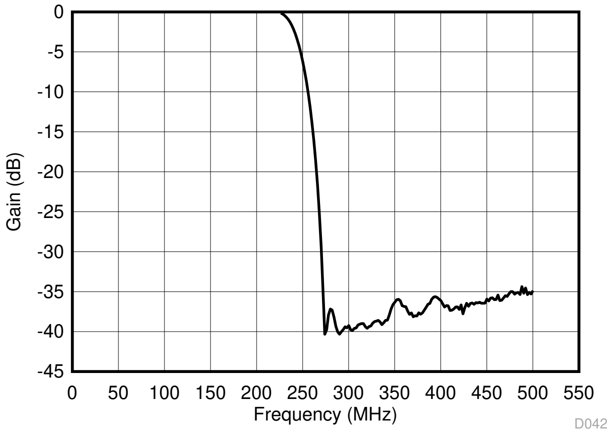
$$f_{NCO} = \frac{\text{NCO Frequency }[n] \times f_S}{2^{16}} \tag{1}$$

7.4.1.2 Decimation Filter

The ADS58J64 has two decimation filters (decimate-by-2) in the data path. The first stage of the decimation filter is non-programmable and is used in all functional modes. The second stage of decimation, available in DDC mode 2 and 6, can be used to obtain noise and linearity improvement for low bandwidth applications.

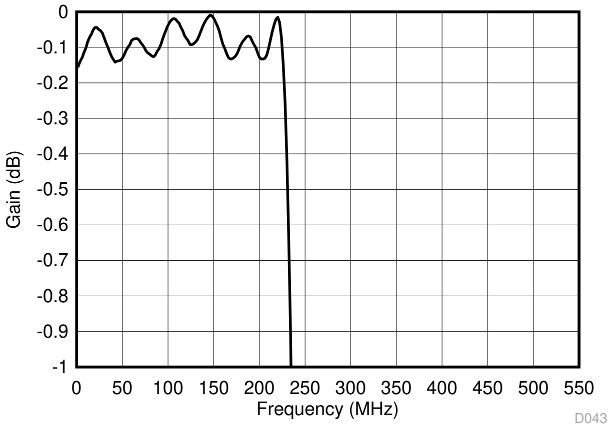
7.4.1.2.1 Stage-1 Filter

The first stage filter is used for decimation of the 2x interleaved data from f_{CLK} to f_{CLK} / 2. The frequency response and pass-band ripple of the first stage decimation filter are shown in Figure 7-5 and Figure 7-6, respectively.



Input clock rate = 1 GHz

Figure 7-5. Decimation Filter Response vs Frequency

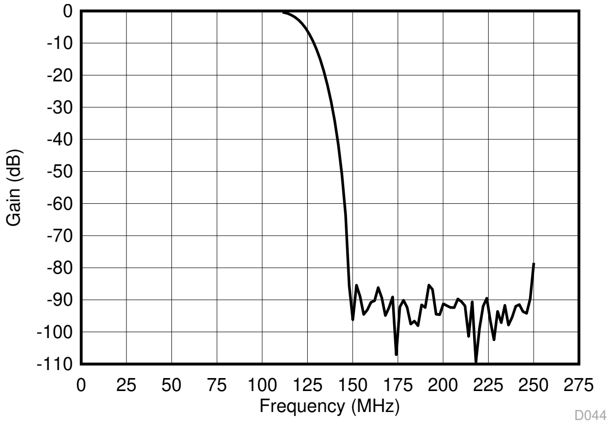


Input clock rate = 1 GHz

Figure 7-6. Decimation Filter Pass-Band Ripple vs Frequency

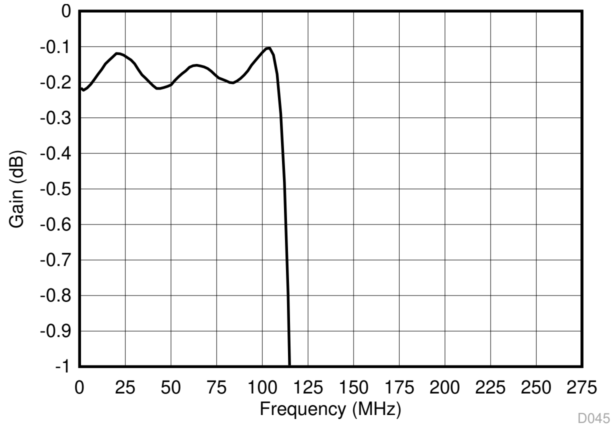
7.4.1.2.2 Stage-2 Filter

The second stage filter is used for decimating the data from a sample rate of f_{CLK} / 2 to f_{CLK} / 4. The frequency response and pass-band ripple of the second stage filter are shown in Figure 7-7 and Figure 7-8, respectively.



Input clock rate (f_{CLK}) = 1 GHz

Figure 7-7. Decimation Filter Response vs Frequency



Input clock rate (f_{CLK}) = 1 GHz

Figure 7-8. Decimation Filter Pass-Band Ripple vs Frequency

7.4.1.3 Mode 0: Decimate-by-4 With IQ Outputs and f_S / 4 Mixer

In mode 0, the DDC block includes a fixed frequency ±f_S / 4 complex digital mixer preceding the second stage decimation filters. The IQ passband is approximately ±100 MHz centered at f_S / 8 or 3f_S / 8, as shown in Figure 7-9.

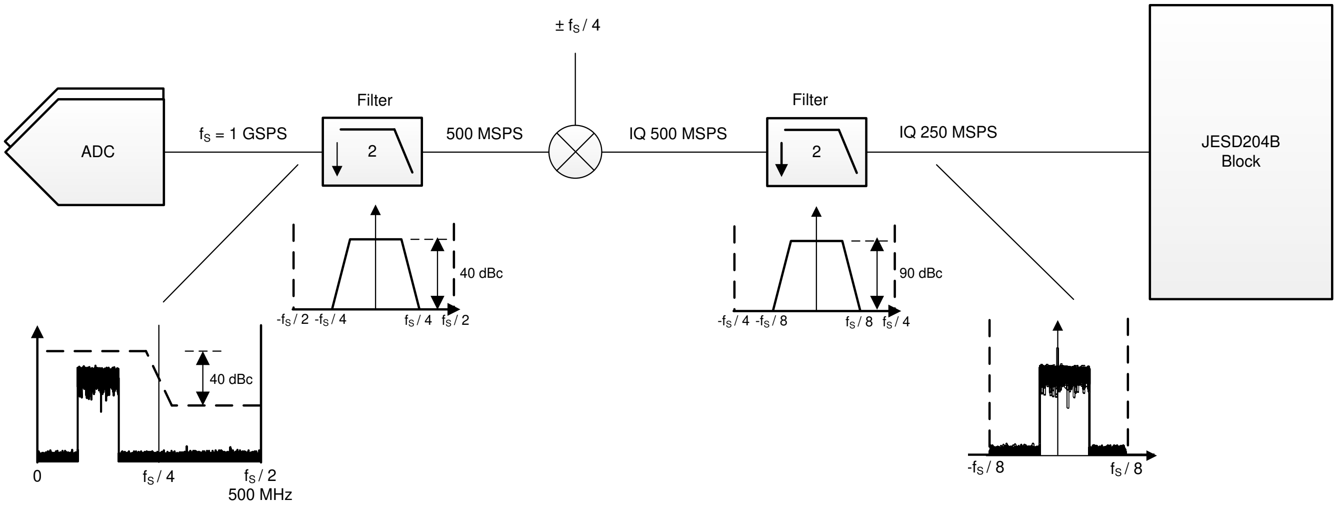


Figure 7-9. Operating Mode 0

7.4.1.4 Mode 1: Decimate-by-4 With IQ Outputs and 16-Bit NCO

In mode 1, the DDC block includes a 16-bit frequency resolution complex digital mixer preceding the second stage decimation filters, as shown in Figure 7-10.

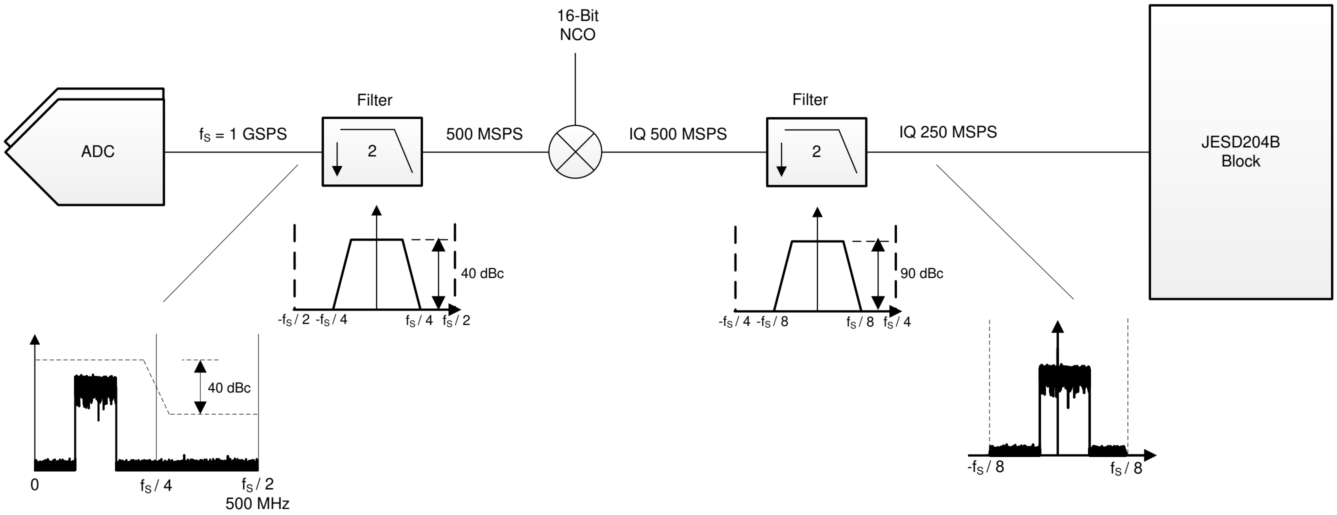


Figure 7-10. Operating Mode 1

7.4.1.5 Mode 2: Decimate-by-4 With Real Output

In mode 2, the DDC block cascades two decimate-by-2 filters. Each filter can be configured as low pass (LP) or high pass (HP) to allow down conversion of different frequency ranges, as shown in Table 7-2. The LP, HP and HP, LP output spectra are inverted as shown in Figure 7-11.

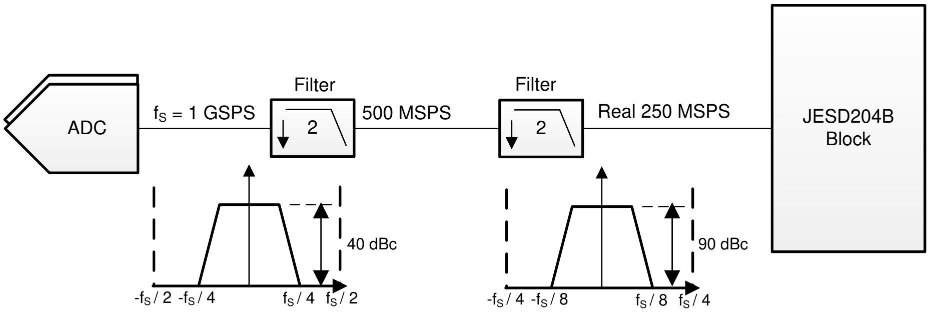


Figure 7-11. Operating in Mode 2

Table 7-2. ADS58J64 Operating Mode 2 Down-Converted Frequency Ranges

1ST STAGE FILTER	2ND STAGE FILTER	FREQUENCY RANGE WITH CLOCK RATE OF 983.04 MHz	BANDWIDTH WITH CLOCK RATE OF 983.04 MHz	FREQUENCY RANGE WITH CLOCK RATE OF 737.28 MHz	BANDWIDTH WITH CLOCK RATE OF 737.28 MHz
LP	LP	0 MHz–100 MHz	100 MHz	0 MHz–75 MHz	75 MHz
LP	HP	150 MHz–223 MHz	73 MHz	112.5 MHz–167.25 MHz	54.75 MHz
HP	LP	268.52 MHz–341.52 MHz	73 MHz	201.39 MHz–256.14 MHz	54.75 MHz
HP	HP	391.52 MHz–491.52 MHz	100 MHz	293.64 MHz–368.64 MHz	75 MHz

7.4.1.6 Mode 3: Decimate-by-2 Real Output With Frequency Shift

In mode 3, the DDC block includes a 16-bit complex NCO digital mixer followed by a f_S / 4 mixer with a real output to center the band at f_S / 4. The NCO must be set to a value different from ±f_S / 4, or else the samples are zeroed as shown in Figure 7-12.

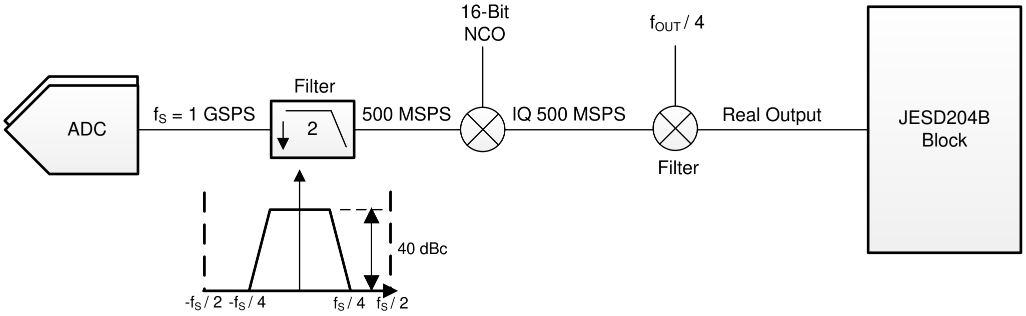


Figure 7-12. Operating Mode 3

7.4.1.7 Mode 4: Decimate-by-4 With Real Output

In mode 4, the DDC block includes a 16-bit complex NCO digital mixer preceding the second stage decimation filter. The signal is then mixed with f_{OUT} / 4 to generate a real output, as shown in Figure 7-13. The bandwidth available in this mode is 100 MHz.

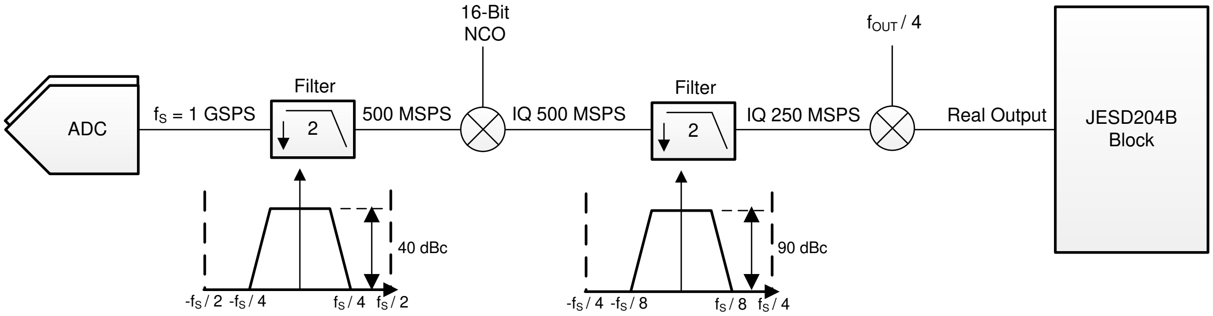


Figure 7-13. Operating Mode 4

7.4.1.8 Mode 6: Decimate-by-4 With IQ Outputs for up to 110 MHz of IQ Bandwidth

In mode 6, the DDC block includes a 16-bit complex NCO digital mixer preceding a second stage with a decimate-by-4 complex, generating a complex output at f_S / 8 as shown in Figure 7-14.

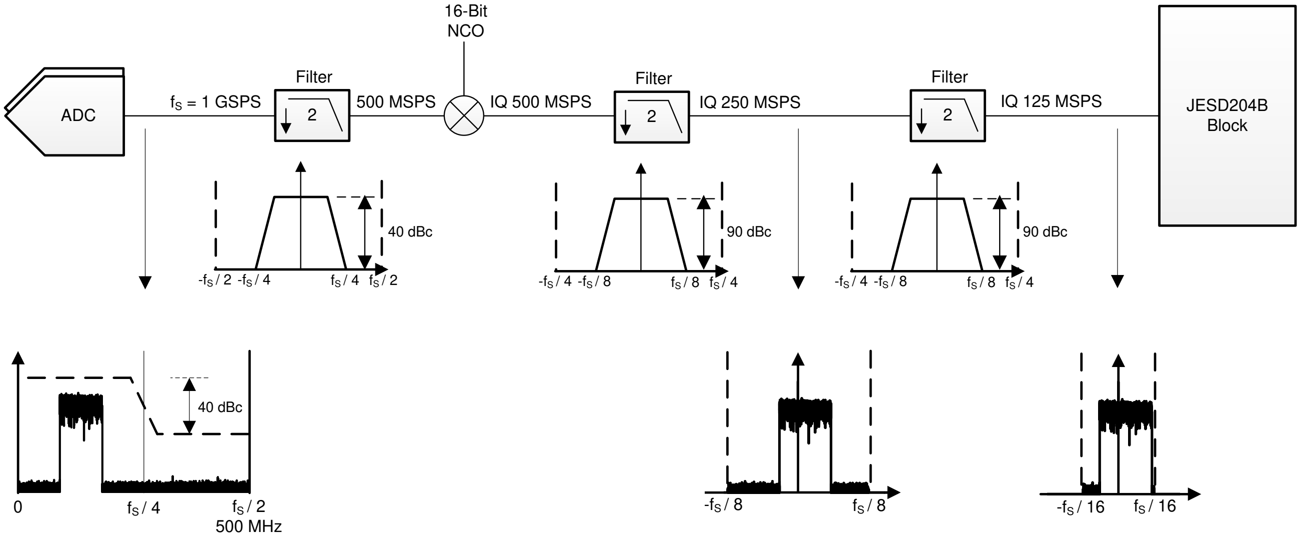


Figure 7-14. Operating Mode 6

7.4.1.9 Mode 7: Decimate-by-4 With Real Output and Zero Stuffing

In mode 7, the DDC block includes a 16-bit complex NCO digital mixer preceding the second stage decimation filter. The signal is then mixed with f_{OUT} / 4 to generate a real output that is then doubled in sample rate by zero stuffing every other sample, as shown in Figure 7-15. The bandwidth available in this mode is 100 MHz.

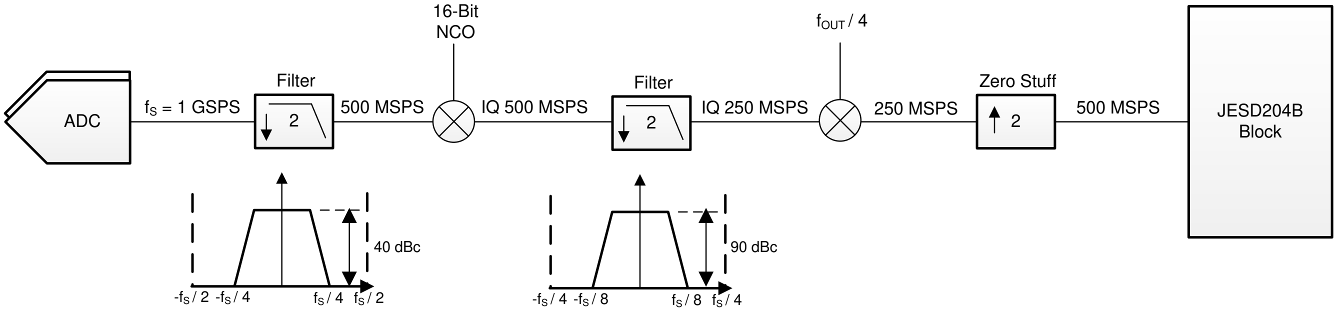


Figure 7-15. Operating Mode 7

7.4.1.10 Mode 8: Burst Mode

In burst mode, the decimate-by-2 data are output alternating between low resolution (L, 9-bit) and high resolution (H, 14-bit) output. The burst mode can be configured via SPI register writes independently for channels A, B and channels C, D. The high-resolution output is 14 bits and the number of high- and low-resolution samples is set with two user-programmable counters: one for high resolution (HC) and one for low resolution (LC). There is one counter pair (HC, LC) for channels A, B and one pair for channels C, D. The internal logic checks if the maximum duty cycle is exceeded and, if necessary, resets the counters to default values. Each output cycle starts with a low resolution and the counter values can be reconfigured for the next cycle prior to the start of the next cycle. The number of high-resolution samples is equal to two times the high-resolution count (HC). Similarly, the number of low-resolution samples is equal to two times the low-resolution count (LC).

An example of burst mode with mode 8 is shown in Figure 7-16.

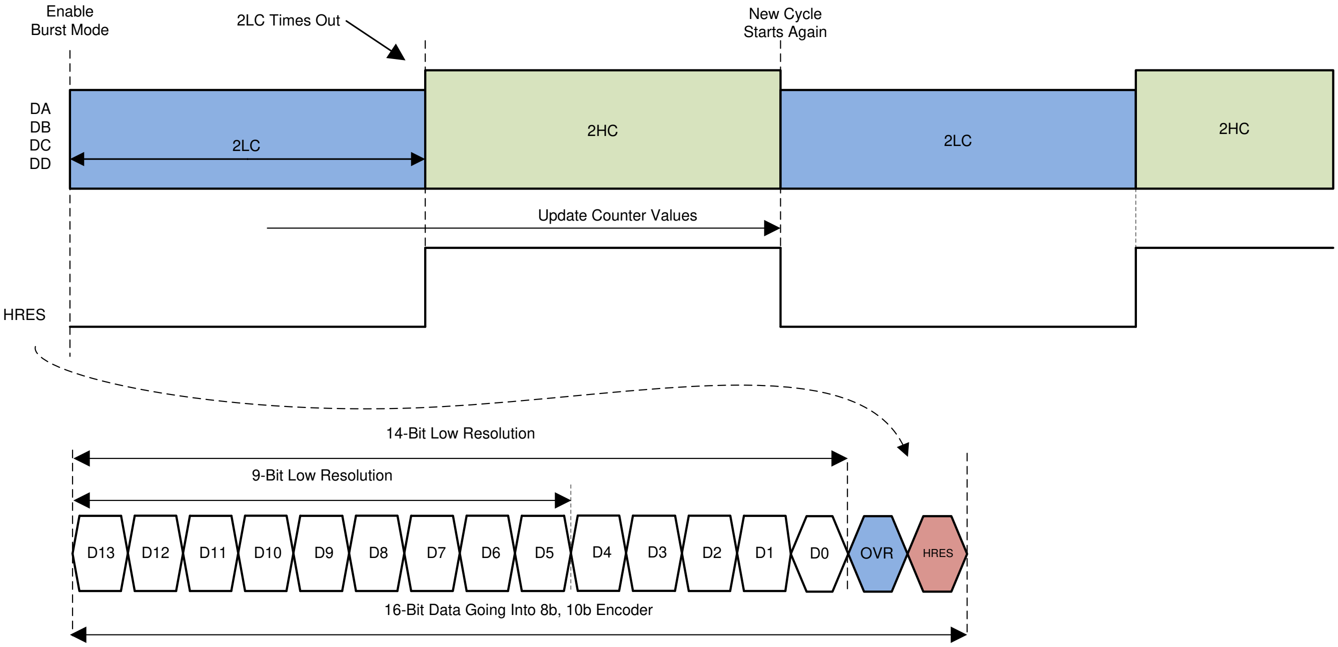


Figure 7-16. Burst Mode

The counter values for high and low resolution can be programmed to:

High-resolution counter (HC): 1 to 2^{25}

Low-resolution counter (LC): 1 to 2^{28}

The output duty cycle limit is shown in Table 7-3.

Table 7-3. Output Duty Cycle Limit

HIGH-RESOLUTION OUTPUT	LOW-RESOLUTION OUTPUT	MAXIMUM-ALLOWED DUTY CYCLE (High:Low Resolution Output)	DEFAULT VALUE (HC)	DEFAULT VALUE (LC)
14 bits	9 bits	1:3	1	3

7.4.1.11 Trigger Input

Burst mode can be operated in auto trigger or manual trigger mode. In manual trigger mode, the TRIGGER input (TRIGAB, TRIGCD) is used to release the high-resolution data (HC) burst after the low-resolution data counter (LC) times out. In auto trigger mode, the high-resolution data are released immediately after completion of the last low-resolution sample.

Using SPI control the ADS58J64 can be configured to use TRIGAB or TRIGCD as the manual trigger input.

7.4.1.12 Manual Trigger Mode

Burst mode can be operated in auto trigger or manual trigger mode. In manual trigger mode, the TRIGGER input (TRIGAB, TRIGCD) is used to release the high-resolution data (HC) burst after the low-resolution data counter (LC) times out. In auto trigger mode, the high-resolution data are released immediately after completion of the last low-resolution sample. Using SPI control, the ADS58J64 can be configured to use TRIGAB or TRIGCD as the manual trigger input.

An example of burst mode with a manual trigger is shown in Figure 7-17.

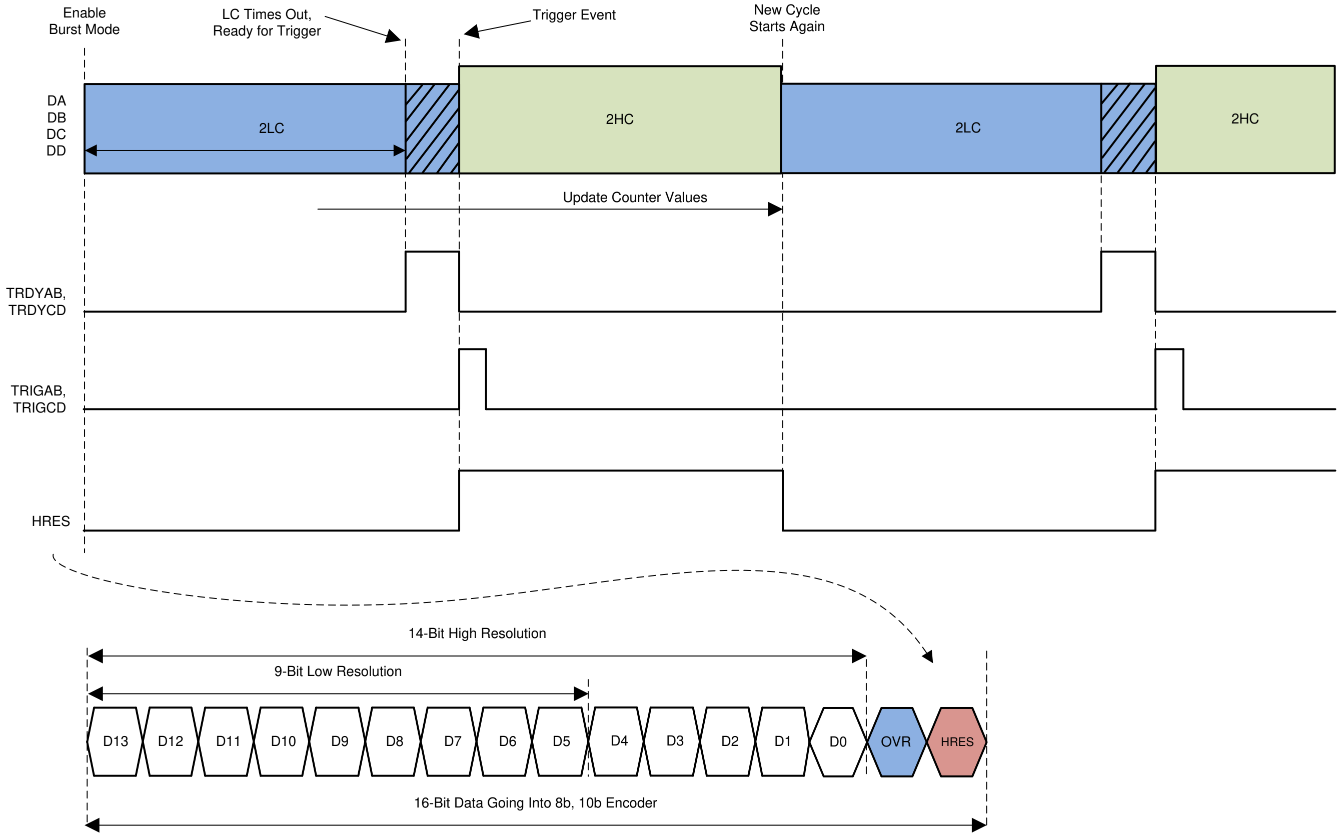


Figure 7-17. Timing Diagram for Manual Trigger Mode

7.4.1.13 Auto Trigger Mode

When auto trigger mode is enabled, the ADS58J64 starts transmission of low-resolution data. As soon as the low-resolution samples counter (LC) is finished, the ADS58J64 immediately begins transmitting the high-resolution output (H). The HRES flag can also be embedded in the JESD204B output data stream. The counter values can be updated until a new burst mode cycle starts with transmission of low-resolution samples. Any input on the trigger input pins is ignored.

An example of burst mode with an automatic trigger is shown in Figure 7-18.

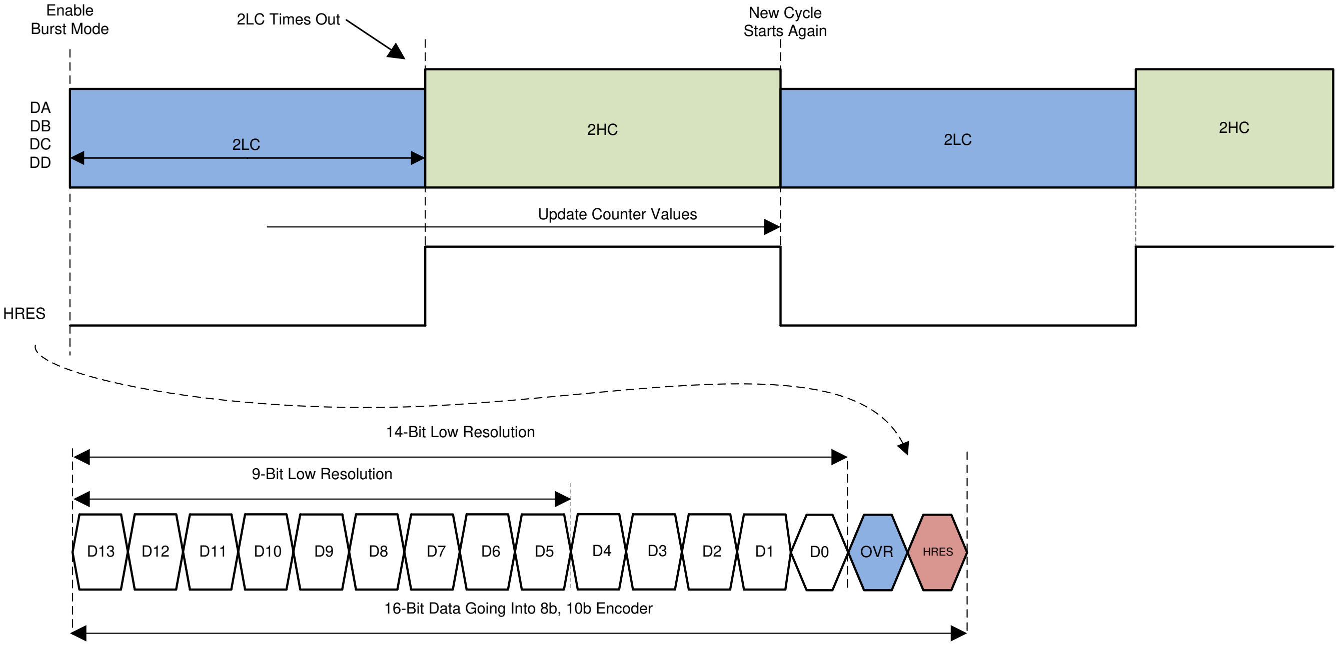


Figure 7-18. Timing Diagram for Auto Trigger Mode

7.4.1.14 Overrange Indication

The ADS58J64 provides a fast overrange indication that can be presented in the digital output data stream via SPI configuration. When the FOVR indication is embedded in the output data stream, this indication replaces the LSB (D0) of the 16 bits going to the 8b, 10b encode, as shown in Figure 7-19.

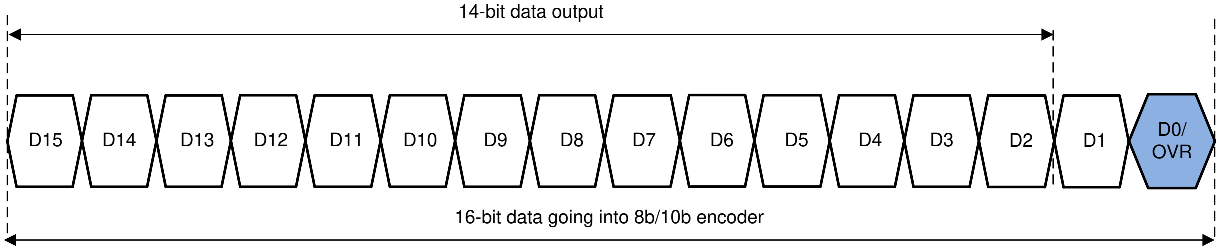


Figure 7-19. Timing Diagram for FOVR

The fast overrange feature of the ADS58J64 is configured using an upper (FOVRHi) and a lower (FOVRLo) 8-bit threshold that are compared against the partial ADC output of the initial pipeline stages. Figure 7-20 shows the FOVR high and FOVR low thresholds.

The two thresholds are configured via the SPI register where a setting of 136 maps to the maximum ADC code for a high FOVR, and a setting of 8 maps to the minimum ADC code for a low FOVR.

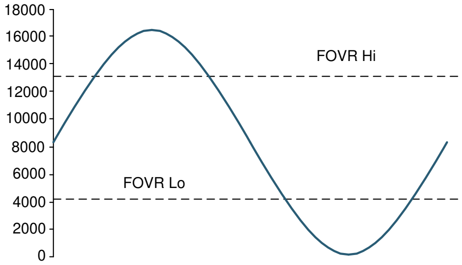


Figure 7-20. FOVR High and FOVR Low Thresholds

The FOVR threshold from a full-scale input based on the ADC code can be calculated by Equation 2:

$$\text{FOVR (dBFS)} = 20\log\left|\frac{\text{FOVR High or FOVR Low} - 72}{64}\right| \tag{2}$$

Therefore, a threshold of –0.5 dBFS from full-scale can be set with:

- FOVR high = 132 (27h, 84h)
- FOVR low = 12 (28h, 0Ch)

7.5 Programming

7.5.1 JESD204B Interface

The ADS58J64 supports device subclass 1 with a maximum output data rate of 10 Gbps for each serial transmitter.

An external SYSREF signal is used to align all internal clock phases and the local multi-frame clock to a specific sampling clock edge, as shown in Figure 7-21. A common SYSREF signal allows synchronization of multiple devices in a system and minimizes timing and alignment uncertainty. The ADS58J64 supports single (for all four JESD links) or dual (for channel A, B and C, D) SYNCb inputs and can be configured via SPI.

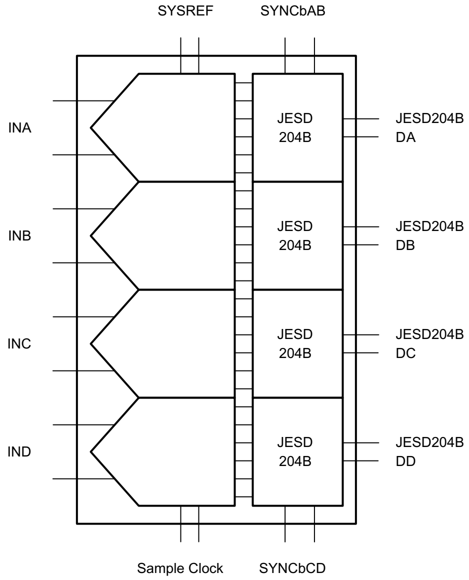


Figure 7-21. JESD204B Transmitter Block

Depending on the ADC sampling rate, the JESD204B output interface can be operated with one lane per channel. The JESD204B setup and configuration of the frame assembly parameters is handled via the SPI interface.

The JESD204B transmitter block consists of the transport layer, the data scrambler, and the link layer, as shown in Figure 7-22. The transport layer maps the ADC output data into the selected JESD204B frame data format and manages if the ADC output data or test patterns are being transmitted. The link layer performs the 8b, 10b data encoding as well as the synchronization and initial lane alignment using the SYNC input signal. Optionally, data from the transport layer can be scrambled.

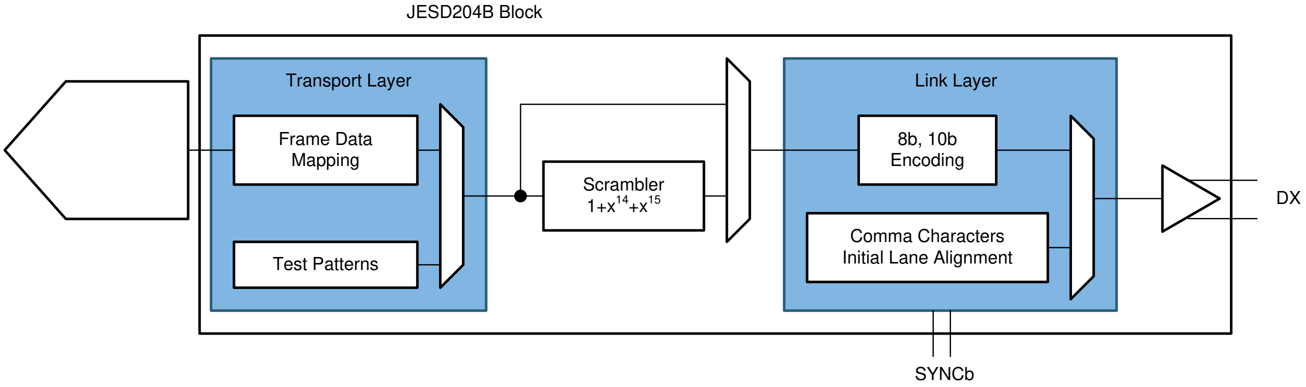


Figure 7-22. JESD Interface Block Diagram

7.5.2 JESD204B Initial Lane Alignment (ILA)

The initial lane alignment process is started by the receiving device by deasserting the SYNCb signal. When a logic low is detected on the SYNC input pins, the ADS58J64 starts transmitting comma (K28.5) characters to establish code group synchronization, as shown in Figure 7-23.

When synchronization is complete, the receiving device reasserts the SYNCb signal and the ADS58J64 starts the initial lane alignment sequence with the next local multi-frame clock boundary. The ADS58J64 transmits four multi-frames, each containing K frames (K is SPI programmable). Each of the multi-frames contains the frame start and end symbols and the second multi-frame also contains the JESD204 link configuration data.

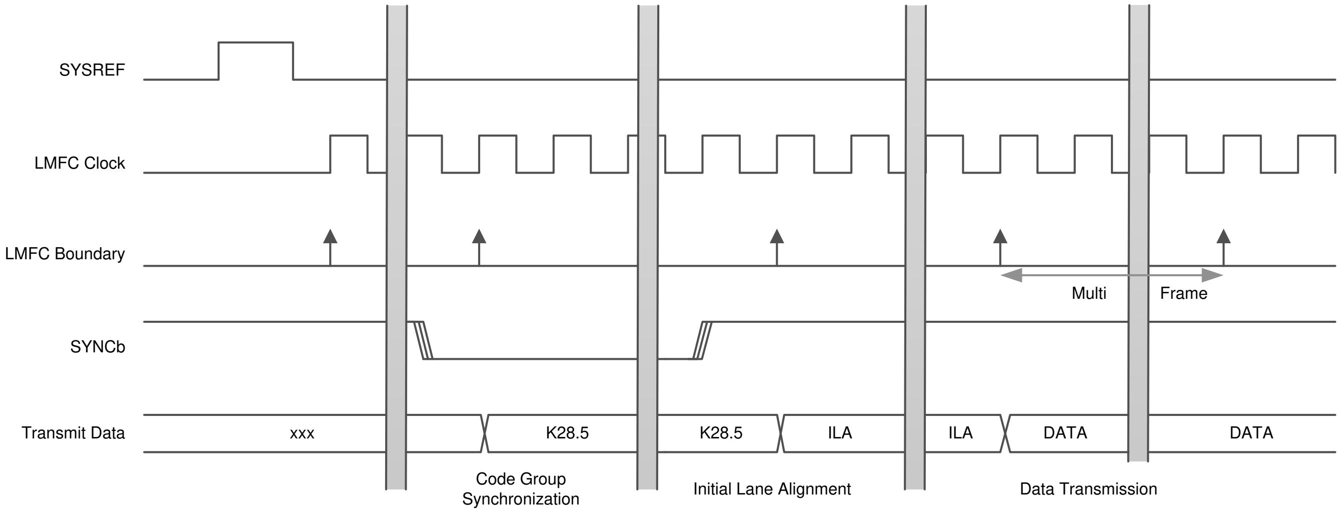


Figure 7-23. ILA Sequence

7.5.3 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L is the number of lanes per link
- M is the number of converters per device
- F is the number of octets per frame clock period
- S is the number of samples per frame

Table 7-4 lists the available JESD204B formats and valid ranges for the ADS58J64. The ranges are limited by the SerDes line rate and the maximum ADC sample frequency.

Table 7-4. Available JESD204B Formats and Valid Ranges for the ADS58J64

L	M	F	S	OPERATING MODE	DIGITAL MODE	OUTPUT FORMAT	JESD MODE	JESD PLL MODE	MAX ADC OUTPUT RATE (MSPS)	MAX f_{SerDes} (Gbps)	JESD PLL REGISTER CONFIGURATION
4	8	4	1	0, 1	2x decimation	Complex	40x	40x	250	10.0	—
4	4	2	1	2, 4	2x decimation	Real	20x	20x	250	5.0	CTRL_SER_MODE = 1, SerDes_MODE = 1
2	4	4	1	2, 4	2x decimation	Real	40x	40x	250	10.0	—
4	8	4	1	6	4x decimation	Complex	40x	20x	125	5.0	—
2	8	8	1	6	4x decimation	Complex	80x	40x	125	10.0	CTRL_SER_MODE = 1, SerDes_MODE = 3
4	4	2	1	7	2x decimation with 0-pad	Real	20x	40x	500	10.0	—
4	4	2	1	3, 8	Burst mode	Real	20x	40x	500	10.0	—

The detailed frame assembly for various LMFS settings are shown in Table 7-5 and Table 7-6.

Table 7-5. Detailed Frame Assembly for Four-Lane Modes (Mode 0, 1, 3, 6, 7, and 8)

OUTPUT LANE	LMFS = 4841				LMFS = 4421				LMFS = 4421 (0-Pad)			
DA	AI_0[15:8]	AI_0[7:0]	AQ_0[15:8]	AQ0[7:0]	A_0[15:8]	A_0[7:0]	A_1[15:8]	A_1[7:0]	A_0[15:8]	A_0[7:0]	0000 0000	0000 0000
DB	BI_0[15:8]	BI_0[7:0]	BQ_0[15:8]	BQ_0[7:0]	B_0[15:8]	B_0[7:0]	B_1[15:8]	B_1[7:0]	B_0[15:8]	B_0[7:0]	0000 0000	0000 0000
DC	CI_0[15:8]	CI_0[7:0]	CQ_0[15:8]	CQ_0[7:0]	C_0[15:8]	C_0[7:0]	C_1[15:8]	C_1[7:0]	C_0[15:8]	C_0[7:0]	0000 0000	0000 0000
DD	DI_0[15:8]	DI_0[7:0]	DQ_0[15:8]	DQ_0[7:0]	D_0[15:8]	D_0[7:0]	D_1[15:8]	D_1[7:0]	D_0[15:8]	D_0[7:0]	0000 0000	0000 0000

Table 7-6. Detailed Frame Assembly for Two-Lane Modes (Mode 2 and 4)

OUTPUT LANE	LMFS = 2441				LMFS = 2881							
DB	A_0[15:8]	A_0[7:0]	B_0[15:8]	B_0[7:0]	AI_0[15:8]	AI_0[7:0]	AQ_0[15:8]	$AQ_{0[}$7:0]	BI_0[15:8]	BI_0[7:0]	BQ_0[15:8]	BQ_0[7:0]
DC	C_0[15:8]	C_0[7:0]	D_0[15:8]	D_0[7:0]	CI_0[15:8]	CI_0[7:0]	CQ_0[15:8]	CQ_0[7:0]	DI_0[15:8]	DI_0[7:0]	DQ_0[15:8]	DQ_0[7:0]

7.5.4 JESD Output Switch

The ADS58J64 provides a digital cross-point switch in the JESD204B block that allows internal routing of any output of the two ADCs within one channel pair to any of the two JESD204B serial transmitters in order to ease layout constraints, as shown in Figure 7-24. The cross-point switch routing is configured via SPI (address 41h in the SERDES_XX digital page).

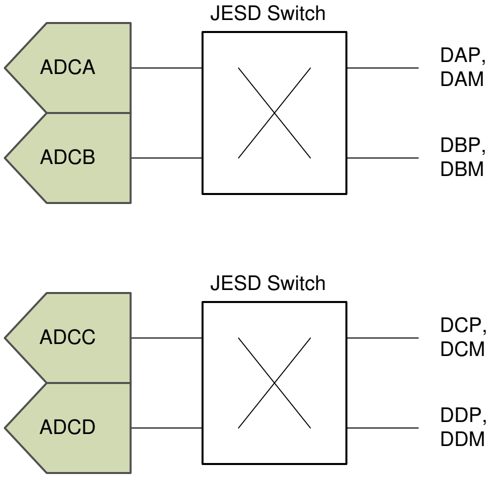


Figure 7-24. Switching the Output Lanes

7.5.4.1 SerDes Transmitter Interface

Each of the 10-Gbps SerDes transmitter outputs require ac-coupling between the transmitter and receiver, as shown in Figure 7-25. Terminate the differential pair with 100 Ω as close to the receiving device as possible to avoid unwanted reflections and signal degradation.

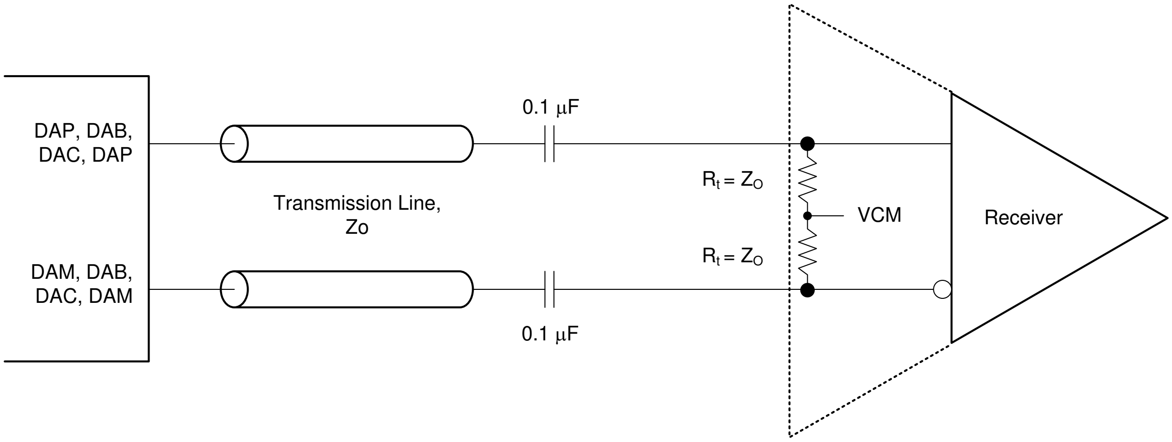


Figure 7-25. SerDes Transmitter Connection to Receiver

7.5.4.2 SYNCb Interface

The ADS58J64 supports single (where either the SYNCb input controls all four JESD204B links) or dual (where one SYNCb input controls two JESD204B lanes: DA, DB and DC, DD) SYNCb control. When using the single SYNCb control, connect the unused input to a differential logic low (SYNCbxxP = 0 V, SYNCbxxM = DVDD).

7.5.4.3 Eye Diagram

Figure 7-26 to Figure 7-29 show the serial output eye diagrams of the ADS58J64 at 7.5 Gbps and 10 Gbps with default and increased output voltage swing against the JESD204B mask.

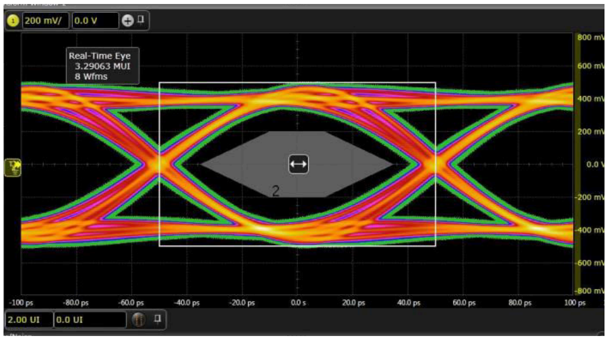


Figure 7-26. Eye at 10-Gbps Bit Rate with Default Output Swing

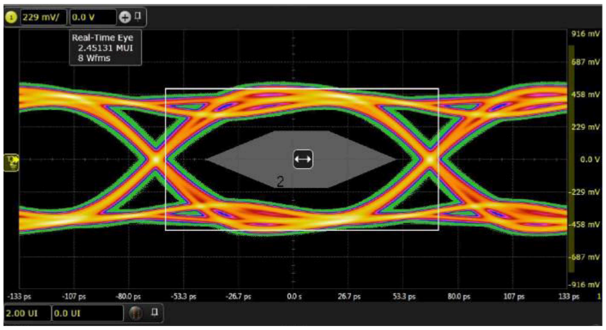


Figure 7-27. Eye at 7.5-Gbps Bit Rate with Default Output Swing

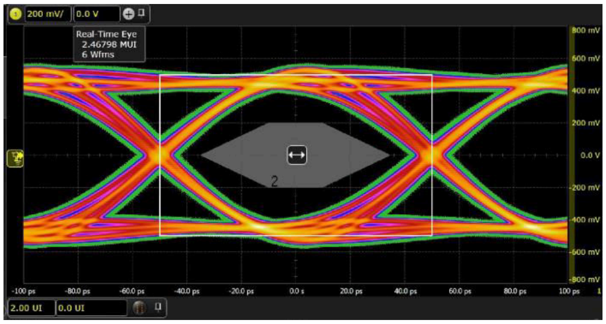


Figure 7-28. Eye at 10-Gbps Bit Rate with Increased Output Swing

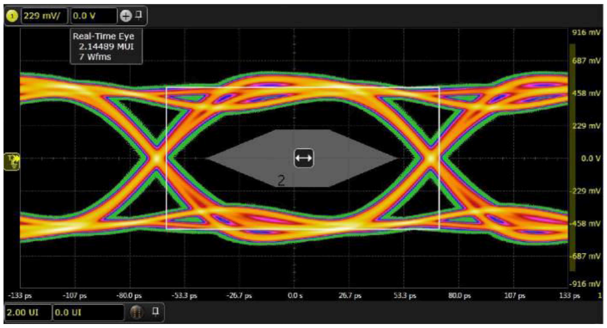


Figure 7-29. Eye at 7.5-Gbps Bit Rate with Increased Output Swing

7.5.5 Device Configuration

The ADS58J64 can be configured using a serial programming interface, as described in the *Section 7.6* section. In addition, the device has one dedicated parallel pin (PDN) for controlling the power-down modes. The ADS58J64 supports a 24-bit (16-bit address, 8-bit data) SPI operation and uses paging to access all register bits.

7.5.5.1 Details of the Serial Interface

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDIN (serial data input data), and SDOUT (serial data output) pins. Serially shifting bits into the device is enabled when SEN is low. SDIN serial data are latched at every SCLK rising edge when SEN is active (low). Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The first 16 bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 10 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

7.5.5.1.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one hardware reset by applying a high pulse on the RESET pin.

7.5.5.2 Serial Register Write

The internal registers of the ADS58J64 can be programmed (as shown in Figure 7-30) by:

1. Driving the SEN pin low
2. Setting the R/W bit = 0
3. Initiating a serial interface cycle specifying the address of the register (A[14:0]) whose content must be written
4. Writing the 8-bit data that is latched in on the SCLK rising edge

The ADS58J64 has several different register pages (page selection in address 11h, 12h). Specify the register page before writing to the desired address. The register page only must be set one time for continuous writes to the same page.

During the write operation, the SDOUT pin is in a high-impedance mode and must float.

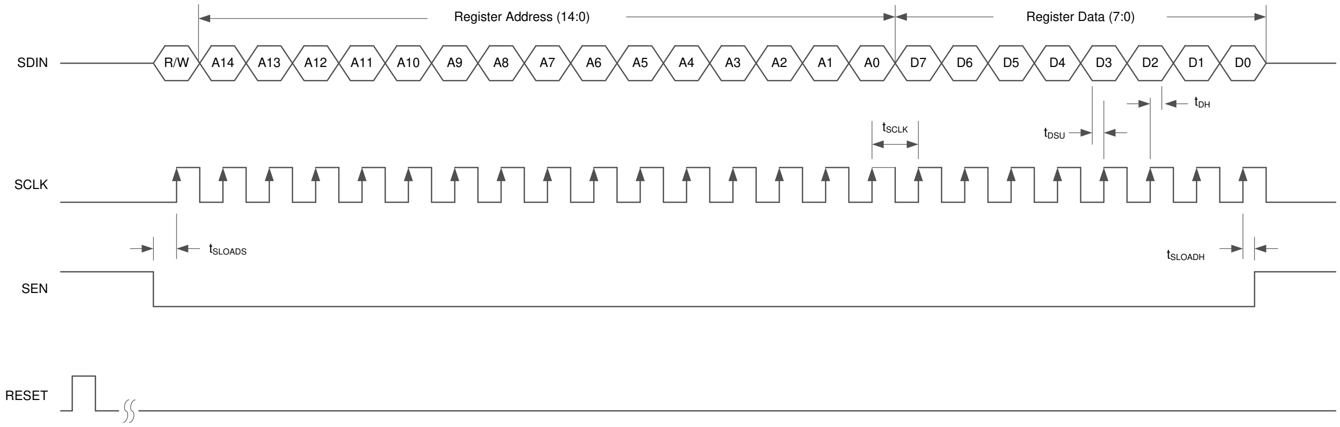


Figure 7-30. Serial Interface Write Timing Diagram

7.5.5.3 Serial Read

A typical 4-wire serial register readout is shown in Figure 7-31. In the default 4-pin configuration, the SDIN pin is the data output from the ADS58J64 during the data transfer cycle when SDOUT is in a high-impedance state. The internal registers of the ADS58J64 can be read out by:

1. Driving the SEN pin low
2. Setting the R/W bit to 1 to enable read back
3. Specifying the address of the register (A[14:0]) whose content must be read back
4. The device outputs the contents (D[7:0]) of the selected register on the SDOUT pin (pin 51)
5. The external controller can latch the contents at the SCLK rising edge

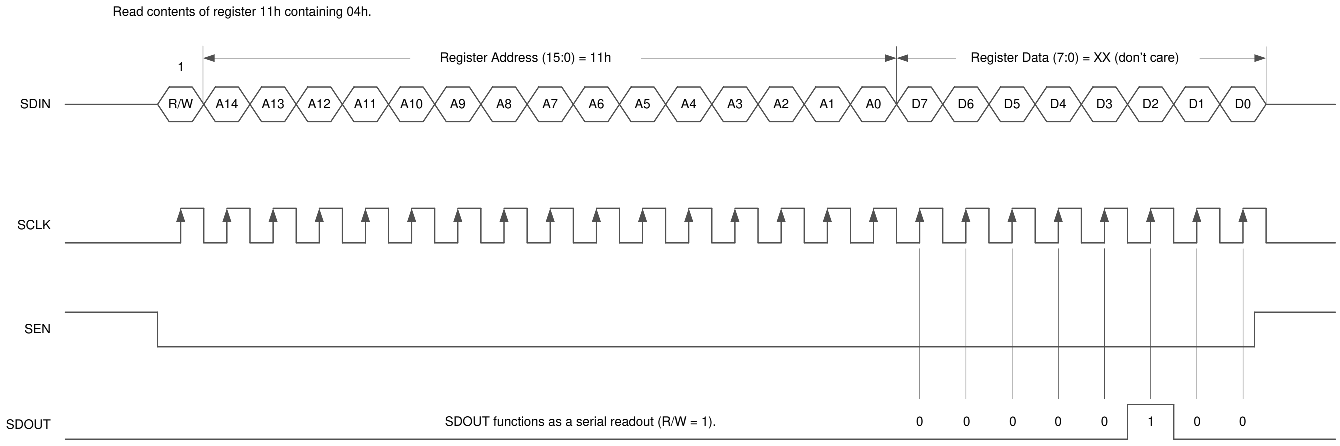


Figure 7-31. Serial Interface 4-Wire Read Timing Diagram

7.6 Register Maps

7.6.1 Register Map

The ADS58J64 registers are organized on different pages depending on their internal functions. The pages are accessed by selecting the page in the master pages 11h–13h. The page selection must only be written one time for a continuous update of registers for that page.

There are six different SPI banks (shown in Figure 7-32) that group together different functions:

- GLOBAL: contains controls for accessing other SPI banks
- DIGTOP: top-level digital functions
- ANALOG: registers controlling power-down and analog functions
- SERDES_XX: registers controlling JESD204B functions
- CHX: registers controlling channel-specific functions, including DDC
- ADCXX: register page for one of the eight interleaved ADCs

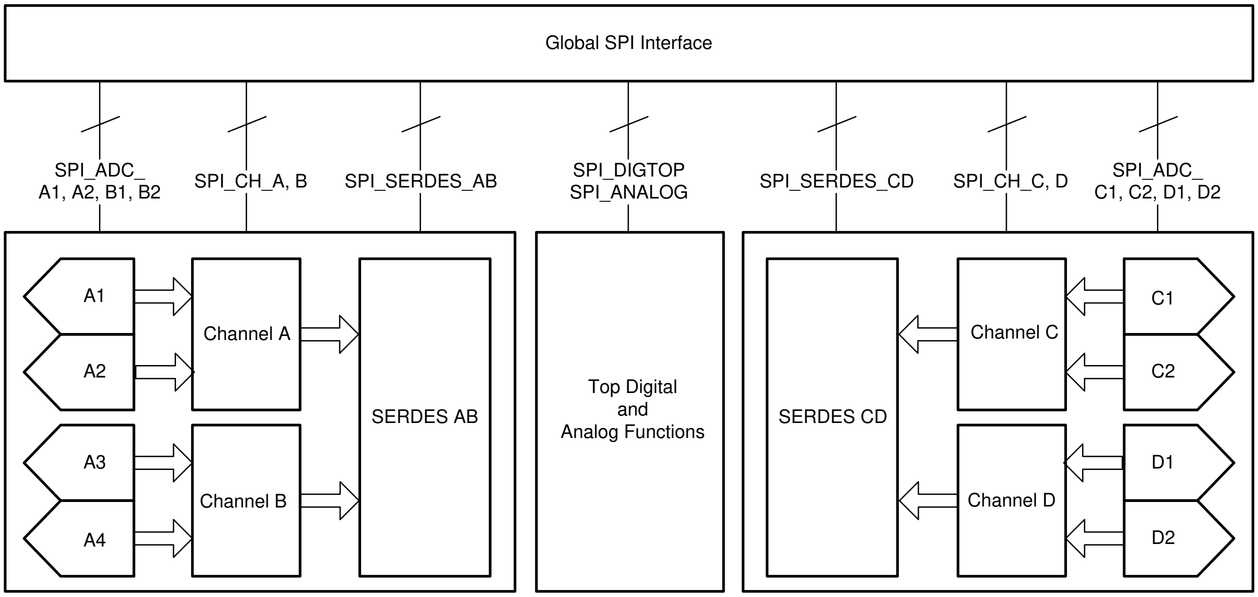


Figure 7-32. SPI Register Block Diagram

Table 7-7. Serial Interface Register Map

ADDRESS (Hex)	7	6	5	4	3	2	1	0
GLOBAL PAGE								
00h	WRITE_1	0	0	0	0	0	0	SW_RESET
04h	VERSION_ID							
11h	SPI_D2	SPI_D1	SPI_C2	SPI_C1	SPI_B2	SPI_B1	SPI_A2	SPI_A1
12h	0	SPI_SerDes_CD	SPI_SerDes_AB	SPI_CHD	SPI_CHC	SPI_CHB	SPI_CHA	SPI_DIGTOP
13h	0	0	0	0	0	0	0	SPI_ANALOG
DIGTOP PAGE								
64h	0	0	0	0	0	0	FS_375_500	0
8Dh	CUSTOMPATTERN1[7:0]							
8Eh	CUSTOMPATTERN1[15:8]							
8Fh	CUSTOMPATTERN2[7:0]							
90h	CUSTOMPATTERN2[15:8]							
91h	TESTPATTERNSELECT				TESTPATTERNEN CHD	TESTPATTERNEN CHC	TESTPATTERNEN CHB	TESTPATTERNEN CHA
ABh	0	0	0	0	0	0	0	SPECIALMODE0
ACh	0	0	0	0	0	0	0	SPECIALMODE1
ADh	0	0	0	0	DDCMODEAB			
AEh	0	0	0	0	DDCMODECD			
B7h	0	0	0	0	0	0	0	LOADTRIMS

Table 7-7. Serial Interface Register Map (continued)

ADDRESS (Hex)	7	6	5	4	3	2	1	0
ANALOG PAGE								
6Ah	0	0	0	0	0	0	DIS_SYSREF	0
6Fh	0	JESD_SWING			0	0	0	0
71h	EMP_LANE_B[5:4]		EMP_LANE_A					
72h	0	0	0	0	EMP_LANE_B[3:0]			
93h	EMP_LANE_D[5:4]		EMP_LANE_C					
94h	0	0	0	0	EMP_LANE_D[3:0]			
9Bh	0	0	0	SYSREF_PDN	0	0	0	0
9Dh	PDN_CHA	PDN_CHB	0	0	PDN_CHD	PDN_CHC	0	0
9Eh	0	0	0	PDN_SYNCAB	0	0	0	PDN_GLOBAL
9Fh	0	0	0	0	0	0	PIN_PDN_MODE	FAST_PDN
AFh	0	0	0	0	0	0	PDN_SYNCCD	0
SERDES_XX PAGE								
20h	CTRL_K	CTRL_SER_MODE	0	TRANS_TEST_EN	0	LANE_ALIGN	FRAME_ALIGN	TX_ILA_DIS
21h	SYNC_REQ	OPT_SYNC_REQ	SYNCB_SEL_AB_CD	0	0	0	SerDes_MODE	
22h	LINK_LAYER_TESTMODE_SEL			RPAT_SET_DISP	LMFC_MASK_RESET	0	0	0
23h	FORCE_LMFC_COUNT	LMFC_CNT_INIT					RELEASE_ILANE_REQ	
25h	SCR_EN	0	0	0	0	0	0	0
26h	0	0	0	K_NO_OF_FRAMES_PER_MULTIFRAME				
28h	0	0	0	0	CTRL_LID	0	0	0
2Dh	LID1				LID2			
36h	PRBS_MODE		0	0	0	0	0	0
SERDES_XX PAGE (continued)								
37h	LSB1_HR_FLAG_EN	LSB0_HR_FLAG_EN	LOAD_RES	TRIG_SEL_AB_CD	AUTO_TRIG_EN	0	RATIO_INVALID	0
39h	0	0	0	0	LOWRESCOUNT[27:24]			
3Ah	LOWRESCOUNT[23:16]							
3Bh	LOWRESCOUNT[15:8]							
3Ch	LOWRESCOUNT[7:0]							
3Dh	0	0	0	0	HIGHRESCOUNT[27:24]			
3Eh	HIGHRESCOUNT[23:16]							
3Fh	HIGHRESCOUNT[15:8]							
40h	HIGHRESCOUNT[7:0]							
41h	LANE_BONA				LANE_AONB			
42h	0	0	0	0	INVERT_AC		INVERT_BD	
CHX PAGE								
26h	0	0	0	0	0	0	GAINWORD	
27h	OVR_ENABLE	OVR_FAST_SEL	0	0	OVR_LSB1	0	OVR_LSB0	0
2Dh	0	0	0	0	0	0	NYQUIST_SELECT	0
78h	0	0	0	0	0	FS4_SIGN	NYQ_SEL_MODE02	NYQ_SEL
7Ah	NCO_WORD[15:8]							
7Bh	NCO_WORD[7:0]							
7Eh	0	0	0	0	0	MODE467_GAIN	MODE0_GAIN	MODE13_GAIN
ADCXX PAGE								
07h	FAST_OVR_THRESHOLD_HIGH							
08h	FAST_OVR_THRESHOLD_LOW							
D5h	0	0	0	0	CAL_EN	0	0	0

7.6.1.1 Register Description

7.6.1.1.1 GLOBAL Page Register Description

7.6.1.1.1.1 Register 00h (address = 00h) [reset = 0h], GLOBAL Page

Figure 7-29. Register 0h

7	6	5	4	3	2	1	0
WRITE_1	0	0	0	0	0	0	SW_RESET
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-8. Register 00h Field Descriptions

Bit	Field	Type	Reset	Description
7	WRITE_1	R/W	0h	Always write 1
6-1	0	R/W	0h	Must read or write 0
0	SW_RESET	R/W	0h	This bit rests the device.

7.6.1.1.1.2 Register 04h (address = 04h) [reset = 0h], GLOBAL Page

Figure 7-30. Register 4h

7	6	5	4	3	2	1	0
VERSION_ID							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 7-9. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VERSION_ID	R	0h	16 : PG 1.0 32 : PG 2.0 48 : PG3.0

7.6.1.1.1.3 Register 11h (address = 11h) [reset = 0h], GLOBAL Page

Figure 7-31. Register 11h

7	6	5	4	3	2	1	0
SPI_D2	SPI_D1	SPI_C2	SPI_C1	SPI_B2	SPI_B1	SPI_A2	SPI_A1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-10. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
7	SPI_D2	R/W	0h	This bit selects the ADC D2 SPI. 0 : ADC D2 SPI is disabled 1 : ADC D2 SPI is enabled
6	SPI_D1	R/W	0h	This bit selects the ADC D1 SPI. 0 : ADC D1 SPI is disabled 1 : ADC D1 SPI is enabled
5	SPI_C2	R/W	0h	This bit selects the ADC C2 SPI 0 : ADC C2 SPI is disabled 1 : ADC C2 SPI is enabled
4	SPI_C1	R/W	0h	This bit selects the ADC C1 SPI. 0 : ADC C1 SPI is disabled 1 : ADC C1 SPI is enabled
3	SPI_B2	R/W	0h	This bit selects the ADC B2 SPI. 0 : ADC B2 SPI is disabled 1 : ADC B2 SPI is enabled
2	SPI_B1	R/W	0h	This bit selects the ADC B1 SPI. 0 : ADC B1 SPI is disabled 1 : ADC B1 SPI is enabled
1	SPI_A2	R/W	0h	This bit selects the ADC A2 SPI. 0 : ADC A2 SPI is disabled 1 : ADC A2 SPI is enabled
0	SPI_A1	R/W	0h	This bit selects the ADC A1 SPI. 0 : ADC A1 SPI is disabled 1 : ADC A1 SPI is enabled

7.6.1.1.1.4 Register 12h (address = 12h) [reset = 0h], GLOBAL Page

Figure 7-32. Register 12h

7	6	5	4	3	2	1	0
0	SPI_SerDes_CD	SPI_SerDes_AB	SPI_CHD	SPI_CHC	SPI_CHB	SPI_CHA	SPI_DIGTOP
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-11. Register 12h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must read or write 0
6	SPI_SerDes_CD	R/W	0h	This bit selects the channel CD SerDes SPI. 0 : Channel CD SerDes SPI is disabled 1 : Channel CD SerDes SPI is enabled
5	SPI_SerDes_AB	R/W	0h	This bit selects the channel AB SerDes SPI. 0 : Channel AB SerDes is disabled 1 : Channel AB SerDes is enabled
4	SPI_CHD	R/W	0h	This bit selects the channel D SPI. 0 : Channel D SPI is disabled 1 : Channel D SPI is enabled
3	SPI_CHC	R/W	0h	This bit selects the channel C SPI. 0 : Channel C SPI is disabled 1 : Channel C SPI is enabled
2	SPI_CHB	R/W	0h	This bit selects the channel B SPI. 0 : Channel B SPI is disabled 1 : Channel B SPI is enabled
1	SPI_CHA	R/W	0h	This bit selects the channel A SPI. 0 : Channel A SPI is disabled 1 : Channel A SPI is enabled
0	SPI_DIGTOP	R/W	0h	This bit selects the DIGTOP SPI. 0 : DIGTOP SPI is disabled 1 : DIGTOP SPI is enabled

7.6.1.1.1.5 Register 13h (address = 13h) [reset = 0h], GLOBAL Page

Figure 7-33. Register 13h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SPI_ANALOG
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-12. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must read or write 0
0	SPI_ANALOG	R/W	0h	This bit selects the analog SPI. 0 : Analog SPI is disabled 1 : Analog SPI is disabled

7.6.1.1.2 DIGTOP Page Register Description

7.6.1.1.2.1 Register 64h (address = 64h) [reset = 0h], DIGTOP Page

Figure 7-34. Register 64h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FS_375_500	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-13. Register 64h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must read or write 0
1	FS_375_500	R/W	0h	This bit selects the clock rate for loading trims.. 0 : 375 MSPS 1 : 500 MSPS
0	0	R/W	0h	Must read or write 0

7.6.1.1.2.2 Register 8Dh (address = 8Dh) [reset = 0h], DIGTOP Page

Figure 7-35. Register 8Dh

7	6	5	4	3	2	1	0
CUSTOMPATTERN1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-14. Register 8Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOMPATTERN1[7:0]	R/W	0h	These bits set the custom pattern 1 that is used when the test pattern is enabled and set to a single or dual test pattern.

7.6.1.1.2.3 Register 8Eh (address = 8Eh) [reset = 0h], DIGTOP Page

Figure 7-36. Register 8Eh

7	6	5	4	3	2	1	0
CUSTOMPATTERN1[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-15. Register 8Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOMPATTERN1[15:8]	R/W	0h	These bits set the custom pattern 1 that is used when the test pattern is enabled and set to a single or dual test pattern.

7.6.1.1.2.4 Register 8Fh (address = 8Fh) [reset = 0h], DIGTOP Page

Figure 7-37. Register 8Fh

7	6	5	4	3	2	1	0
CUSTOMPATTERN2[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-16. Register 8Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOMPATTERN2[7:0]	R/W	0h	These bits set the custom pattern 2 that is used when the test pattern select is set to dual pattern mode.

7.6.1.1.2.5 Register 90h (address = 90h) [reset = 0h], DIGTOP Page

Figure 7-38. Register 90h

7	6	5	4	3	2	1	0
CUSTOMPATTERN2[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-17. Register 90h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOMPATTERN2[15:8]	R/W	0h	These bits set the custom pattern 2 that is used when the test pattern select is set to dual pattern mode.

7.6.1.1.2.6 Register 91h (address = 91h) [reset = 0h], DIGTOP Page

Figure 7-39. Register 91h

7	6	5	4	3	2	1	0
TESTPATTERNSELECT				TESTPATTERNENCHD	TESTPATTERNENCHC	TESTPATTERNENCHB	TESTPATTERNENCHA
R/W-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-18. Register 91h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	TESTPATTERNSELECT	R/W	0h	These bits select the test pattern on the output when the test pattern is enabled for a suitable channel. 0 : Default 1 : All zeros 2 : All ones 3 : Toggle pattern 4 : Ramp pattern 6 : Custom pattern 1 7 : Toggle between custom pattern 1 and custom pattern 2 8 : Deskew pattern (0xAAAA)
3	TESTPATTERNENCHD	R/W	0h	This bit enables the channel D test pattern. 0 : Default data on channel D 1 : Enable test pattern on channel D
2	TESTPATTERNENCHC	R/W	0h	This bit enables the channel C test pattern. 0 : Default data on channel C 1 : Enable test pattern on channel C
1	TESTPATTERNENCHB	R/W	0h	This bit enables the channel B test pattern. 0 : Default data on channel B 1 : Enable test pattern on channel B
0	TESTPATTERNENCHA	R/W	0h	This bit enables the channel A test pattern. 0 : Default data on channel A 1 : Enable test pattern on channel A

7.6.1.1.2.7 Register ABh (address = ABh) [reset = 0h], DIGTOP Page

Figure 7-40. Register ABh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SPECIALMODE0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-19. Register ABh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must read or write 0
0	SPECIALMODE0	R/W	0h	Always write 1

7.6.1.1.2.8 Register ACh (address = ACh) [reset = 0h], DIGTOP Page

Figure 7-41. Register ACh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SPECIALMODE1
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-20. Register ACh Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must read or write 0
0	SPECIALMODE1	R/W	0h	Always write 1

7.6.1.1.2.9 Register ADh (address = ADh) [reset = 0h], DIGTOP Page

Figure 7-42. Register ADh

7	6	5	4	3	2	1	0
0	0	0	0	DDCMODEAB			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-21. Register ADh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3-0	DDCMODEAB	R/W	0h	These bits select the DDC mode for channel AB. 0 : Mode 0 1 : Mode 1 2 : Mode 2 3 : Mode 3 4 : Mode 4 6 : Mode 6 7 : Mode 7 8 : Mode 8

7.6.1.1.2.10 Register AEh (address = AEh) [reset = 0h], DIGTOP Page

Figure 7-43. Register AEh

7	6	5	4	3	2	1	0
0	0	0	0	DDCMODECD			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-22. Register AEh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3-0	DDCMODECD	R/W	0h	These bits select the DDC mode for channel CD. 0 : Mode 0 1 : Mode 1 2 : Mode 2 3 : Mode 3 4 : Mode 4 6 : Mode 6 7 : Mode 7 8 : Mode 8

7.6.1.1.2.11 Register B7h (address = B7h) [reset = 0h], DIGTOP Page

Figure 7-44. Register B7h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LOADTRIMS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-23. Register B7h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0h	Must read or write 0
0	LOADTRIMS	R/W	0h	This bit load trims the device.

7.6.1.1.3 ANALOG Page Register Description

7.6.1.1.3.1 Register 6Ah (address = 6Ah) [reset = 0h], ANALOG Page

Figure 7-45. Register 6Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS_SYSREF	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-24. Register 6Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must read or write 0
1	DIS_SYSREF	R/W	0h	This bit masks the SYSREF input. 0 : SYSREF input is not masked 1 : SYSREF input is masked
0	0	R/W	0h	Must read or write 0

7.6.1.1.3.2 Register 6Fh (address = 6Fh) [reset = 0h], ANALOG Page

Figure 7-46. Register 6Fh

7	6	5	4	3	2	1	0
0	JESD_SWING			0	0	0	0
R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-25. Register 6Fh Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	Must read or write 0
6-4	JESD_SWING	R/W	0h	These bits control the JESD swing. 0 : 860 mV_{PP} 1 : 810 mV_{PP} 2 : 770 mV_{PP} 3 : 745 mV_{PP} 4 : 960 mV_{PP} 5 : 930 mV_{PP} 6 : 905 mV_{PP} 7 : 880 mV_{PP}
3-0	0	R/W	0h	Must read or write 0

7.6.1.1.3.3 Register 71h (address = 71h) [reset = 0h], ANALOG Page

Figure 7-47. Register 71h

7	6	5	4	3	2	1	0
EMP_LANE_B[5:4]		EMP_LANE_A					
R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-26. Register 71h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EMP_LANE_B[5:4]	R/W	0h	De-emphasis for lane B. These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in decibels (dB) is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 : 0 dB 1 : –1 dB 3 : –2 dB 7 : –4.1 dB 15 : –6.2 dB 31 : –8.2 dB 63 : –11.5 dB Others: Do not use
5-0	EMP_LANE_A	R/W	0h	De-emphasis for lane A. These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 : 0 dB 1 : –1 dB 3 : –2 dB 7 : –4.1 dB 15 : –6.2 dB 31 : –8.2 dB 63 : –11.5 dB Others: Do not use

7.6.1.1.3.4 Register 72h (address = 72h) [reset = 0h], ANALOG Page

Figure 7-48. Register 72h

7	6	5	4	3	2	1	0
0	0	0	0	EMP_LANE_B[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-27. Register 72h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0

Table 7-27. Register 72h Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	EMP_LANE_B[3:0]	R/W	0h	De-emphasis for lane B. These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 : 0 dB 1 : –1 dB 3 : –2 dB 7 : –4.1 dB 15 : –6.2 dB 31 : –8.2 dB 63 : –11.5 dB Others: Do not use

7.6.1.1.3.5 Register 93h (address = 93h) [reset = 0h], ANALOG Page

Figure 7-49. Register 93h

7	6	5	4	3	2	1	0
EMP_LANE_D[5:4]		EMP_LANE_C					
R/W-0h		R/W-0h					

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-28. Register 93h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EMP_LANE_D[5:4]	R/W	0h	De-emphasis for lane D. These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 : 0 dB 1 : –1 dB 3 : –2 dB 7 : –4.1 dB 15 : –6.2 dB 31 : –8.2 dB 63 : –11.5 dB Others: Do not use
5-0	EMP_LANE_C	R/W	0h	De-emphasis for lane C. These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 : 0 dB 1 : –1 dB 3 : –2 dB 7 : –4.1 dB 15 : –6.2 dB 31 : –8.2 dB 63 : –11.5 dB Others: Do not use

7.6.1.1.3.6 Register 94h (address = 94h) [reset = 0h], ANALOG Page

Figure 7-50. Register 94h

7	6	5	4	3	2	1	0
0	0	0	0	EMP_LANE_D[3:0]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-29. Register 94h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3-0	EMP_LANE_D[3:0]	R/W	0h	De-emphasis for lane D. These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period. 0 : 0 dB 1 : –1 dB 3 : –2 dB 7 : –4.1 dB 15 : –6.2 dB 31 : –8.2 dB 63 : –11.5 dB Others: Do not use

7.6.1.1.3.7 Register 9Bh (address = 9Bh) [reset = 0h], ANALOG Page

Figure 7-51. Register 9Bh

7	6	5	4	3	2	1	0
0	0	0	SYSREF_PDN	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-30. Register 9Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0h	Must read or write 0
4	SYSREF_PDN	R/W	0h	This bit powers down the SYSREF buffer. 0 : SYSREF buffer is powered up 1 : SYSREF buffer is powered down
3-0	0	R/W	0h	Must read or write 0

7.6.1.1.3.8 Register 9Dh (address = 9Dh) [reset = 0h], ANALOG Page

Figure 7-52. Register 9Dh

7	6	5	4	3	2	1	0
PDN_CHA	PDN_CHB	0	0	PDN_CHD	PDN_CHC	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-31. Register 9Dh Field Descriptions

Bit	Field	Type	Reset	Description
7	PDN_CHA	R/W	0h	This bit powers down channel A. 0 : Normal operation 1 : Channel A is powered down
6	PDN_CHB	R/W	0h	This bit powers down channel B. 0 : Normal operation 1 : Channel B is powered down
5-4	0	R/W	0h	Must read or write 0
3	PDN_CHD	R/W	0h	This bit powers down channel D. 0 : Normal operation 1 : Channel D is powered down

Table 7-31. Register 9Dh Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	PDN_CHC	R/W	0h	This bit powers down channel C. 0 : Normal operation 1 : Channel C is powered down
1-0	0	R/W	0h	Must read or write 0

7.6.1.1.3.9 Register 9Eh (address = 9Eh) [reset = 0h], ANALOG Page

Figure 7-53. Register 9Eh

7	6	5	4	3	2	1	0
0	0	0	PDN_SYNCAB	0	0	0	PDN_GLOBAL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-32. Register 9Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0h	Must read or write 0
4	PDN_SYNCAB	R/W	0h	This bit controls the STNCAB buffer power-down. 0 : SYNCAB buffer is powered up 1 : SYNCAB buffer is powered down
3-1	0	R/W	0h	Must read or write 0
0	PDN_GLOBAL	R/W	0h	This bit controls the global power-down. 0 : Global power-up 1 : Global power-down

7.6.1.1.3.10 Register 9Fh (address = 9Fh) [reset = 0h], ANALOG Page

Figure 7-54. Register 9Fh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PIN_PDN_MODE	FAST_PDN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-33. Register 9Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must read or write 0
1	PIN_PDN_MODE	R/W	0h	This bit selects the pin power-down mode. 0 : PDN pin is configured to fast power-down 1 : PDN pin is configured to global power-down
0	FAST_PDN	R/W	0h	This bit controls the fast power-down. 0 : Device powered up 1 : Fast power down

7.6.1.1.3.11 Register AFh (address = AFh) [reset = 0h], ANALOG Page

Figure 7-55. Register AFh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PDN_SYNCCD	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-34. Register AFh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must read or write 0
1	PDN_SYNCCD	R/W	0h	This bit controls the SYNCCD buffer power-down. 0 : SYNCCD buffer is powered up 1 : SYNCCD buffer is powered down
0	0	R/W	0h	Must read or write 0

7.6.1.1.4 SERDES_XX Page Register Description

7.6.1.1.4.1 Register 20h (address = 20h) [reset = 0h], SERDES_XX Page

Figure 7-56. Register 20h

7	6	5	4	3	2	1	0
CTRL_K	CTRL_SER_MODE	0	TRANS_TEST_EN	0	LANE_ALIGN	FRAME_ALIGN	TX_ILA_DIS
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-35. Register 20h Field Descriptions

Bit	Field	Type	Reset	Description
7	CTRL_K	R/W	0h	This bit is the enable bit for programming the number of frames per multi-frame. 0 : Default: 5 frames per multi-frame 1 : Frames per multi-frame can be programmed using register 26h
6	CTRL_SER_MODE	R/W	0h	This bit allows the SerDes_MODE setting in register 21h (bits 1-0) to be changed. 0 : Disabled 1 : Enables SerDes_MODE setting
5	0	R/W	0h	Must read or write 0
4	TRANS_TEST_EN	R/W	0h	This bit generates the long transport layer test pattern mode, as per section 5.1.6.3 of the JESD204B specification. 0 : Test mode is disabled 1 : Test mode is enabled
3	0	R/W	0h	Must read or write 0
2	LANE_ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.3) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 : Normal operation 1 : Inserts lane alignment characters
1	FRAME_ALIGN	R/W	0h	This bit inserts the lane alignment character (K28.7) for the receiver to align to the lane boundary, as per section 5.3.3.5 of the JESD204B specification. 0 : Normal operation 1 : Inserts frame alignment characters
0	TX_ILA_DIS	R/W	0h	This bit disables sending the initial link alignment (ILA) sequence when SYNC is deasserted. 0 = Normal operation 1 = Disables ILA

7.6.1.1.4.2 Register 21h (address = 21h) [reset = 0h], SERDES_XX Page

Figure 7-57. Register 21h

7	6	5	4	3	2	1	0
SYNC_REQ	OPT_SYNC_REQ	SYNCB_SEL_AB_CD	0	0	0	SerDes_MODE	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-36. Register 21h Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC_REQ	R/W	0h	This bit controlls the SYNC register (bit 6 must be enabled). 0 : Normal operation 1 : ADC output data are replaced with K28.5 characters
6	OPT_SYNC_REQ	R/W	0h	This bit enables SYNC operation. 0 : Normal operation 1 : Enables SYNC from the SYNC_REQ register bit
5	SYNCB_SEL_AB_CD	R/W	0h	This bit selects which SYNCb input controls the JESD interface. 0 : Use the SYNCbAB, SYNCbCD pins 1 : When set in the SerDes AB SPI, SYNCbCD is used for the SerDes AB and CD. When set in the SerDes CD SPI, SYNCbAB is used for the SerDes AB and CD
4-2	0	R/W	0h	Must read or write 0
1-0	SerDes_MODE	R/W	0h	These bits set the JESD output parameters. The CTRL_SER_MODE bit (register 20h, bit 6) must also be set to control these bits. These bits are auto configured for modes 0, 1, 3, and 7, but must be configured for modes 2, 4, and 6.

7.6.1.1.4.3 Register 22h (address = 22h) [reset = 0h], SERDES_XX Page

Figure 7-58. Register 22h

7	6	5	4	3	2	1	0
LINK_LAYER_TESTMODE_SEL			RPAT_SET_DISP	LMFC_MASK_RESET	0	0	0
R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-37. Register 22h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LINK_LAYER_TESTMODE_SEL	R/W	0h	These bits generate a pattern as per section 5.3.3.8.2 of the JESD204B document. 0 : Normal ADC data 1 : D21.5 (high-frequency jitter pattern) 2 : K28.5 (mixed-frequency jitter pattern) 3 : Repeat the initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 4 : 12-octet RPAT jitter pattern 6 : PRBS pattern (PRBS7, 15, 23, 31). Use PRBS_MODE (register 36h, bits 7-6) to select the PRBS pattern.
4	RPAT_SET_DISP	R/W	0h	This bit changes the running disparity in the modified RPAT pattern test mode (only when the link layer test mode = 100). 0 : Normal operation 1 : Changes disparity
3	LMFC_MASK_RESET	R/W	0h	0 : Default 1 : Resets the LMFC mask
2-0	0	R/W	0h	Must read or write 0

7.6.1.1.4.4 Register 23h (address = 23h) [reset = 0h], SERDES_XX Page

Figure 7-59. Register 23h

7	6	5	4	3	2	1	0
FORCE_LMFC_COUNT	LMFC_CNT_INIT					RELEASE_ILANE_REQ	
R/W-0h	R/W-0h					R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-38. Register 23h Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE_LMFC_COUNT	R/W	0h	This bit forces an LMFC count. 0 : Normal Operation 1 : Enables using a different starting value for the LMFC counter
6-2	LMFC_CNT_INIT	R/W	0h	These bits set the initial value to which the LMFC count resets. The FORCE_LMFC_COUNT register bit must be enabled.
1-0	RELEASE_ILANE_REQ	R/W	0h	These bits delay the generation of the lane alignment sequence by 0, 1, 2, or 3 multi-frames after the code group synchronization. 0 : 0 multi-frames 1 : 1 multi-frame 2 : 2 multi-frames 3 : 3 multi-frames

7.6.1.1.4.5 Register 25h (address = 25h) [reset = 0h], SERDES_XX Page

Figure 7-60. Register 25h

7	6	5	4	3	2	1	0
SCR_EN	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-39. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
7	SCR_EN	R/W	0h	This bit is the scramble enable bit in the JESD204B interface. 0 : Scrambling is disabled 1 : Scrambling is enabled
6-0	0	R/W	0h	Must read or write 0

7.6.1.1.4.6 Register 26h (address = 26h) [reset = 0h], SERDES_XX Page

Figure 7-61. Register 26h

7	6	5	4	3	2	1	0
0	0	0	K_NO_OF_FRAMES_PER_MULTIFRAME				
R/W-0h	R/W-0h	R/W-0h	R/W-0h				

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-40. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0h	Must read or write 0
4-0	K_NO_OF_FRAMES_PER_MULTIFRAME	R/W	0h	These bits set the number of frames per multi-frame. The K value used is set value + 1 (for example, if the set value is 0xF, then K = 16).

7.6.1.1.4.7 Register 28h (address = 28h) [reset = 0h], SERDES_XX Page

Figure 7-62. Register 28h

7	6	5	4	3	2	1	0
0	0	0	0	CTRL_LID	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-41. Register 28h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3	CTRL_LID	R/W	0h	This bit is the enable bit to program the lane ID (LID). 0 : Default LID 1 : Enable LID programming
2-0	0	R/W	0h	Must read or write 0

7.6.1.1.4.8 Register 2Dh (address = 2Dh) [reset = 0h], SERDES_XX Page

Figure 7-63. Register 2Dh

7	6	5	4	3	2	1	0
LID1				LID2			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-42. Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LID1	R/W	0h	Lane ID for channels A, C. Select SerDes AB for channel A and SerDes CD for channel C. Valid only when CTRL_LID = 1.
3-0	LID2	R/W	0h	Lane ID for channels B, D. Select SerDes AB for channel B and SerDes CD for channel D.

7.6.1.1.4.9 Register 36h (address = 36h) [reset = 0h], SERDES_XX Page

Figure 7-64. Register 36h

7	6	5	4	3	2	1	0
PRBS_MODE		0	0	0	0	0	0
R-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-43. Register 36h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PRBS_MODE	R	0h	These bits select the PRBS polynomial in the PRBS pattern mode. 0 : PRBS7 1 : PRBS15 2 : PRBS23 3 : PRBS31
5-0	0	R/W	0h	Must read or write 0

7.6.1.1.4.10 Register 37h (address = 37h) [reset = 0h], SERDES_XX Page

Figure 7-65. Register 37h

7	6	5	4	3	2	1	0
LSB1_HR_ FLAG_EN	LSB0_HR_ FLAG_EN	LOAD_RES	TRIG_SEL_AB _CD	AUTO_TRIG_ EN	0	RATIO_ INVALID	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-44. Register 37h Field Descriptions

Bit	Field	Type	Reset	Description
7	LSB1_HR_FLAG_EN	R/W	0h	This bit enables the HiRes flag on LSB1. 0 : LSB1 is stuck to 0 1 : LSB1 carries the high-resolution flag
6	LSB0_HR_FLAG_EN	R/W	0h	This bit enables the HiRes flag on LSB0. 0 : LSB0 is stuck to 0 1 : LSB0 carries the high-resolution flag
5	LOAD_RES	R/W	0h	This bit enables loading of high- or low-resolution values. 0 : High- and low-resolution values are not updated 1 : High- and low-resolution values are updated
4	TRIG_SEL_AB_CD	R/W	0h	This bit determines if the TRIGAB or TRIGCD pin is used for burst mode; must be configured individually for channel AB and channel CD with paging. 0 : Uses the TRIGAB, TRIGCD pin separately 1 : Uses the TRIGCD pin when set for the SerDes AB SPI; uses the TRIGAB pin when set for the SerDes CD SPI
3	AUTO_TRIG_EN	R/W	0h	This bit enables an automatic trigger in burst mode (ignores the TRIGAB, TRIGCD inputs). 0 : Disable auto trigger; trigger is accepted from the pin 1 : Enable auto trigger; pin trigger is ignored
2	0	R/W	0h	Must read or write 0
1	RATIO_INVALID	R	0h	This bit generates an alarm flag when the duty cycle ratio between the high- and low-resolution counter is set incorrectly. 0 : LowRes, HighRes ratio is valid (≥ 3) 1 : LowRes, HighRes ratio is valid (< 3)
0	0	R/W	0h	Must read or write 0

7.6.1.1.4.11 Register 39h (address = 39h) [reset = 0h], SERDES_XX Page

Figure 7-66. Register 39h

7	6	5	4	3	2	1	0
0	0	0	0	LOWRESCOUNT[27:24]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-45. Register 39h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3-0	LOWRESCOUNT[27:24]	R	0h	28-bit, low-resoluton sample count.

7.6.1.1.4.12 Register 3Ah (address = 3Ah) [reset = 0h], SERDES_XX Page

Figure 7-67. Register 3Ah

7	6	5	4	3	2	1	0
LOWRESCOUNT[23:16]							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 7-46. Register 3Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOWRESCOUNT[23:16]	R	0h	28-bit, low-resoluton sample count.

7.6.1.1.4.13 Register 3Bh (address = 3Bh) [reset = 0h], SERDES_XX Page

Figure 7-68. Register 3Bh

7	6	5	4	3	2	1	0
LOWRESCOUNT[15:8]							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 7-47. Register 3Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOWRESCOUNT[15:8]	R	0h	28-bit, low-resoluton sample count.

7.6.1.1.4.14 Register 3Ch (address = 3Ch) [reset = 0h], SERDES_XX Page

Figure 7-69. Register 3Ch

7	6	5	4	3	2	1	0
LOWRESCOUNT[7:0]							
R-0h							

LEGEND: R = Read only; -n = value after reset

Table 7-48. Register 3Ch Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOWRESCOUNT[7:0]	R	0h	28-bit, low-resoluton sample count.

7.6.1.1.4.15 Register 3Dh (address = 3Dh) [reset = 0h], SERDES_XX Page

Figure 7-70. Register 3Dh

7	6	5	4	3	2	1	0
0	0	0	0	HIGHRESCOUNT[27:24]			
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-49. Register 3Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3-0	HIGHRESCOUNT[27:24]	R/W	0h	28-bit, high-resoluton sample count.

7.6.1.1.4.16 Register 3Eh (address = 3Eh) [reset = 0h], SERDES_XX Page

Figure 7-71. Register 3Eh

7	6	5	4	3	2	1	0
HIGHRESCOUNT[23:16]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-50. Register 3Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGHRESCOUNT[23:16]	R/W	0h	28-bit, high-resoluton sample count.

7.6.1.1.4.17 Register 3Fh (address = 3Fh) [reset = 0h], SERDES_XX Page

Figure 7-72. Register 3Fh

7	6	5	4	3	2	1	0
HIGHRESCOUNT[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-51. Register 3Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGHRESCOUNT[15:8]	R/W	0h	28-bit, high-resoluton sample count.

7.6.1.1.4.18 Register 40h (address = 40h) [reset = 0h], SERDES_XX Page

Figure 7-73. Register 40h

7	6	5	4	3	2	1	0
HIGHRESCOUNT[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-52. Register 40h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGHRESCOUNT[7:0]	R/W	0h	28-bit, high-resoluton sample count.

7.6.1.1.4.19 Register 41h (address = 41h) [reset = 0h], SERDES_XX Page

Figure 7-74. Register 41h

7	6	5	4	3	2	1	0
LANE_BONA				LANE_AONB			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-53. Register 41h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LANE_BONA	R/W	0h	These bits enable lane swap. 0 : Default 10 : Channel B on lane A; for SerDes CD, channel D on lane C Others: Do not use
3-0	LANE_AONB	R/W	0h	These bits enable lane swap. 0 : Default 10 : Channel A on lane B; for SerDes CD, Channel C on lane D Others: Do not use

7.6.1.1.4.20 Register 42h (address = 42h) [reset = 0h], SERDES_XX Page

Figure 7-75. Register 42h

7	6	5	4	3	2	1	0
0	0	0	0	INVERT_AC		INVERT_BD	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-54. Register 42h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3-2	INVERT_AC	R/W	0h	These bits invert lanes A and C. 0 : No inversion 3 : Data inversion on lane A, C Others: Do not use
1-0	INVERT_BD	R/W	0h	These bits invert lanes B and D. 0 : No inversion 3 : Data inversion on lane B, D Others: Do not use

7.6.1.1.5 CHX Page Register Description

7.6.1.1.5.1 Register 26h (address = 26h) [reset = 0h], CHX Page

Figure 7-76. Register 26h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	GAINWORD	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-55. Register 26h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must read or write 0
1-0	GAINWORD	R/W	0h	These bits control the channel A gain word. 0 : 0 dB 1 : 1 dB 2 : 2 dB 3 : 3 dB

7.6.1.1.5.2 Register 27h (address = 27h) [reset = 0h], CHX Page

Figure 7-77. Register 27h

7	6	5	4	3	2	1	0
OVR_ENABLE	OVR_FAST_SEL	0	0	OVR_LSB1	0	OVR_LSB0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-56. Register 27h Field Descriptions

Bit	Field	Type	Reset	Description
7	OVR_ENABLE	R/W	0h	This bit enables or disables the OVR on the JESD lanes. 0 : Disables OVR 1 : Enables OVR
6	OVR_FAST_SEL	R/W	0h	This bit selects the fast or delay-matched OVR 0 : Delay-matched OVR 1 : Fast OVR
5-4	0	R/W	0h	Must read or write 0
3	OVR_LSB1	R/W	0h	This bit selects either data or OVR on LSB1. 0 : Data selected 1 : OVR or FOVR selected
2	0	R/W	0h	Must read or write 0
1	OVR_LSB0	R/W	0h	This bit selects either data or OVR on LSB0. 0 : Data selected 1 : OVR or FOVR selected
0	0	R/W	0h	Must read or write 0

7.6.1.1.5.3 Register 2Dh (address = 2Dh) [reset = 0h], CHX Page

Figure 7-78. Register 2Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	NYQUIST_SELECT	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-57. Register 2Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0h	Must read or write 0
1	NYQUIST_SELECT	R/W	0h	This bit selects the Nyquist zone of operation for trim loading. 0 : Nyquist 1 1 : Nyquist 2
0	0	R/W	0h	Must read or write 0

7.6.1.1.5.4 Register 78h (address = 78h) [reset = 0h], CHX Page

Figure 7-79. Register 78h

7	6	5	4	3	2	1	0
0	0	0	0	0	FS4_SIGN	NYQ_SEL_MODE02	NYQ_SEL
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-58. Register 78h Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0h	Must read or write 0
2	FS4_SIGN	R/W	0h	This bit controls the sign of mixing in mode 0. 0 : Centered at $-f_S$ / 4 1 : Centered at f_S / 4
1	NYQ_SEL_MODE02	R/W	0h	This bit selects the pass band of the decimation filter in mode 2. 0 : Low pass 1 : High pass
0	NYQ_SEL	R/W	0h	This bit selects the pass band of the filter before the DDC. 0 : LPF (0 – f_S / 2) 1 : HPF (0 – f_S / 2)

7.6.1.1.5.5 Register 7Ah (address = 7Ah) [reset = 0h], CHX Page

Figure 7-80. Register 7Ah

7	6	5	4	3	2	1	0
NCO_WORD[15:8]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-59. Register 7Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO_WORD[15:8]	R/W	0h	These bits set the NCO frequency word. 0 : 0 × f_S / 2^{16} 1 : 1 × f_S / 2^{16} 2 : 2 × f_S / 2^{16} 3 : 3 × f_S / 2^{16} 5 : 5 × f_S / 2^{16} 6 : 6 × f_S / 2^{16} … 65535 : 65535 × f_S / 2^{16}

7.6.1.1.5.6 Register 7Bh (address = 7Bh) [reset = 0h], CHX Page

Figure 7-81. Register 7Bh

7	6	5	4	3	2	1	0
NCO_WORD[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-60. Register 7Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO_WORD[7:0]	R/W	0h	These bits set the NCO frequency word. 0 : 0 × f_S / 2^{16} 1 : 1 × f_S / 2^{16} 2 : 2 × f_S / 2^{16} 3 : 3 × f_S / 2^{16} 5 : 5 × f_S / 2^{16} 6 : 6 × f_S / 2^{16} … 65535 : 65535 × f_S / 2^{16}

7.6.1.1.5.7 Register 7Eh (address = 7Eh) [reset = 3h], CHX Page

Figure 7-82. Register 7Eh

7	6	5	4	3	2	1	0
0	0	0	0	0	MODE467_GAIN	MODE0_GAIN	MODE13_GAIN
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-61. Register 7Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0h	Must read or write 0
2	MODE467_GAIN	R/W	0h	This bit sets the mixer loss compensation for modes 4, 6, and 7. 0 : No gain 1 : 6-dB gain
1	MODE0_GAIN	R/W	1h	This bit sets the mixer loss compensation for mode 0. 0 : No gain 1 : 6-dB gain
0	MODE13_GAIN	R/W	1h	This bit sets the mixer loss compensation for modes 1 and 3. 0 : No gain 1 : 6-dB gain

7.6.1.1.6 ADCXX Page Register Description

7.6.1.1.6.1 Register 07h (address = 07h) [reset = FFh], ADCXX Page

Figure 7-83. Register 7h

7	6	5	4	3	2	1	0
FAST_OVR_THRESHOLD_HIGH							
R/W-FFh							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-62. Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FAST_OVR_THRESHOLD_HIGH	R/W	FFh	Fast OVR threshold high; see the *Section 7.4.1.14* section for programming.

7.6.1.1.6.2 Register 08h (address = 08h) [reset = 0h], ADCXX Page

Figure 7-84. Register 8h

7	6	5	4	3	2	1	0
FAST_OVR_THRESHOLD_LOW							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-63. Register 08h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FAST_OVR_THRESHOLD_LOW	R/W	0h	Fast OVR threshold low; see the *Section 7.4.1.14* section for programming.

7.6.1.1.6.3 Register D5h (address = D5h) [reset = 0h], ADCXX Page

Figure 7-85. Register D5h

7	6	5	4	3	2	1	0
0	0	0	0	CAL_EN	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 7-64. Register D5h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0h	Must read or write 0
3	CAL_EN	R/W	0h	This bit is the enable calibration bit. This bit must be toggled during the startup sequence. 0 : Disables calibration 1 : Enables calibration
2-0	0	R/W	0h	Must read or write 0

8 Application and Implementation

8.1 Application Information

8.1.1 Start-Up Sequence

Table 8-1 lists the recommended start-up sequence for a 500-MSPS, Nyquist 2 operation with DDC mode 0 enabled.

Table 8-1. Recommended Start-Up Sequence for 500-MSPS, Nyquist 2, DDC Mode 0 Operation

STEP	DESCRIPTION	REGISTER ADDRESS	REGISTER DATA	COMMENT
1	Provide a 1.15-V power supply (AVDD, DVDD, IOVDD)	—	—	—
2	Provide a 1.9-V power supply (AVDD19)	—	—	A 1.15-V supply must be supplied first for proper operation.
3	Provide a clock to CLKINM, CLKINP and a SYSREF signal to SYSREFM, SYSREFP	—	—	SYSREF must be established before SPI programming.
4	Pulse a reset (low to high to low) via a hardware reset (pin 50), wait 100 µs	—	—	Hardware reset loads all trim register settings.
5	Issue a software reset to initialize the registers	00h	81h	—
6	Set the high SNR mode for channels AB and CD, select trims for 500-MSPS operation	11h	00h	Select the DIGTOP page.
		12h	01h	
		13h	00h	
		ABh	01h	Set the high SNR mode for channel A and B.
		ACh	01h	Set the high SNR mode for channel C and D.
		64h	02h	Select trims for 500-MSPS operation.
7	Set up the SerDes configuration	11h	00h	Select the SerDes_AB and SerDes_CD pages.
		12h	60h	
		13h	00h	
		26h	0Fh	Set the K value to 16 frames per multi-frame.
		20h	80h	Enable the K value from register 26h.
8	ADC calibration	11h	FFh	Select the ADC_A1, ADC_A2, ADC_B1, ADC_B2, ADC_C1, ADC_C2, ADC_D1, and ADC_D2 pages.
		12h	00h	
		13h	00h	
		D5h	08h	Enable ADC calibration.
		Wait 2 ms		ADC calibration time.
		D5h	00h	Disable ADC calibration.
		2Ah	00h	Internal trims.
		CFh	50h	
9	Select trims for the second Nyquist	11h	00h	Select the channel A, channel B, channel C, and channel D pages.
		12h	1Eh	
		13h	00h	
		2Dh	02h	Select trims for the second Nyquist.
10	Load linearity trims	11h	00h	Select the DIGTOP page.
		12h	01h	
		13h	00h	
		8Ch	02h	Load linearity trims.
		B7h	01h	
		B7h	00h	
11	Disable SYSREF	11h	00h	Select the ANALOG page.
		12h	00h	
		13h	01h	
		6Ah	02h	Disable SYSREF.

Table 8-2 shows the recommended start-up sequence for a 375-MSPS, Nyquist 2 operation with DDC mode 0 enabled.

Table 8-2. Recommended Start-Up Sequence for 375-MSPS, Nyquist 2, DDC Mode 0 Operation

STEP	DESCRIPTION	REGISTER ADDRESS	REGISTER DATA	COMMENT
1	Provide a 1.15-V power supply (AVDD, DVDD, IOVDD)	—	—	—
2	Provide a 1.9-V power supply (AVDD19)	—	—	A 1.15-V supply must be supplied first for proper operation.
3	Provide a clock to CLKINM, CLKINP and a SYSREF signal to SYSREFM, SYSREFP	—	—	SYSREF must be established before SPI programming.
4	Pulse a reset (low to high to low) via a hardware reset (pin 50), wait 100 µs	—	—	Hardware reset loads all trim register settings.
5	Issue a software reset to initialize registers	00h	81h	—
6	Set the high SNR mode for channels AB and CD	11h	00h	Select the DIGTOP page.
		12h	01h	
		13h	00h	
		ABh	01h	Set the high SNR mode for channel A and B.
		ACh	01h	Set the high SNR mode for channel C and D.
7	Set up the SerDes configuration	11h	00h	Select the SerDes_AB and SerDes_CD pages.
		12h	60h	
		13h	00h	
		26h	0Fh	Set the K value to 16 frames per multi-frame.
		20h	80h	Enable the K value from register 26h.
8	ADC calibration	11h	FFh	Select the ADC_A1, ADC_A2, ADC_B1, ADC_B2, ADC_C1, ADC_C2, ADC_D1, and ADC_D2 pages.
		12h	00h	
		13h	00h	
		D5h	08h	Enable ADC calibration.
		Wait 2 ms		ADC calibration time.
		D5h	00h	Disable ADC calibration.
		2Ah	00h	Internal trims.
		CFh	50h	
9	Select trims for the second Nyquist.	11h	00h	Select the channel A, channel B, channel C, and channel D pages.
		12h	1Eh	
		13h	00h	
		2Dh	02h	Select trims for the second Nyquist.
10	Load linearity trims	11h	00h	Select the DIGTOP page.
		12h	01h	
		13h	00h	
		8Ch	02h	Load linearity trims.
		B7h	01h	
		B7h	00h	
11	Disable SYSREF	11h	00h	Select the ANALOG page.
		12h	00h	
		13h	01h	
		6Ah	02h	Disable SYSREF.

8.1.2 Hardware Reset

Timing information for the hardware reset is shown in Figure 8-1.

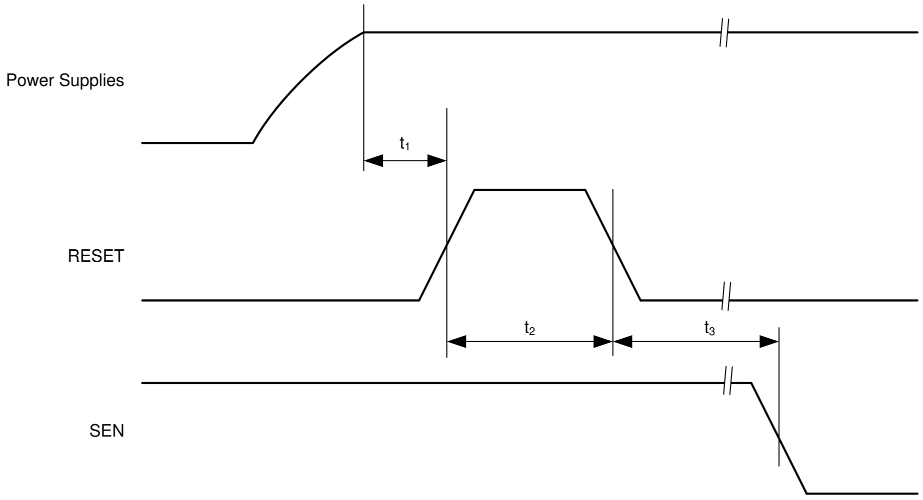


Figure 8-1. Hardware Reset Timing Diagram

Table 8-3. Timing Requirements for Figure 8-1

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10			ns
t_3	Register write delay from RESET disable to SEN active	100			µs

8.1.3 Frequency Planning

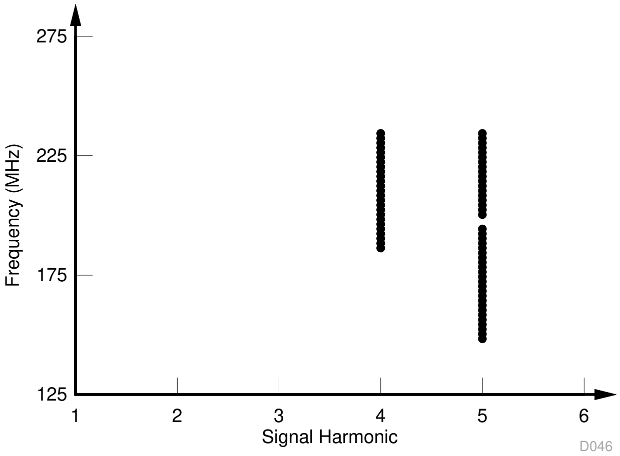
The ADS58J64 uses an architecture where the ADCs are 2x interleaved followed by a digital decimation by 2. The 2x interleaved and decimation architecture comes with a unique advantage of improved linearity resulting from frequency planning. Frequency planning refers to choosing the clock frequency and signal band appropriately such that the harmonic distortion components, resulting from the analog front-end (LNA, PGA), can be made to fall outside the decimation filter pass band. In absence of the 2x interleave and decimation architecture, these components alias back in band and limit the performance of the signal chain. For example, for f_{CLK} = 983.04 MHz and f_{IN} = 184.32 MHz:

Second-order harmonic distortion (HD2) = 2 × 184.32 = 368.64 MHz

Pass band of the 2x decimation filter = 0 MHz to 245.76 MHz (0 to f_{CLK} / 4)

The second-order harmonic performance improves by the stop-band attenuation of the filter (approximately 40 dBc) because the second-order harmonic frequency is outside the pass band of the decimation filter.

Figure 8-2 shows the harmonic components (HD2–HD5) that fall in the decimation pass band for the input clock rate (f_{CLK}) of the 983.04-MHz and 100-MHz signal band around the center frequency of 184.32 MHz.



f_{CLK} = 983.04 MHz, signal band = 134.32 MHz to 234.32 MHz

Figure 8-2. In-Band Harmonics for a Frequency Planned System

As shown in Figure 8-2, both HD2 and HD3 are completely out of band. HD4 and HD5 fall in the decimation pass band for some frequencies of the input signal band.

Through proper frequency planning, the specifications of the ADC antialias filter can be relaxed.

8.1.4 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors (as shown in Equation 3): the quantization noise is typically not noticeable in pipeline converters and is 84 dB for a 14-bit ADC. The thermal noise limits the SNR at low input frequencies and the clock jitter sets the SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20log\sqrt{\left(10^{-\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \qquad (3)$$

The SNR limitation resulting from sample clock jitter can be calculated by Equation 4:

$$SNR_{Jitter}[dBc] = -20log(2\pi \times f_{in} \times T_{Jitter}) \qquad (4)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (100 fs for the ADS58J64) that is set by the noise of the clock input buffer and the external clock jitter. T_{Jitter} can be calculated by Equation 5:

$$T_{Jitter} = \sqrt{(T_{Jitter,\ Ext\_Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \qquad (5)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input; a faster clock slew rate also improves the ADC aperture jitter.

The ADS58J64 has a thermal noise of approximately 70 dBFS and an internal aperture jitter of 100 fs.

8.1.5 ADC Test Pattern

The ADS58J64 provides several different options to output test patterns instead of the actual output data of the ADC in order to simplify debugging of the JESD204B digital interface link. The output data path is shown in Figure 8-3.

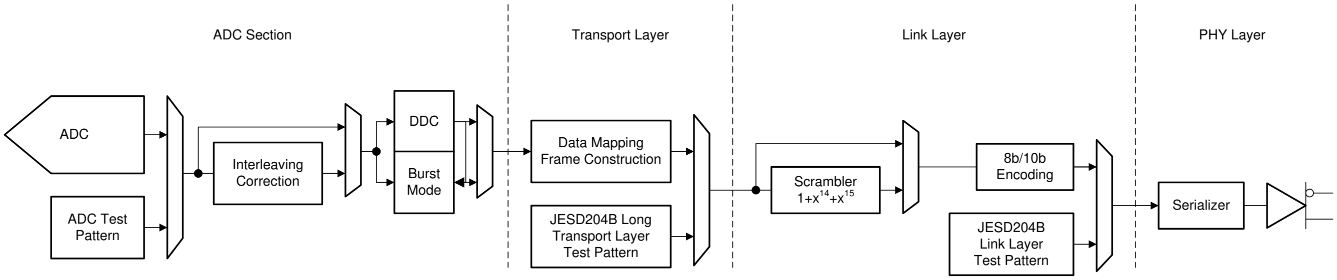


Figure 8-3. ADC Test Pattern

8.1.5.1 ADC Section

The ADC test pattern replaces the actual output data of the ADC. These test patterns can be programmed using register 91h of the DIGTOP page. The supported test patterns are shown in Table 8-4.

Table 8-4. ADC Test Pattern Settings

BIT	NAME	DEFAULT	DESCRIPTION
7-4	TESTPATTERNSELECT	0000	These bits select the test pattern on the output when the test pattern is enabled for a suitable channel. 0 : Default 1 : All zeros 2 : All ones 3 : Toggle pattern 4 : Ramp pattern 6 : Custom pattern 1 7 : Toggles between custom pattern 1 and custom pattern 2 8 : Deskew pattern (AAAAh)

8.1.5.2 Transport Layer Pattern

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0s are added when needed. Alternatively, the JESD204B long transport layer test pattern can be substituted by programming register 20h, as shown in Table 8-5.

Table 8-5. Transport Layer Test Mode

BIT	NAME	DEFAULT	DESCRIPTION
4	TRANS_TEST_EN	0	This bit generates the long transport layer test pattern mode according to clause 5.1.6.3 of the JESD204B specification. 0 = Test mode disabled 1 = Test mode enabled

8.1.5.3 Link Layer Pattern

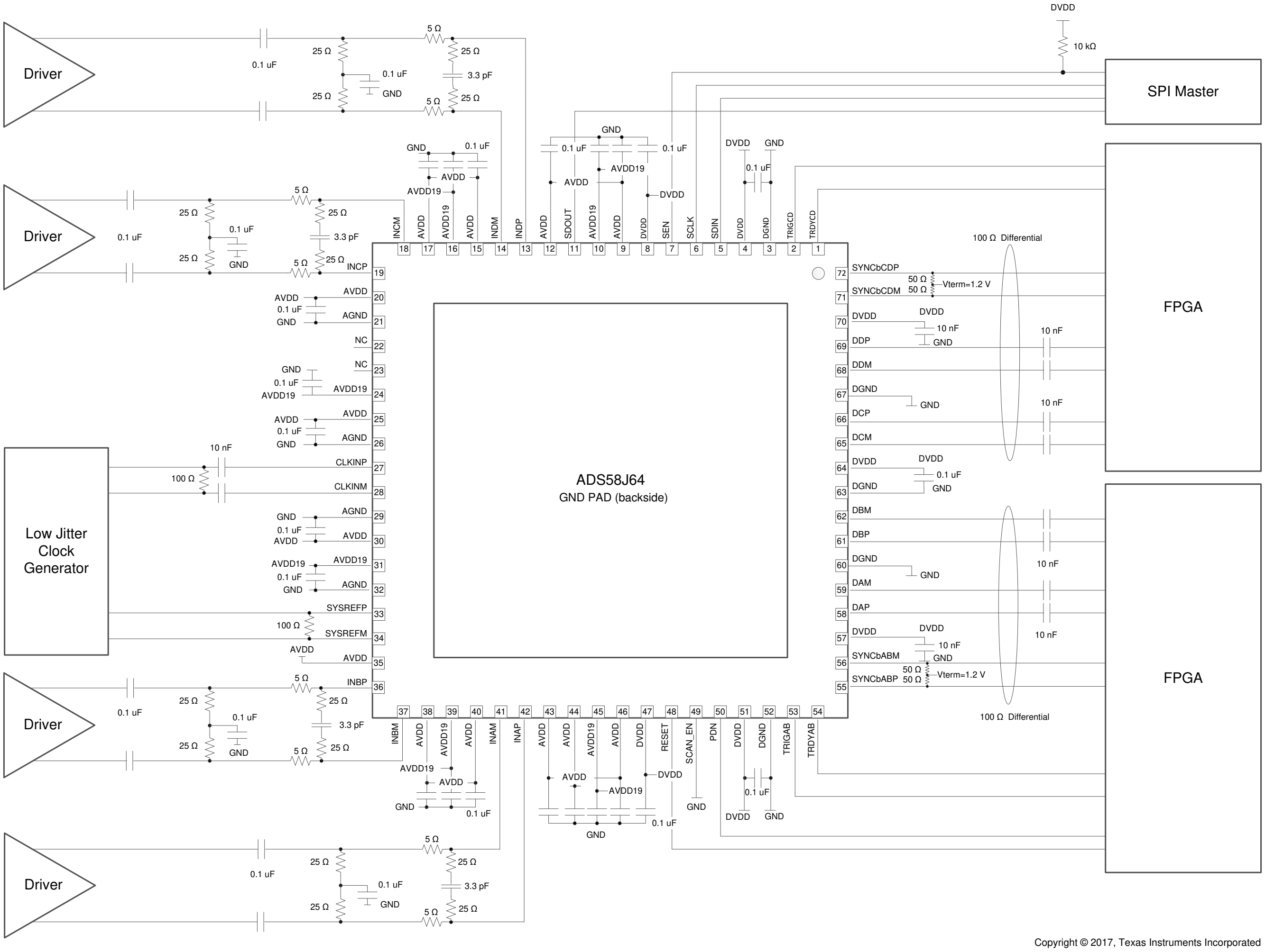
The link layer contains the scrambler and the 8b, 10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that can be manually restarted. The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b, 10b encoder. These test patterns can be used by programming register 22h of the SERDES_XX page. Table 8-6 shows the supported programming options.

Table 8-6. Link Layer Test Mode

BIT	NAME	DEFAULT	DESCRIPTION
7-5	LINK_LAYER_TESTMODE_SEL	000	These bits generate a pattern according to clause 5.3.3.8.2 of the JESD204B document. 0 : Normal ADC data 1 : D21.5 (high-frequency jitter pattern) 2 : K28.5 (mixed-frequency jitter pattern) 3 : Repeats initial lane alignment (generates a K28.5 character and continuously repeats lane alignment sequences) 4 : 12-octet RPAT jitter pattern 6 : PRBS pattern (PRBS7,15,23,31); use PRBS mode (register 36h) to select the PRBS pattern

8.2 Typical Application

The ADS58J64 is designed for wideband receiver applications demanding excellent dynamic range over a large input frequency range. A typical schematic for an ac-coupled dual receiver [dual field-programmable gate array (FPGA) with a dual SYNC] is shown in Figure 8-4.



NOTE: GND = AGND and DGND are connected in the PCB layout.

Figure 8-4. Application Diagram for the ADS58J64

8.2.1 Design Requirements

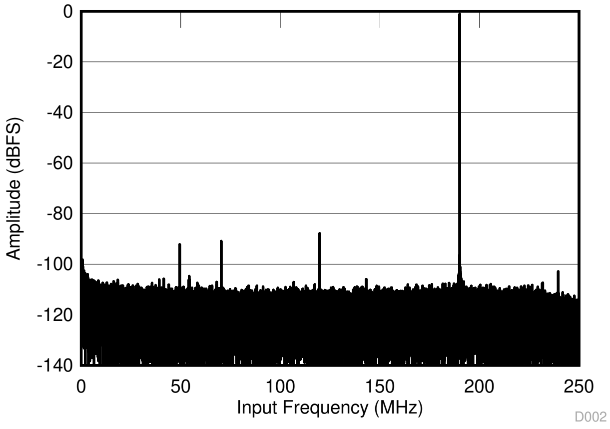
By using the simple drive circuit of Figure 8-4 (when the amplifier drives the ADC) or Figure 7-1 (when transformers drive the ADC), uniform performance can be obtained over a wide frequency range. The buffers present at the analog inputs of the device help isolate the external drive source from the switching currents of the sampling circuit.

8.2.2 Detailed Design Procedure

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics, as shown in Figure 8-4.

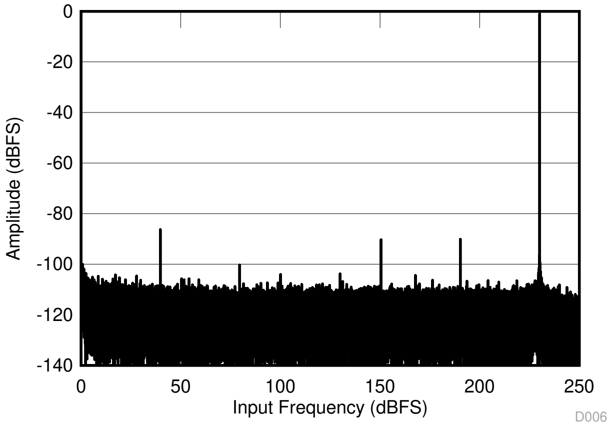
8.2.3 Application Curves

Figure 8-5 and Figure 8-6 show the typical performance at 190 MHz and 230 MHz, respectively.



f_{IN} = 190 MHz, A_{IN} = –1 dBFS, SNR = 69.4 dBFS, SFDR = 88 dBc, SFDR = 96 dBc (non 23)

Figure 8-5. FFT for 190-MHz Input Signal



f_{IN} = 230 MHz, A_{IN} = –1 dBFS, SNR = 69.4 dBFS, SFDR = 85 dBc, SFDR = 96 dBc (non 23)

Figure 8-6. FFT for 230-MHz Input Signal

9 Power Supply Recommendations

The device requires a 1.15-V nominal supply for DVDD, a 1.15-V nominal supply for AVDD, and a 1.9-V nominal supply for AVDD19. AVDD and DVDD are recommended to be powered up the before AVDD19 supply for reliable loading of factory trims.

10 Layout

10.1 Layout Guidelines

The device evaluation module (EVM) layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 10-1. A complete layout of the EVM is available at the ADS58J64 EVM folder. Some important points to remember during board layout are:

- Analog inputs are located on opposite sides of the device pinout to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pinout in opposite directions, as shown in the reference layout of Figure 10-1 as much as possible.
- In the device pinout, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 10-1 as much as possible.
- Keep digital outputs away from the analog inputs. When these digital outputs exit the pinout, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from the digital outputs to the analog inputs and degrade performance. All digital output traces to the receiver [such as an FPGA or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
- At each power-supply pin (AVDD, DVDD, or AVDD19), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

10.2 Layout Example

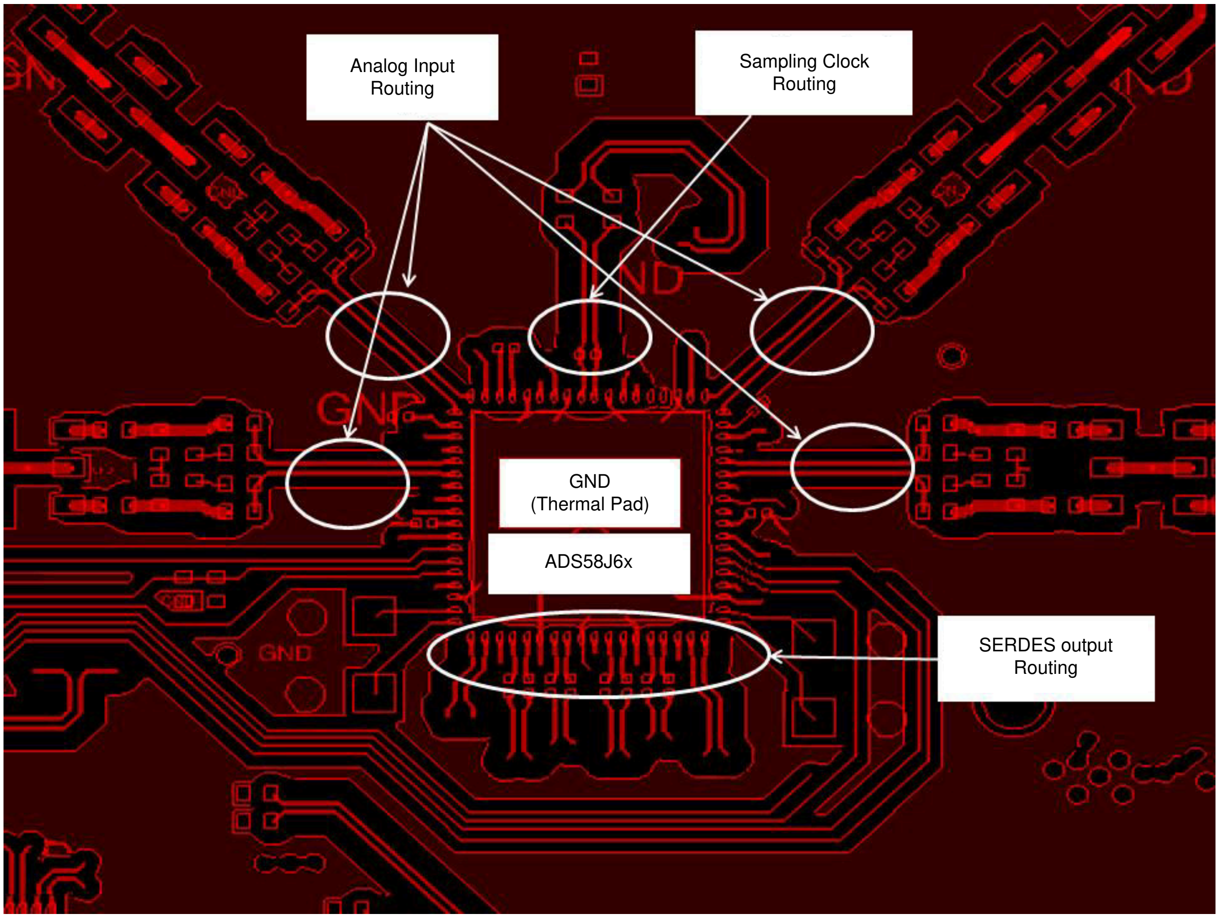


Figure 10-1. ADS58J64EVM Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS58J64IRMPR	ACTIVE	VQFN	RMP	72	1500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ58J64	Samples
ADS58J64IRMPT	ACTIVE	VQFN	RMP	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ58J64	Samples
ADS58J64IRRHR	ACTIVE	VQFN	RRH	72	1500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ58J64	Samples
ADS58J64IRRHT	ACTIVE	VQFN	RRH	72	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ58J64	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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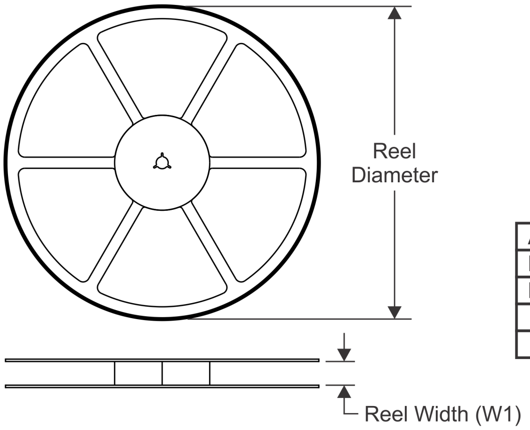
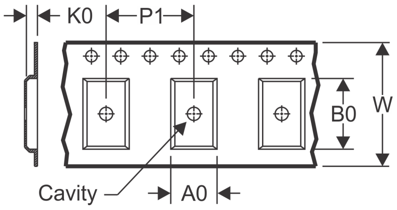
TAPE AND REEL INFORMATION

REEL DIMENSIONS

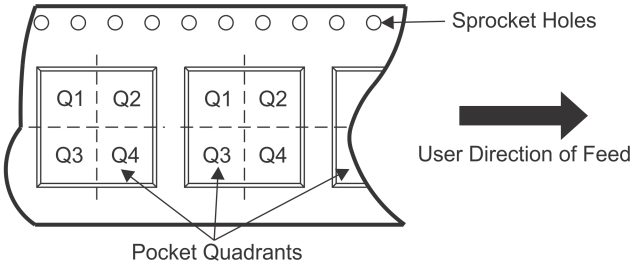


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

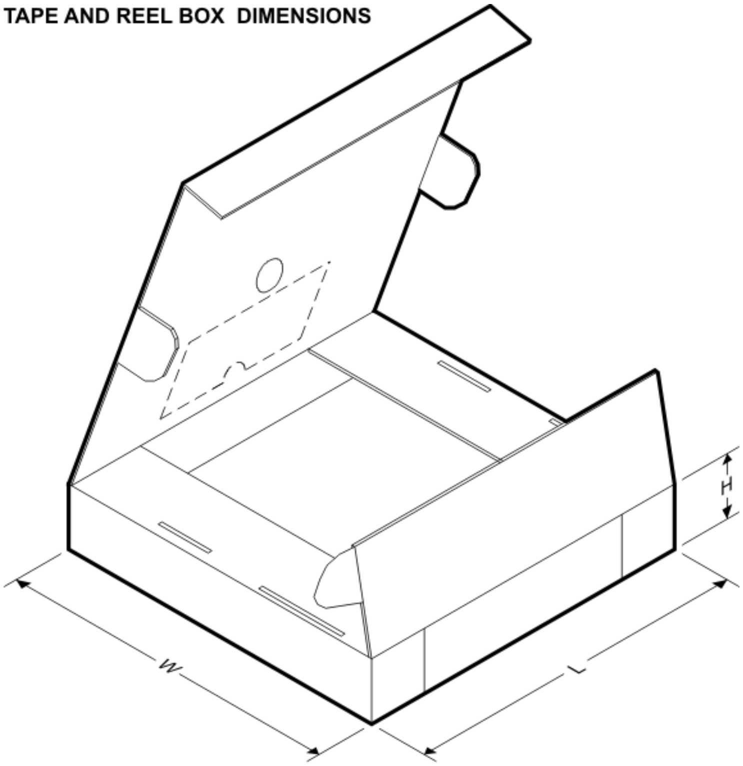
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

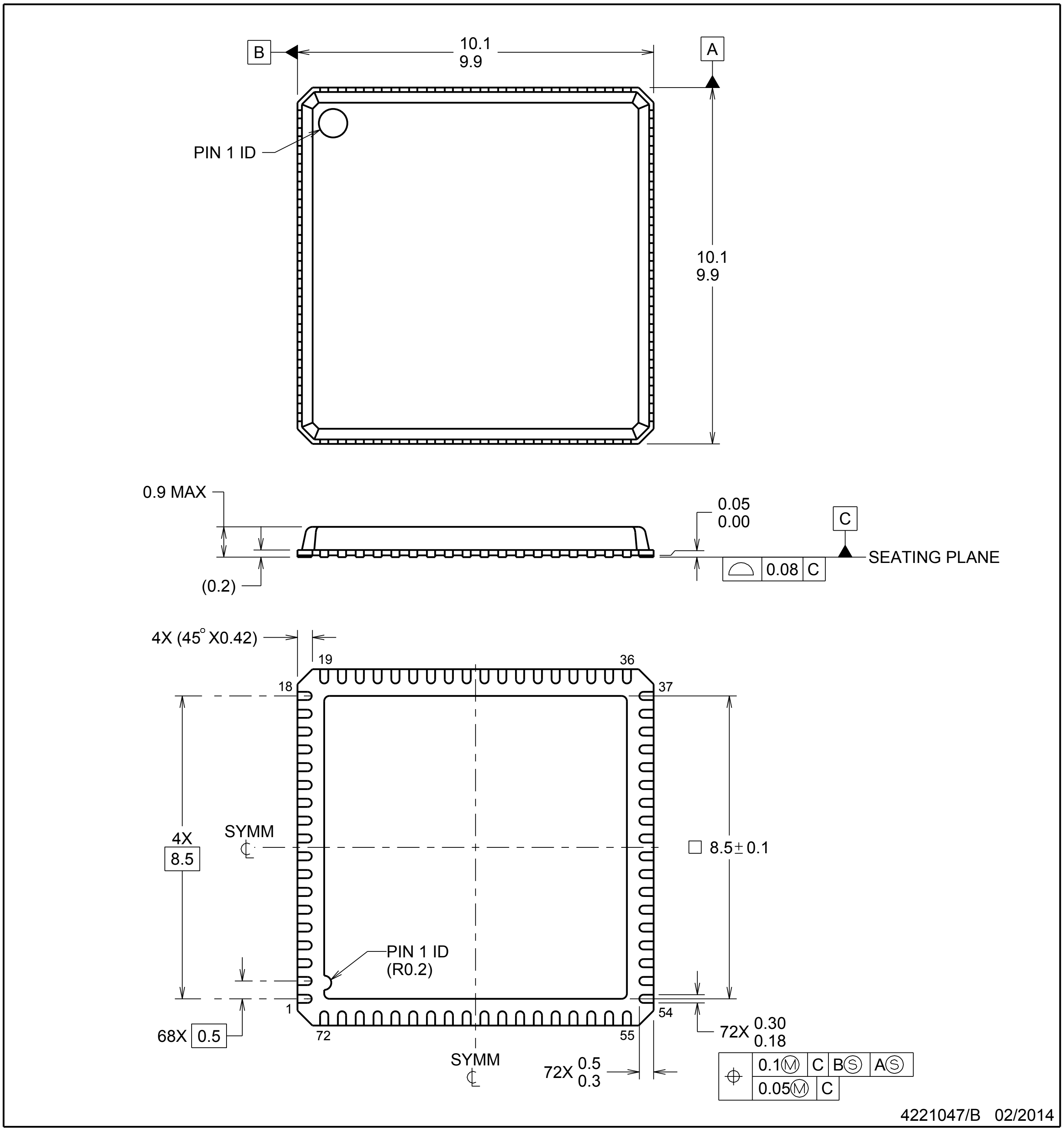
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS58J64IRMPR	VQFN	RMP	72	1500	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2
ADS58J64IRRHR	VQFN	RRH	72	1500	330.0	24.4	10.25	10.25	2.25	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



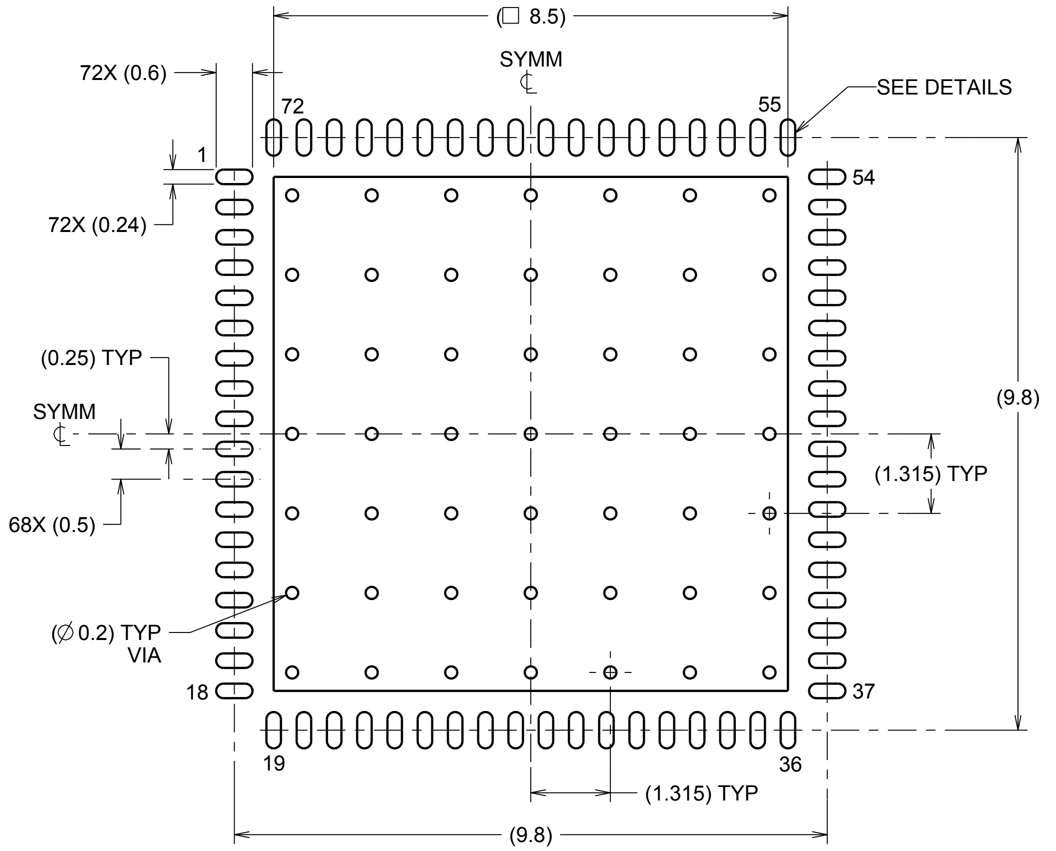
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS58J64IRMPR	VQFN	RMP	72	1500	350.0	350.0	43.0
ADS58J64IRRHR	VQFN	RRH	72	1500	350.0	350.0	43.0

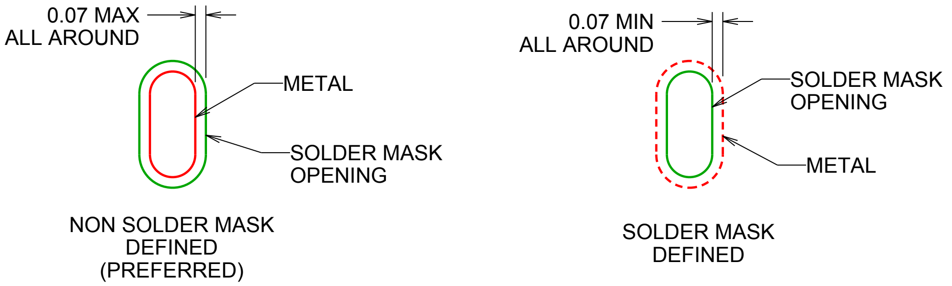


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X

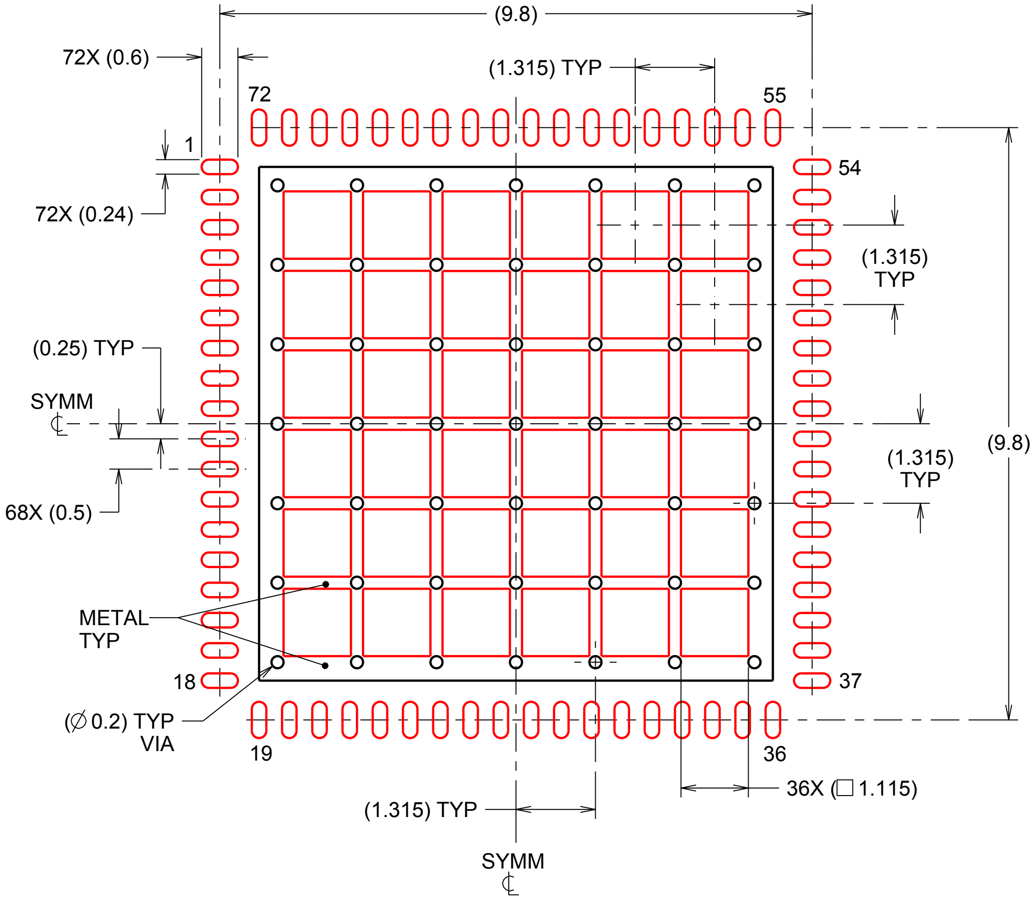


SOLDER MASK DETAILS

4221047/B 02/2014

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
62% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

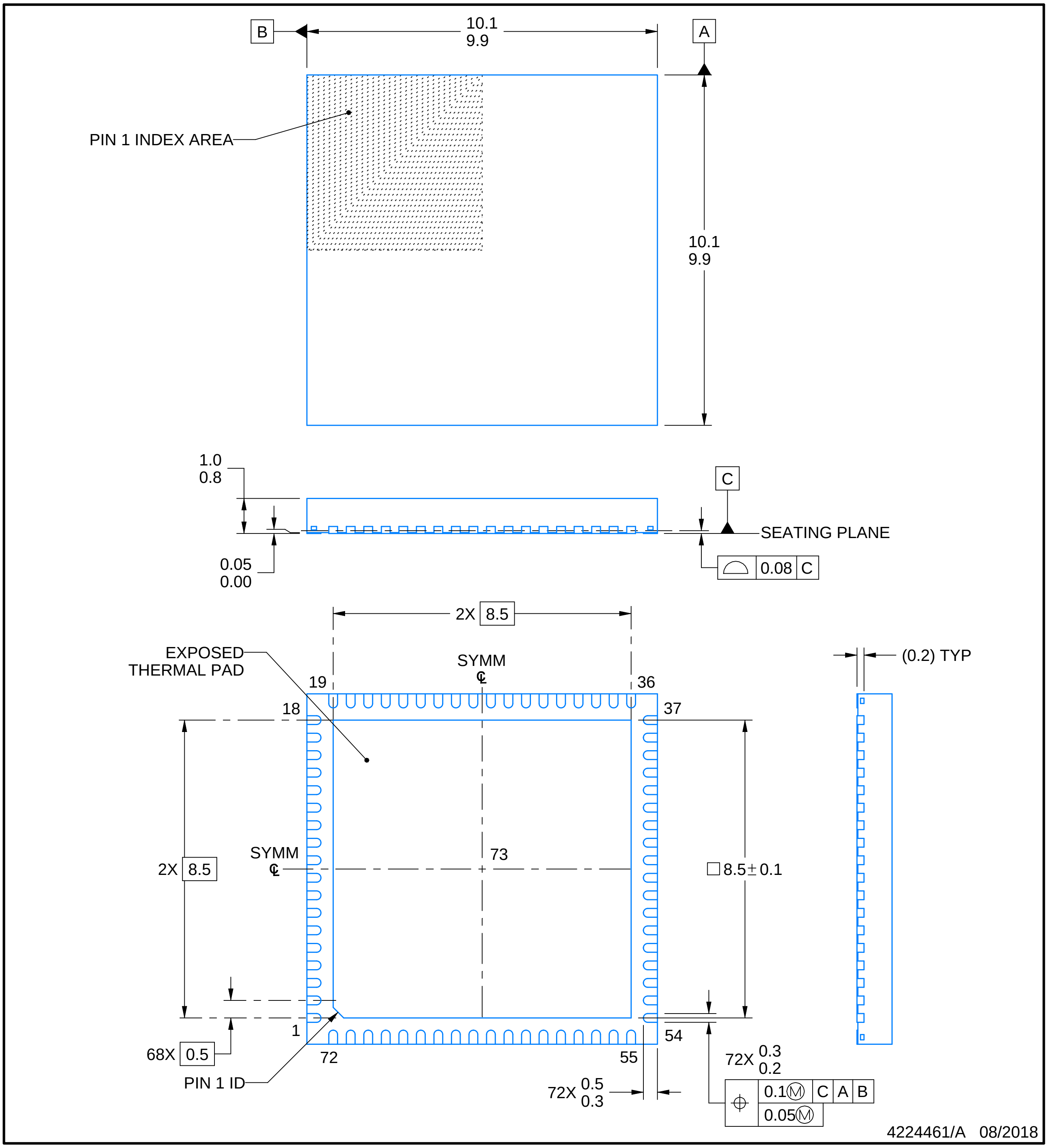
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

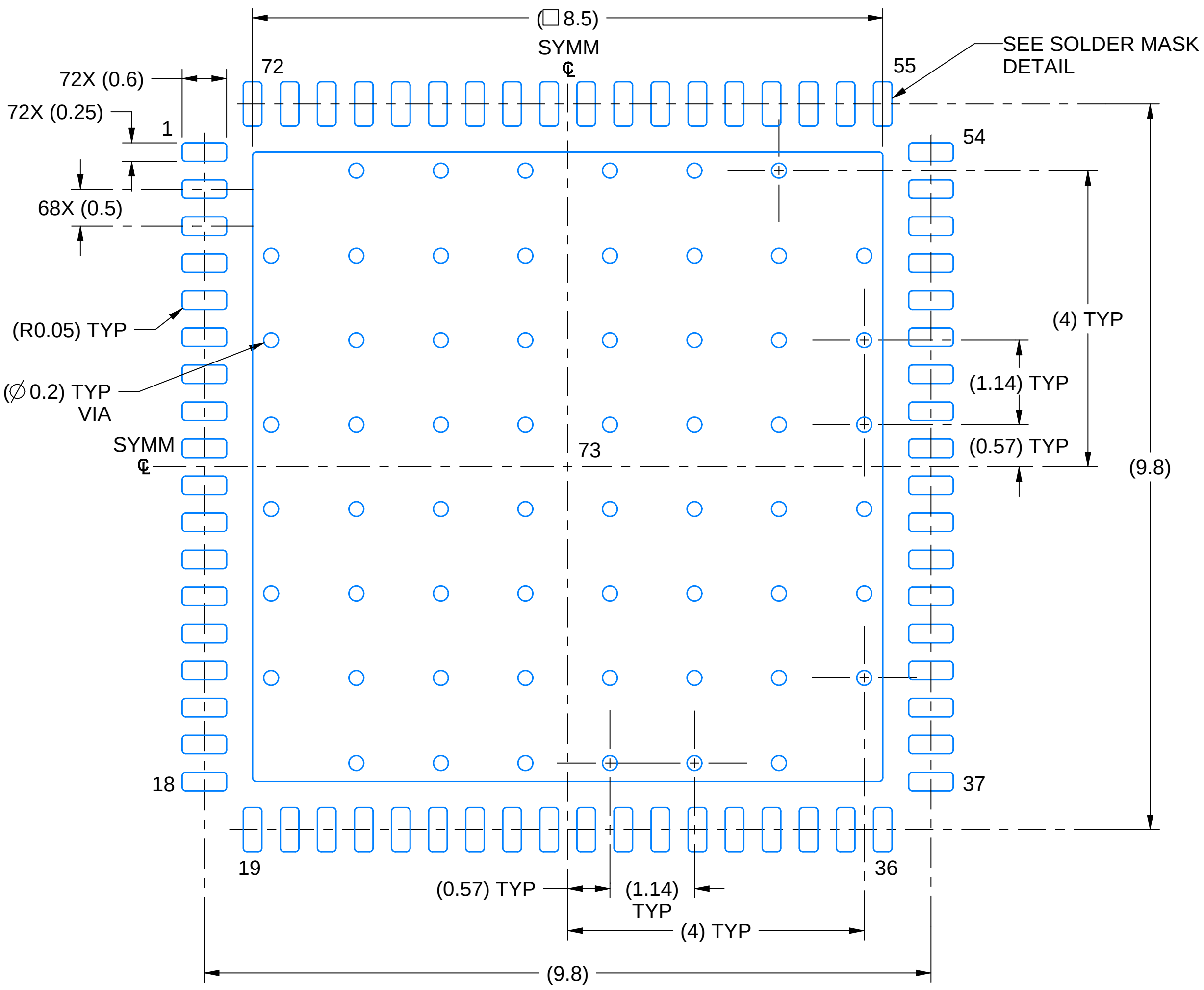
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

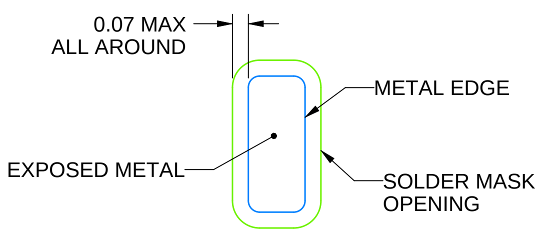


NOTES:

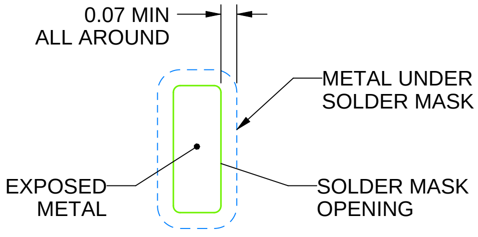
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON SOLDER MASK
DEFINED
(PREFERRED)



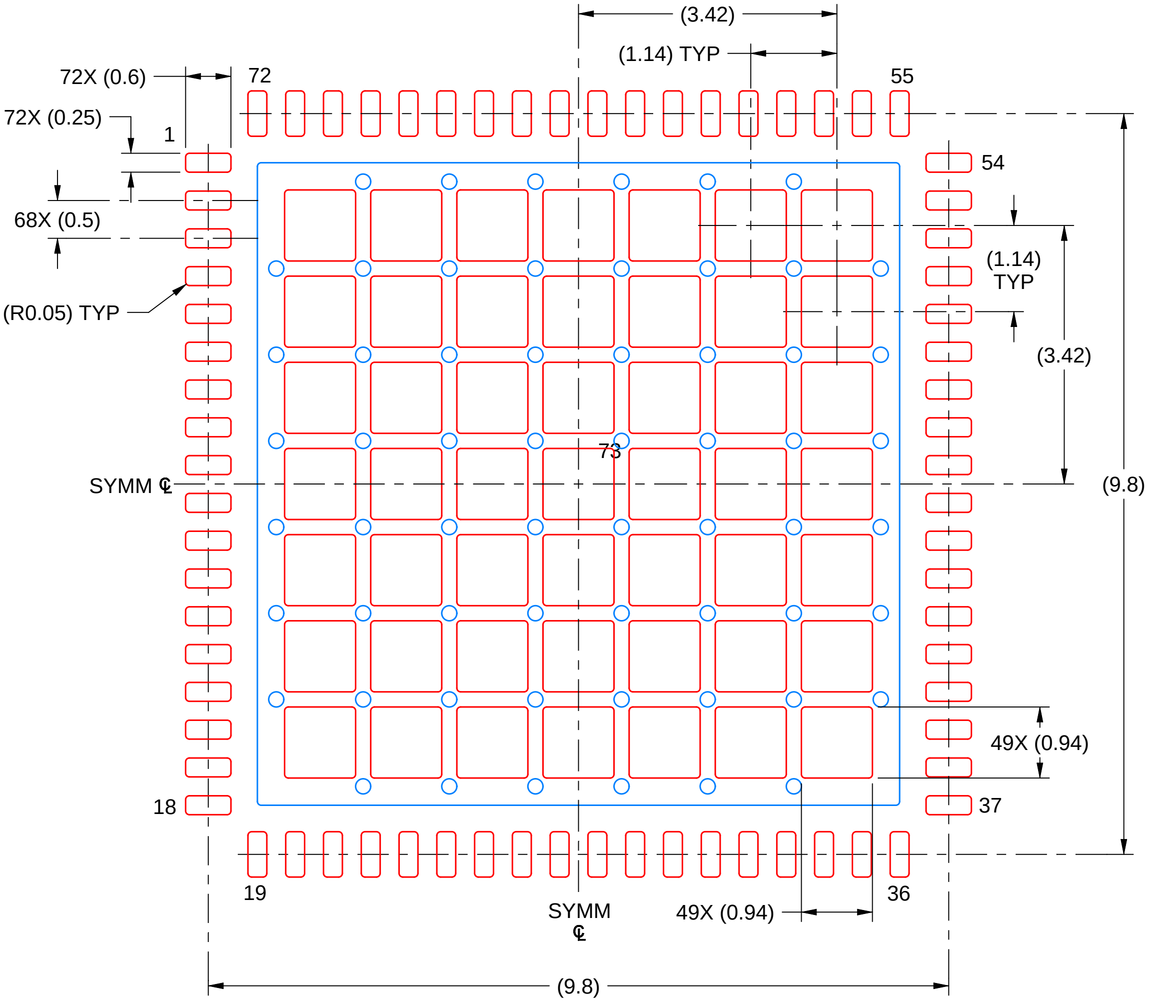
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224461/A 08/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 73
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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