

Product Datasheet

FTL410QE2C-C

Finisar® Compatible 40Gb/s QSFP SR4 QSFP Transceiver

Hot Pluggable, MTP/MPO Connector, +3.3V, MMF 150M DDM 0~70C

FEATURES

- 4 independent full-duplex channels
- Up to 11.2Gbps per channel bandwidth
- Aggregate bandwidth of > 40Gbps
- MTP/MPO optical connector
- QSFP MSA compliant
- Digital diagnostic capabilities
- CML compatible electrical I/O
- Single +3.3V power supply operating
- TX input and RX output CDR retiming
- Built-in digital diagnostic functions
- Temperature range 0°C to 70°C
- RoHS Compliant Part

APPLICATIONS

- Rack to rack
- Data Centre
- Metro networks
- Switches and Routers
- Infini band 4x SDR, DDR, QDR

DESCRIPTION

ATGBICS® FTL410QE2C-C is a parallel 40Gbps Quad Small Form-factor Pluggable (QSFP) optical module that provides increased port density and total system cost savings. The QSFP full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gbps operation for an aggregate bandwidth of 40Gbps 70m on OM3 Multimode Fiber (MMF) and 150m on OM4 MMF.

An optical fiber ribbon cable with an MPO/MTP connector at each end plugs into the QSFP module receptacle. The orientation of the ribbon cable is “keyed” and guide pins are present inside the module’s receptacle to ensure proper alignment. The cable usually has no twist (key up to key up) to ensure proper channel to channel alignment. Electrical connection is achieved through a z-pluggable 38-pin IPASS® connector.

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The module operates from a single +3.3V power supply and LVCMOS/LVTTL global control signals such as Module Present, Reset, Interrupt and Low Power Mode are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals and to obtain digital diagnostic information. Individual channels can be addressed, and unused channels can be shut down for maximum design flexibility.

The FTL410QE2C-C is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Typical | Max. | Unit |
|---------------------|---------------------|------|---------|------|------|
| Storage Temperature | T _s | -40 | | +85 | °C |
| Supply Voltage | V _{CC,T,R} | -0.5 | | 4 | V |
| Relative Humidity | RH | 0 | | 85 | % |

Recommended Operating Environment

| Parameter | Symbol | Min. | Typical | Max. | Unit |
|-----------------------------------|---------------------|-------|---------|-------|------|
| Case operating Temperature | T _C | 0 | | +70 | °C |
| Supply Voltage | V _{CC,T,R} | +3.13 | 3.3 | +3.47 | V |
| Supply Current | I _{CC} | | | 1000 | mA |
| Power Dissipation | PD | | | 3.5 | W |

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Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------------------|-----------------|-----|---------|-----------------|------|------|
| Data Rate per Channel | | - | 10.3125 | 11.2 | Gbps | |
| Power Consumption | | - | 2.5 | 3.5 | W | |
| Supply Current | I _{cc} | | 0.75 | 1.0 | A | |
| Control I/O Voltage-High | V _{IH} | 2.0 | | V _{cc} | V | |
| Control I/O Voltage-Low | V _{IL} | 0 | | 0.7 | V | |
| Inter-Channel Skew | TSK | | | 150 | Ps | |
| RESETL Duration | | | 10 | | Us | |
| RESETL De-assert time | | | | 100 | ms | |
| Power On Time | | | | 100 | ms | |
| Transmitter | | | | | | |
| Single Ended Output Voltage Tolerance | | 0.3 | | 4 | V | 1 |
| Common mode Voltage Tolerance | | 15 | | | mV | |
| Transmit Input Diff Voltage | V _I | 120 | | 1200 | mV | |
| Transmit Input Diff Impedance | Z _{IN} | 80 | 100 | 120 | | |
| Data Dependent Input Jitter | DDJ | | | 0.1 | UI | |
| Data Input Total Jitter | T _J | | | 0.28 | UI | |
| Receiver | | | | | | |
| Single Ended Output Voltage Tolerance | | 0.3 | | 4 | V | |
| Rx Output Diff Voltage | V _o | | 600 | 800 | mV | |
| Rx Output Rise and Fall Voltage | Tr/Tf | | | 35 | ps | 1 |
| Total Jitter | T _J | | | 0.7 | UI | |
| Deterministic Jitter | DJ | | | 0.42 | UI | |

Note:

1. 20 – 80 %

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Optical Parameters

| Parameter | Symbol | Min | Typ | Max | Unit | Ref. |
|-----------------------------------|------------------|------|------|------|-------|------|
| Transmitter | | | | | | |
| Optical Wavelength | λ | 840 | | 860 | nm | |
| RMS Spectral Width | P _m | | 0.5 | 0.65 | nm | |
| Average Optical Power per Channel | P _{avg} | -8 | -2.5 | +1.0 | dBm | |
| Laser Off Power Per Channel | P _{off} | | | -30 | dBm | |
| Optical Extinction Ratio | ER | 3.5 | | | dB | |
| Relative Intensity Noise | R _{in} | | | -128 | dB/HZ | 1 |
| Optical Return Loss Tolerance | | | | 12 | dB | |
| Receiver | | | | | | |
| Optical Center Wavelength | λ_c | 840 | | 860 | nm | |
| Receiver Sensitivity per Channel | R | | -13 | | dBm | |
| Maximum Input Power | P _{MAX} | +0.5 | | | dBm | |
| Receiver Reflectance | R _{RX} | | | -12 | dB | |
| LOS De-Assert | LOS _D | | | -14 | dBm | |
| LOS Assert | LOS _A | -30 | | | dBm | |
| LOS Hysteresis | LOS _H | 0.5 | | | dB | |

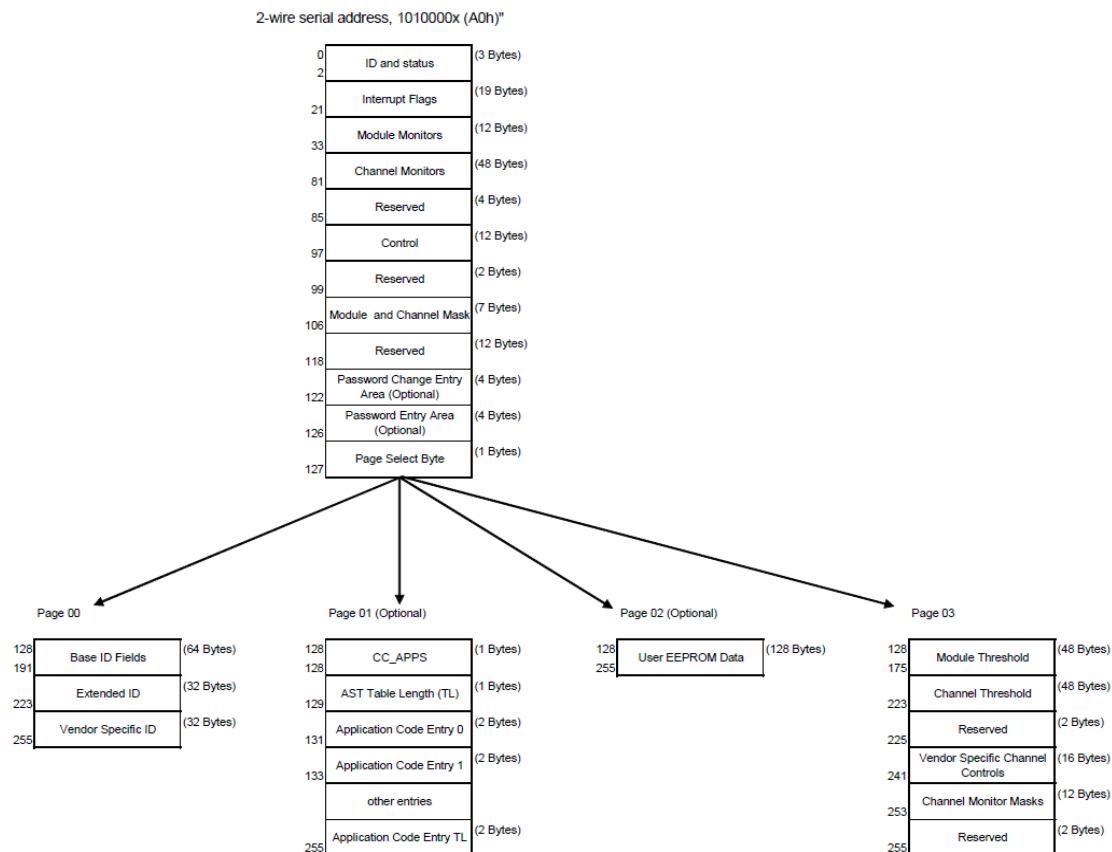
Note:

- 12dB Reflection

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Diagnostic Monitoring Interface

Digital diagnostics monitoring function is available on all QSFP+ SR4. A 2-wire serial interface provides user to contact with module. The structure of the memory is shown in flowing. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.



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Lower Memory Map

| Byte Address | Description | Type |
|--------------|---|------------|
| 0 | Identifier (1 Byte) | Read-Only |
| 1-2 | Status (2 Bytes) | Read-Only |
| 3-21 | Interrupt Flags (19 Bytes) | Read-Only |
| 22-33 | Module Monitors (12 Bytes) | Read-Only |
| 34-81 | Channel Monitors (48 Bytes) | Read-Only |
| 82-85 | Reserved (4 Bytes) | Read-Only |
| 86-97 | Control (12 Bytes) | Read/Write |
| 98-99 | Reserved (2 Bytes) | Read/Write |
| 100-106 | Module and Channel Masks (7 Bytes) | Read/Write |
| 107-118 | Reserved (12 Bytes) | Read/Write |
| 119-122 | Password Change Entry Area (optional) (4 Bytes) | Read/Write |
| 123-126 | Password Entry Area (optional) (4 Bytes) | Read/Write |
| 127 | Page Select Byte | Read/Write |

Upper Memory Map

| Byte Address | Description | Type |
|--------------|---|------------|
| 128-175 | Module Thresholds (48 Bytes) | Read-Only |
| 176-223 | Channel Thresholds (48 Bytes) | Read-Only |
| 224-225 | Reserved (2 Bytes) | Read-Only |
| 226-239 | Vendor Specific Channel Controls (14 Bytes) | Read/Write |
| 240-241 | Optional Channel Controls (2 Bytes) | Read/Write |
| 242-253 | Channel Monitor Masks (12 Bytes) | Read/Write |
| 254-255 | Reserved (2 Bytes) | Read/Write |

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Serial ID: Data Fields

| Address | Size (Bytes) | Name | Description of Base ID Field |
|----------------------------------|--------------|--------------------------------|--|
| Base_ID Fields | | | |
| 128 | 1 | Identifier | Identifier Type of serial transceiver |
| 129 | 1 | Ext. Identifier | Extended identifier of serial transceiver |
| 130 | 1 | Connector | Code for connector type |
| 131-138 | 8 | Transceiver | Code for electronic compatibility or optical compatibility |
| 139 | 1 | Encoding | Code for serial encoding algorithm |
| 140 | 1 | BR, nominal | Nominal bit rate, units of 100 Mbits/s. |
| 141 | 1 | Extended RateSelect Compliance | Tags for Extended RateSelect compliance |
| 142 | 1 | Length(SMF) | Link length supported for SMF fiber in km |
| 143 | 1 | Length (E-50µm) | Link length supported for EBW 50/125 µm fiber, units of 2 m |
| 144 | 1 | Length (50 µm) | Link length supported for 50/125 µm fiber, units of 1 m |
| 145 | 1 | Length (62.5 µm) | Link length supported for 62.5/125 µm fiber, units of 1 m |
| 146 | 1 | Length Copper | Link length supported for copper, units of 1m |
| 147 | 1 | Device Tech | Device technology |
| 148-163 | 16 | Vendor name | ATGBICS |
| 164 | 1 | Extended | Extended Transceiver Codes for InfiniBand |
| 165-167 | 3 | Vendor OUI | QSFP vendor IEEE company ID |
| 168-183 | 16 | Vendor PN | FTL410QE2C-C |
| 184-185 | 2 | Vendor rev | Revision level for part number provided by vendor (ASCII) |
| 186-187 | 2 | Wavelength | Nominal laser wavelength (Wavelength = value / 20 in nm) |
| 188-189 | 2 | Wavelength Tolerance | Guaranteed range of laser wavelength (+/- value) from Nominal wavelength.(Wavelength Tol. = value/200 in nm) |
| 190 | 1 | Max Case Temp | Maximum Case Temperature in Degrees C. |
| 191 | 1 | CC_BASE | Check code for Base ID Fields (addresses 128-190) |
| Extended ID Fields | | | |
| 192-195 | 4 | Options | Rate Select, TX Disable, TX Fault, LOS |
| 196-211 | 16 | Vendor SN | Serial number provided by vendor (ASCII) |
| 212-219 | 8 | Date code | Vendor's manufacturing date code |
| 220 | 1 | Diagnostic Monitoring Type | Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver. Bit 1, 0 Reserved |
| 221 | 1 | Enhanced Options | Indicates which optional enhanced features are implemented in |
| 222 | 1 | Reserved | Reserved |
| 223 | 1 | CC_EXT | Check code for the Extended ID Fields (addresses 192- |
| Vendor Specific ID Fields | | | |
| 224-255 | 32 | Vendor Specific | Vendor Specific EEPROM |

The detail description of low memory and page00.page03 upper memory please see SFF-8436 document.

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Timing for Soft Control and Status Functions

| Parameter | Symbol | Max | Unit | Conditions |
|--------------------------------|--------------|------|------|--|
| Initialization Time | t_init | 2000 | ms | Time from power on ¹ , hot plug or rising edge of Reset until the module is fully functional ² |
| Reset Init Assert Time | t_reset_init | 2 | µs | A Reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin. |
| Serial Bus Hardware Ready Time | t_serial | 2000 | ms | Time from power on ¹ until module responds to data transmission over the 2-wire serial bus |
| Monitor Data Ready Time | t_data | 2000 | ms | Time from power on ¹ to data not ready, bit 0 of Byte 2, deasserted and IntL asserted |
| Reset Assert Time | t_reset | 2000 | ms | Time from rising edge on the ResetL pin until the module is fully functional ² |
| LPMODE Assert Time | ton_LPMODE | 100 | µs | Time from assertion of LPMODE (Vin:LPMODE =Vih) until module power consumption enters lower Power Level |
| IntL Assert Time | ton_IntL | 200 | ms | Time from occurrence of condition triggering IntL until Vout:IntL = Vol |
| IntL Deassert Time | toff_IntL | 500 | µs | toff_IntL 500 µs Time from clear on read ³ operation of associated flag until Vout:IntL = Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits. |
| Rx LOS Assert Time | ton_los | 100 | ms | Time from Rx LOS state to Rx LOS bit set and IntL asserted |
| Flag Assert Time | ton_flag | 200 | ms | Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted |
| Mask Assert Time | ton_mask | 100 | ms | Time from mask bit set ⁴ until associated IntL assertion is inhibited |
| Mask De-assert Time | toff_mask | 100 | ms | Time from mask bit cleared ⁴ until associated IntL operation resumes |
| ModSelL Assert Time | ton_ModSelL | 100 | µs | Time from assertion of ModSelL until module responds to data transmission over the 2-wire serial bus |
| ModSelL Deassert Time | toff_ModSelL | 100 | µs | Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus |
| Power_over-ride or | ton_Pdown | 100 | ms | Time from P_Down bit set 4 until module power |

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| | | | | |
|---|------------|-----|----|---|
| Power-set Assert Time | | | | consumption enters lower Power Level |
| Power-over-ride or Power-set De-assert Time | toff_Pdown | 300 | ms | Time from P_Down bit cleared ⁴ until the module is fully functional ³ |

Notes :

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

● Transceiver Block Diagram

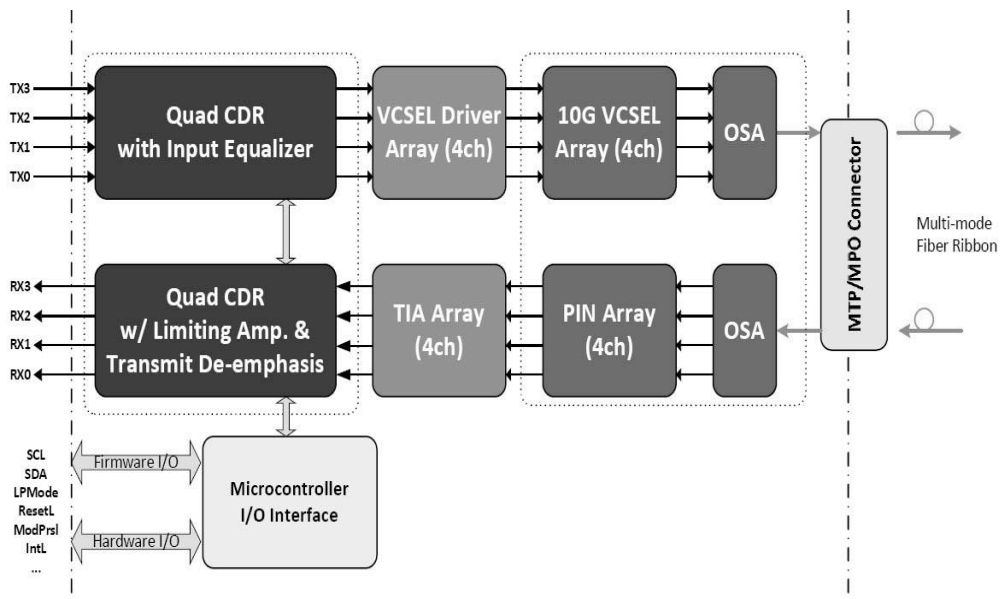


Figure1: Block Diagram

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Pin Assignment

Diagram of Host Board Connector Block Pin Numbers and Name

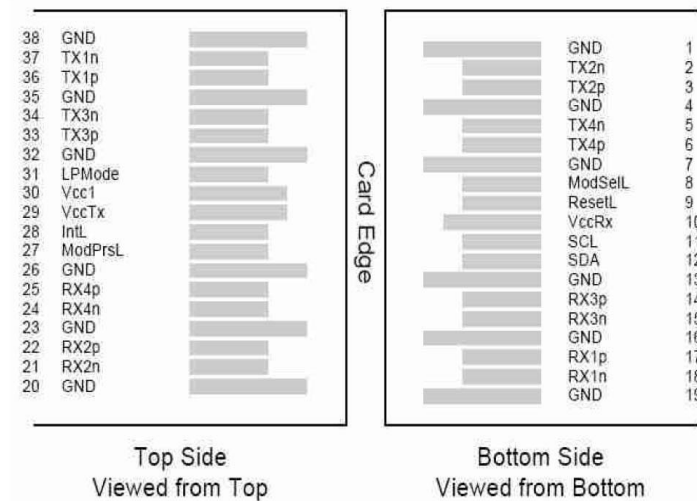


Diagram of Host Board Connector Block Pin Numbers and Names

Pin Function Definitions

| Pin | Logic | Symbol | Name/Description | Ref. |
|-----|---------|---------|--------------------------------------|------|
| 1 | | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data output | |
| 4 | | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Output | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Output | |
| 7 | | GND | Ground | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | |
| 9 | LVTTL-I | ResetL | Module Reset | |
| 10 | | VCCRx | +3.3V Power Supply Receiver | 2 |

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| | | | | |
|----|------------|---------|-----------------------------------|---|
| 11 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock | |
| 12 | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data | |
| 13 | | GND | Ground | 1 |
| 14 | CML-O | Rx3p | Receiver Inverted Data Output | |
| 15 | CML-O | Rx3n | Receiver Non-Inverted Data Output | |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Inverted Data Output | |
| 18 | CML-O | Rx1n | Receiver Non-Inverted Data Output | |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | | GND | Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | |
| 28 | LVTTL-O | IntL | Interrupt | |
| 29 | | VccTx | +3.3V Power Supply Transmitter | 2 |
| 30 | | Vcc1 | +3.3V Power Supply | 2 |

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| | | | | |
|-----------|----------|--------|--------------------------------------|---|
| 31 | LVTTTL-I | LPMODE | Low Power Mode | |
| 32 | | GND | Ground | 1 |
| 33 | CML-I | Tx3p | Transmitter Inverted Data Output | |
| 34 | CML-I | Tx3n | Transmitter Non-Inverted Data Output | |
| 35 | | GND | Ground | 1 |
| 36 | CML-I | Tx1p | Transmitter Inverted Data Output | |
| 37 | CML-I | Tx1n | Transmitter Non-Inverted Data Output | |
| 38 | | GND | Ground | 1 |

Notes:

1. GND is the symbol for single and supply(power) common for QSFP modules, All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane. Laser output disabled on TDIS >2.0V or open, enabled on TDIS <0.8V.
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. VccRx, Vcc1 and VccTx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for maximum current of 500mA.

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Optical Interface Lanes and Assignment

Below figure shows the orientation of the multi-mode fiber facets of the optical connector



Outside View of the QSFP Module MPO

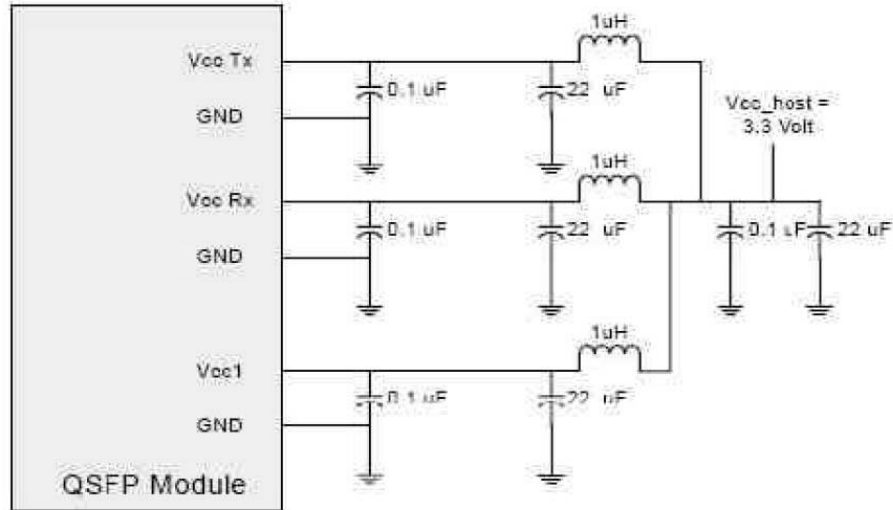
| Fiber No. | Lane Assignment |
|-----------|-----------------|
| 1 | RX0 |
| 2 | RX1 |
| 3 | RX2 |
| 4 | RX3 |
| 5 | Not Used |
| 6 | Not Used |

Lane Assignment Table



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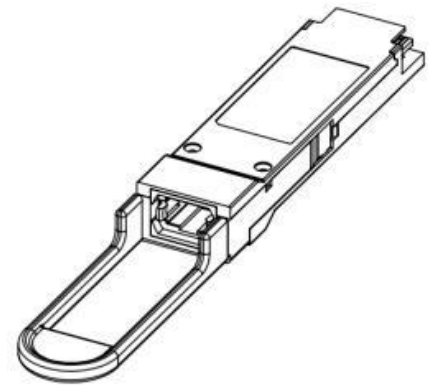
Recommended Circuit



QSF Host Recommended Circuit

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Mechanical Dimensions



TOLERANCES: $\pm 0.10\text{mm}$