

IS32LT3174

SINGLE CHANNEL, LINEAR LED DRIVER WITH FADE IN/FADE OUT

August 2022

GENERAL DESCRIPTION

The IS32LT3174 is a linear programmable current regulator consisting of one output channel capable of up to 200mA. It features an ON/OFF input pin to toggle the channel between the OFF condition and the source condition.

A single external resistor programs the current level for the channel, while a separate, single resistor programs the fade in and fade out rate for channel.

The device integrates a 63 steps fade in and fade out algorithm (Gamma correction) which causes the output LED current to gradually ramp up to the full source value after the channel's control pin is pulsed. The same controller causes the LED current to gradually ramp down to zero if the channel's input control pin is pulsed while the output channel is on. The LED current output can be controlled by a momentary contact switch or logic level signal.

The IS32LT3174 is targeted at the automotive market with end applications to include map and dome lighting as well as exterior accent lighting. For 12V automotive applications the low dropout driver can support 1 to 3 LEDs per channel. It is offered in a small thermally enhanced SOP-8-EP package.

FEATURES

- Output current can source up to 200mA
- On/off control for channel
 - Input is debounced
- Programmable current via a single external resistor
- Programmable fade in, fade out via external resistor
 - Pull down resistor value sets fade speed
 - Gamma corrected fade in/out algorithm
- Fault Protection:
 - LED string shorted to GND
 - ISET pin short to GND
 - Over temperature
- SOP-8-EP package
- Automotive Grade - AEC-Q100
- Operating temperature range from -40°C ~ +125°C
- RoHS & Halogen-Free compliant (Pb-free) package

APPLICATIONS

- Automotive Interior:
 - Map light
 - Dome lighting
 - Puddle lamp in doors
 - Glove box
 - Vanity mirror

TYPICAL APPLICATION CIRCUIT

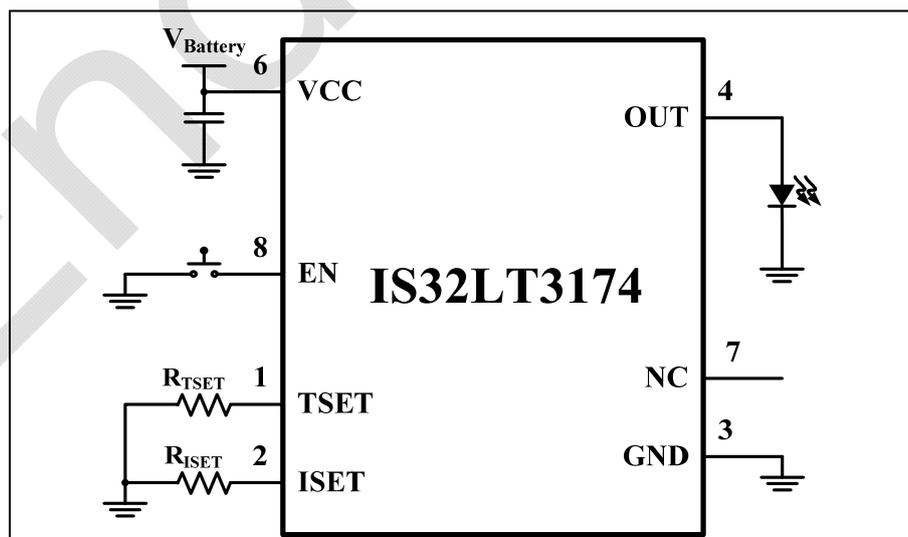
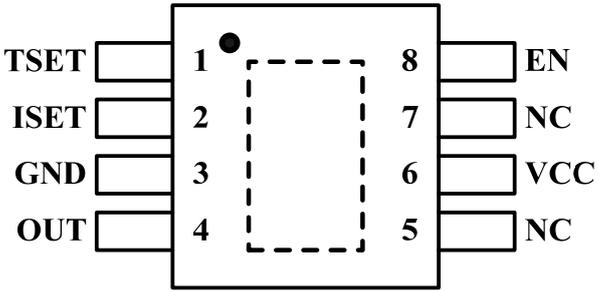


Figure 1 Typical Application Circuit

Note: The switches on EN pin should be momentary touch type.

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PIN CONFIGURATION

Package	Pin Configuration (Top view)
SOP-8-EP	 <p> TSET [] 1 [] 8 [] EN ISET [] 2 [] 7 [] NC GND [] 3 [] 6 [] VCC OUT [] 4 [] 5 [] NC </p>

PIN DESCRIPTION

No.	Pin	Description
1	TSET	Timing control for the fade in and fade out feature. Connect a resistor between this pin and GND to set the fade in and fade out time. Connect this pin directly to ground to disable the fade function for instant on/off.
2	ISET	Output current setting. Connect a resistor between this pin and GND to set the maximum output current.
3	GND	Ground pin for the device.
4	OUT	Output current source channel.
5	NC	Not connect.
6	VCC	Power supply input pin.
7	NC	Not connect. It must be floating when the IC operates.
8	EN	Internally debounced input pin for control of channel. Momentary contact will toggle the state of the OUT LED. Fade in or out function can be interrupted by EN pin state change after debounce period.
	Thermal Pad	Connect to GND.

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ORDERING INFORMATION
AUTOMOTIVE RANGE: -40°C TO +125°C

Order Part No.	Package	QTY/Reel
IS32LT3174-GRLA3-TR	SOP-8-EP, Lead-free	2500

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- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

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ABSOLUTE MAXIMUM RATINGS

VCC, OUT	-0.3V ~ +50V
EN, ISET, TSET	-0.3V ~ +7.0V
Ambient operating temperature, $T_A = T_J$	-40°C ~ +125°C
Maximum continuous junction temperature, $T_{J(MAX)}$	150°C
Storage temperature range, T_{STG}	-55°C ~ +150°C
Maximum power dissipation, P_{DMAX} (Note 2)	1.96W
ESD (HBM)	±2kV
ESD (CDM)	±750V

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Detail information please refers to package thermal de-rating curve on Page 12.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions	Value
Package Thermal Resistance (Junction to Ambient), $R_{\theta JA}$	On 4-layer PCB based on JEDEC standard at 1W, $T_A=25^\circ\text{C}$	50.98°C/W
Package Thermal Resistance (Junction to Pad), $R_{\theta JP}$		2.24°C/W

ELECTRICAL CHARACTERISTICS

$T_J = -40^\circ\text{C} \sim +125^\circ\text{C}$, $V_{CC}=12\text{V}$, the detail refers to each condition description. Typical values are at $T_J = 25^\circ\text{C}$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage range		6		45	V
V_{DO}	Minimum dropout voltage	$V_{CC} - V_{OUT}$, $I_{OUT} = -200\text{mA}$ (Note1)			900	mV
		$V_{CC} - V_{OUT}$, $I_{OUT} = -100\text{mA}$ (Note1)			700	mV
I_{CC}	Quiescent supply current	OUT is shutdown	0.1		1	mA
		$I_{SET}=20\text{k}\Omega$, enable. OUT connects to VCC		3.6		mA
t_{ON}	Startup time	$V_{CC} > 6\text{V}$ to $I_{OUT} < -5\text{mA}$ (Note 3)			400	μs
I_{OUT_LIM}	Output limit current	$V_{CC} - V_{OUT} = 1\text{V}$, OUT sourcing current, $V_{ISET} = 0\text{V}$	-310	-240	-205	mA
I_{OUT}	Output current (Note 2)	$I_{SET} = 20\text{k}\Omega$, $V_{CC} - V_{OUT} = 1\text{V}$, $T_J = 25^\circ\text{C}$	-103	-100	-97	mA
		$I_{SET} = 20\text{k}\Omega$, $V_{CC} - V_{OUT} = 1\text{V}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$	-105	-100	-95	
$E_{I_{OUT}}$	Absolute current accuracy (Note 2)	$-50\text{mA} \leq I_{OUT} < -20\text{mA}$, $V_{CC} - V_{OUT} = 1\text{V}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$	-8		8	%
		$-200\text{mA} < I_{OUT} < -50\text{mA}$, $V_{CC} - V_{OUT} = 1\text{V}$, $-40^\circ\text{C} < T_J < +125^\circ\text{C}$	-6		6	%
g_{LINE}	Output current line regulation	$I_{OUT} = -50\text{mA}$, $6\text{V} < V_{CC} < 18\text{V}$, $V_{OUT} = V_{CC} - 2\text{V}$ (Note 3)	-0.2		0.2	mA/V
g_{LOAD}	Output current load regulation	$2.5\text{V} < V_{OUT} < V_{CC} - 2.0\text{V}$, $I_{OUT} = -50\text{mA}$ (Note 3)	-0.2		0.2	mA/V
t_{SL}	Current slew time	Current rise/fall between 0%~100% $V_{TSET} = 0\text{V}$	45	70	100	μs

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ELECTRICAL CHARACTERISTICS (CONTINUE)

$T_J = -40^{\circ}\text{C} \sim +125^{\circ}\text{C}$, $V_{CC}=12\text{V}$, the detail refers to each condition description. Typical values are at $T_J = 25^{\circ}\text{C}$.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Logic Input TSET						
V_{TSET}	Voltage reference			1		V
T_{ACC}	Fade timing accuracy	*Neglecting the R_{TSET} Tolerance* $R_{TSET}=100\text{k}\Omega$, $T_J = 25^{\circ}\text{C}$	-5		5	%
Logic Input EN						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2			V
V_{IN_HY}	Input hysteresis	(Note 3)	150	350		mV
R_{PU}	Pull-up resistor	(Note 3)		50		$\text{k}\Omega$
I_{PU}	Pull-up current			75		μA
t_{SW}	EN input debounce time	EN pin must not change state within this time to be interpreted as a switch press or release	25	37	50	ms
Protection						
V_{SCD}	Short detect voltage	Measured at OUT	1.2		1.8	V
V_{SC_HY}	Short detect voltage hysteresis	$V_{SCR} - V_{SCD}$ (Note 3)		220		mV
t_{FD}	Fault detect persistence time	(Note 3)		5		ms
T_{RO}	Thermal roll off threshold	(Note 3)		130		$^{\circ}\text{C}$
T_{SD}	Thermal shutdown threshold	Temperature increasing (Note 3)		155		$^{\circ}\text{C}$
T_{HY}	Over temperature hysteresis	(Note 3)		20		$^{\circ}\text{C}$

Note 1: I_{OUT} output current in case of $V_{CC}-V_{OUT}=V_{DO}$ called I_{OUT_VDO} . I_{OUT} output current in case of $V_{CC}-V_{OUT}=1\text{V}$ called I_{OUT_VDO1V} , V_{DO} accuracy is computed as $|I_{OUT_VDO}-I_{OUT_VDO1V}|/I_{OUT_VDO1V}<5\%$.

Note 2: Output current accuracy is not intended to be guaranteed at output voltages less than 1.8V.

Note 3: Guaranteed by design.

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TYPICAL PERFORMANCE CHARACTERISTICS

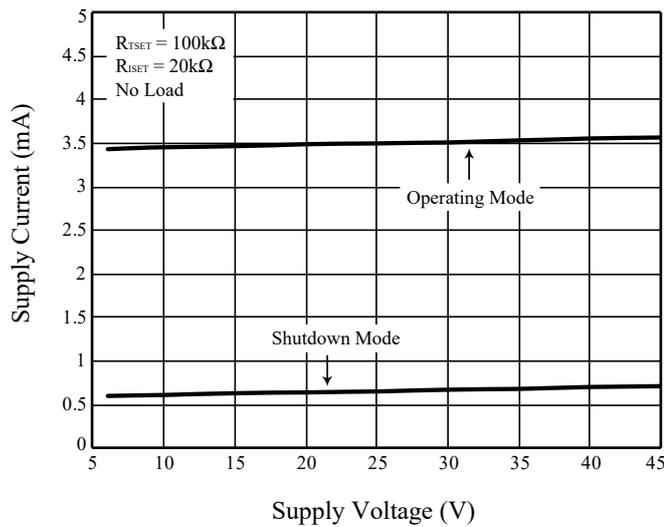


Figure 2 Supply Current vs. Supply Voltage

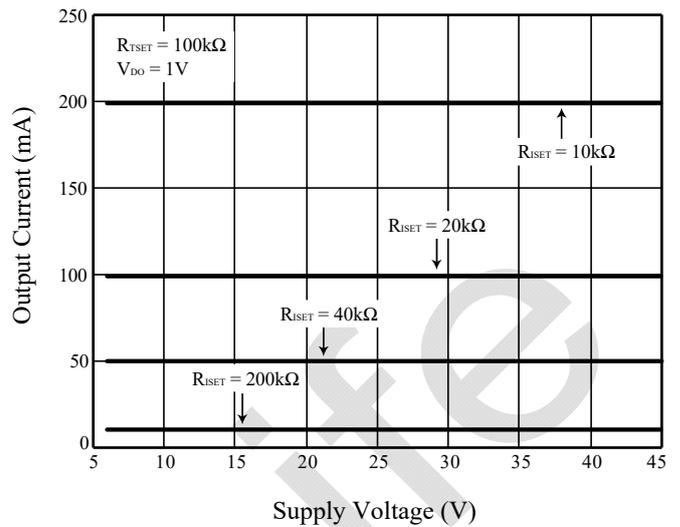


Figure 3 Output Current vs. Supply Voltage

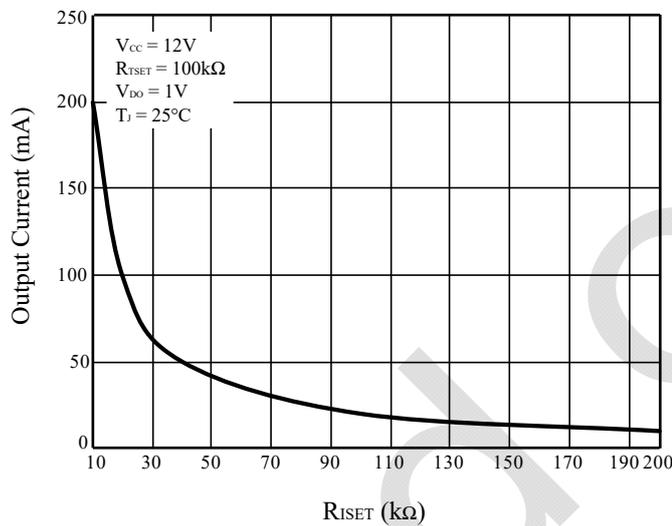


Figure 4 Output Current vs. R_{ISET}

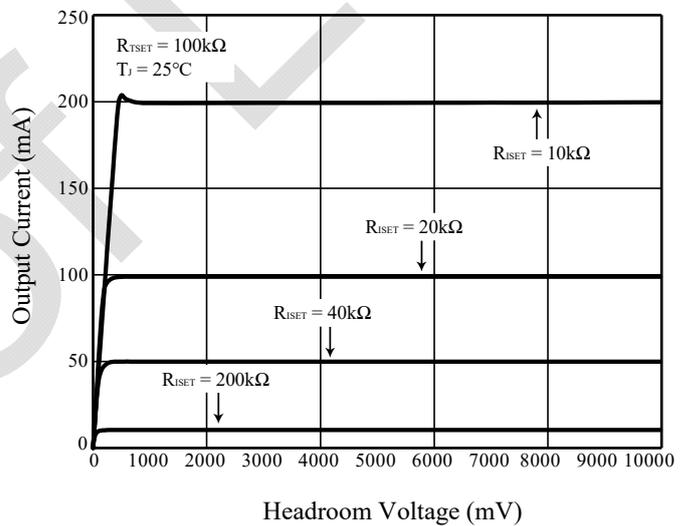


Figure 5 Output Current vs. Headroom Voltage

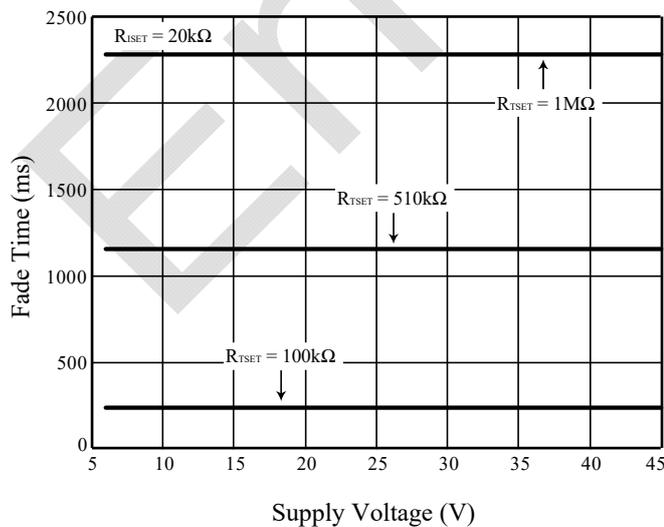


Figure 6 Fade Time vs. Supply Voltage

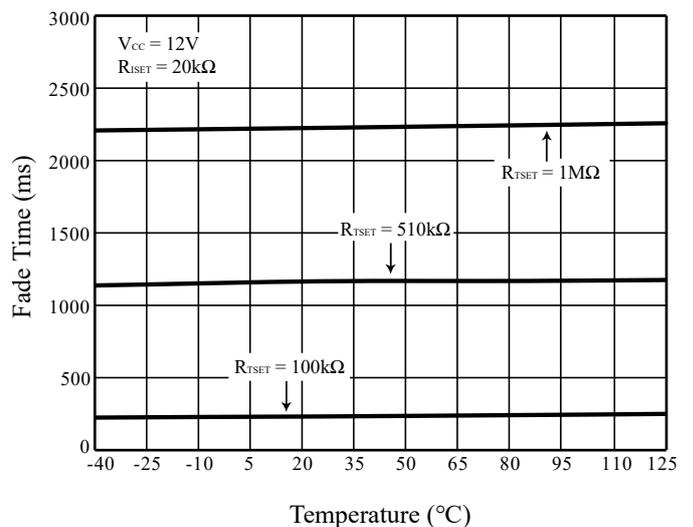


Figure 7 Fade Time vs. Temperature

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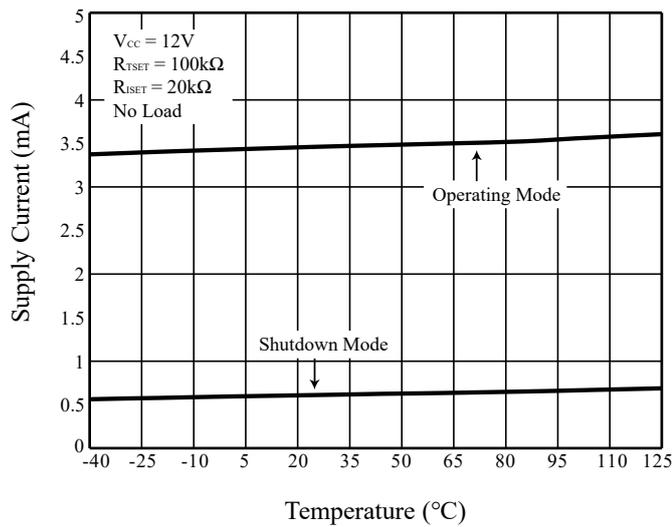


Figure 8 Supply Current vs. Temperature

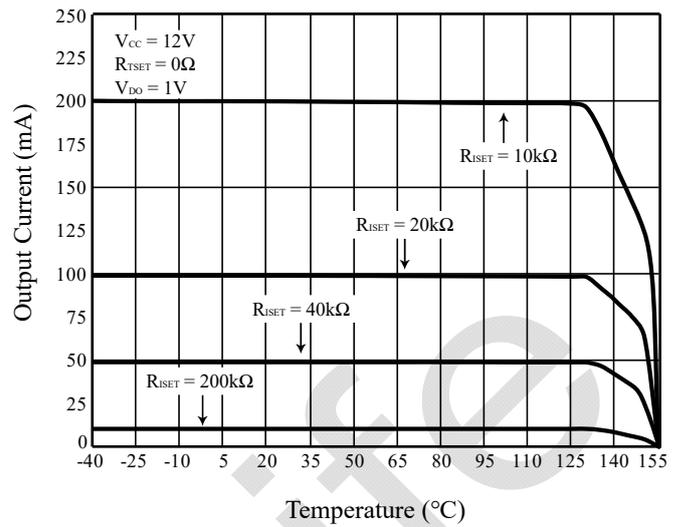


Figure 9 Output Current vs. Temperature

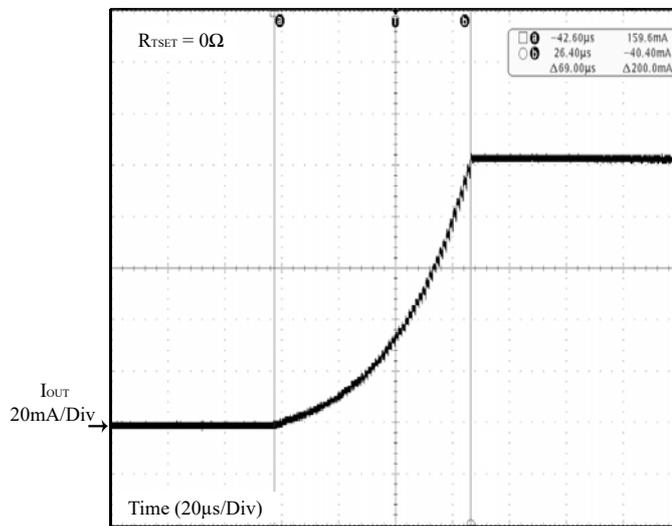


Figure 10 Instant on

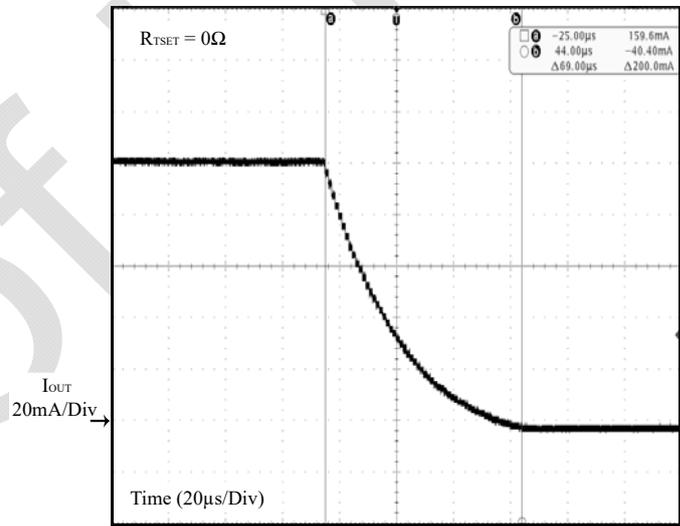


Figure 11 Instant Off

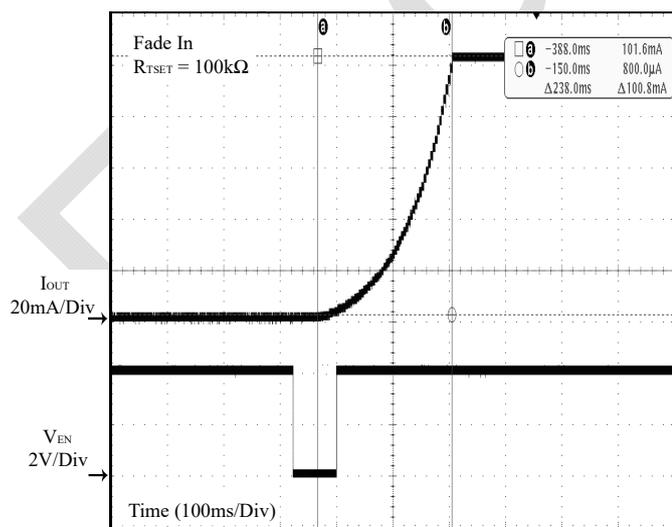


Figure 12 V_{EN} vs. I_{OUT}

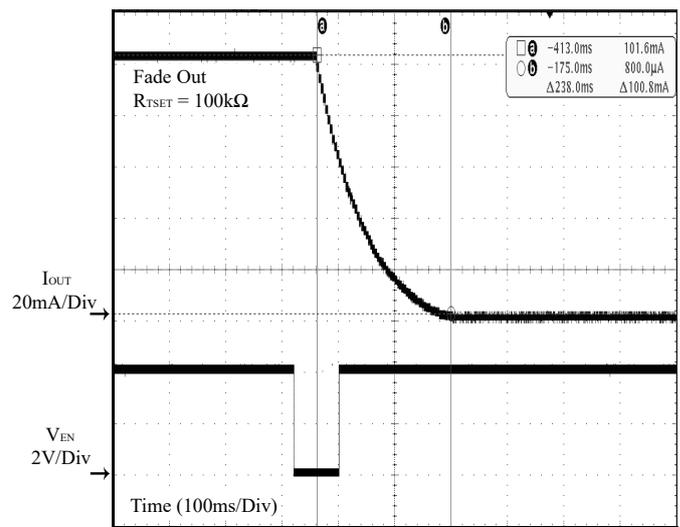


Figure 13 V_{EN} vs. I_{OUT}

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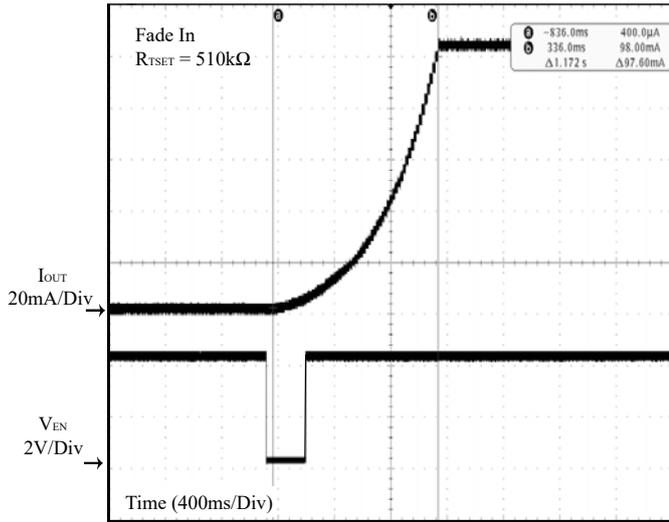


Figure 14 V_{EN} VS. I_{OUT}

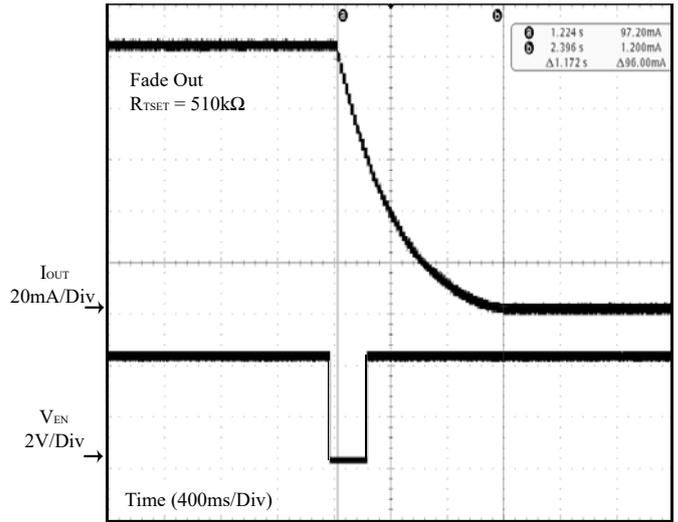


Figure 15 V_{EN} VS. I_{OUT}

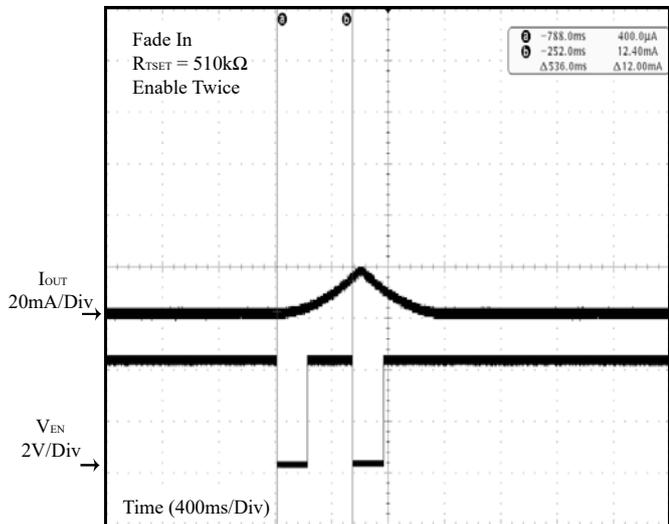


Figure 16 V_{EN} VS. I_{OUT}

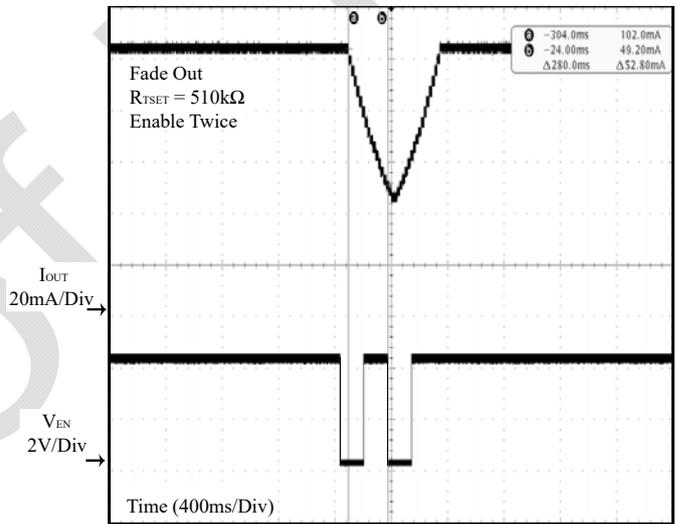
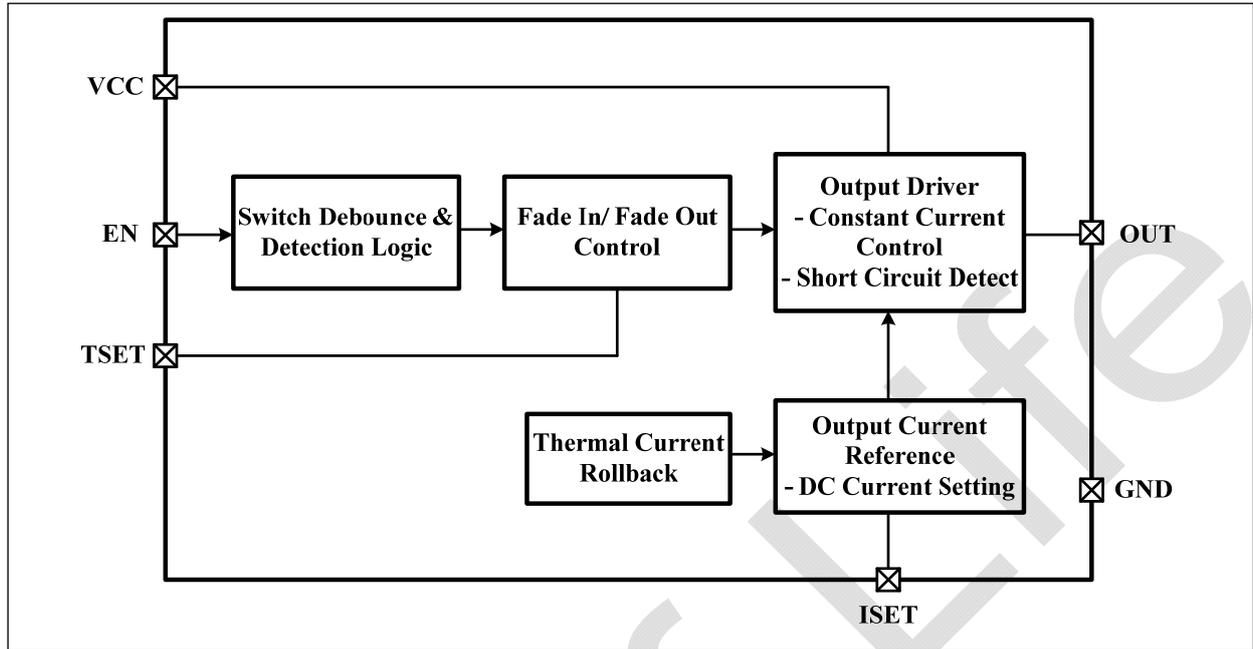


Figure 17 V_{EN} VS. I_{OUT}

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FUNCTIONAL BLOCK DIAGRAM



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APPLICATION INFORMATION

The IS32LT3174 is a single channel linear current driver optimized to drive an automotive interior map light, or other interior lamp which is frequently toggled between the on and off condition. The device integrates an input control for the channel allowing for on/off operation. In addition, a programmable fade in and fade out feature is integrated into channel's control block to allow the end customer maximum flexibility in setting up their light timing requirements.

The regulated LED current (up to 200mA) is set by a single reference resistor (R_{ISET}).

OUTPUT CURRENT SETTING

A single programming resistor (R_{ISET}) controls the maximum output current for output channel simultaneously. The programming resistor may be computed using the following Equation (1):

$$R_{ISET} = \frac{2000}{I_{SET}} \quad (1)$$

$$(10k\Omega \leq R_{ISET} \leq 100k\Omega)$$

The device is protected from an output overcurrent condition caused by an accidental short circuit of the ISET pin, by internally limiting the maximum current in the event of an ISET short circuit to 260mA.

EN PIN OPERATION

The EN inputs to the device include internal pull-up sources so that no external components are required to provide the input high level to the pin.

The output channel powers up in the 'OFF' condition. Toggling the EN pin from high to low on a given channel for a period of time that exceeds the debounce time will cause that channel's output to toggle from the OFF condition to the source condition. When this happens, the output current of the channel gradually ramps up from zero to the programmed value (set by R_{ISET}) over the time set by the resistor (R_{TSET}) attached to the ISET pin. Conversely, if a channel is already in the source condition, and that channel's EN pin is toggled low, then the output current shall begin to ramp down towards zero in the time period as programmed by the resistor (R_{TSET}) attached to the TSET pin.

Note, the EN input is available during the period of either fade in or fade out condition.

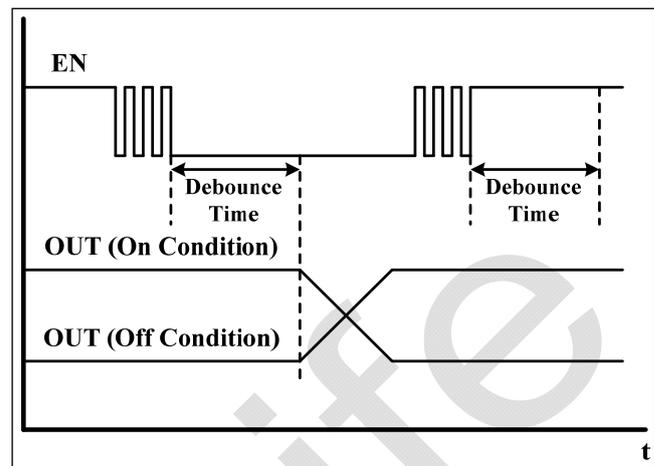


Figure 18 EN Debounced

Debounce - Output control is provided by a debounced switch input, providing an ON/OFF toggle action for various switch or button characteristics. An internal debounce circuit will condition the input signal so a single press of the mechanical switch doesn't appear like multiple presses. The EN input is debounced by typically 37ms.

Note: The debounce time applies to both falling and rising edges of the EN signal.

FADE IN AND FADE OUT

When an EN channel is turned on (pulled low), the output current of the channel shall gradually ramp up from zero to the final value as programmed by the resistor (R_{ISET}) connected to the ISET pin. The time period over which the ramping happens is determined by the resistor (R_{TSET}) connected to the TSET pin. The output current shall ramp up (or down) in 63 steps, with integrated gamma correction for an extremely linear ramping of the luminous output of the LED bulb.

SETTING THE FADE TIME

The fade time, either in or out, for channel is set by a single external programming resistor (R_{TSET}). The fade time is programmable by Equation (2):

$$t \approx R_{TSET} \times 2.5\mu s \quad (2)$$

For example, $R_{TSET}=100k\Omega$, fade time is about 0.25s.

Note: In order to get the optimized effect, the recommended fading time is between 1.5s ($R_{TSET}=600k\Omega$) and 0.25s ($R_{TSET}=100k\Omega$).

If the TSET pin is tied directly to GND, the fade in/out function is canceled and the ramp time is about 73 μs , or 'instant on'. However, the debounce feature of the EN pin is not disabled.

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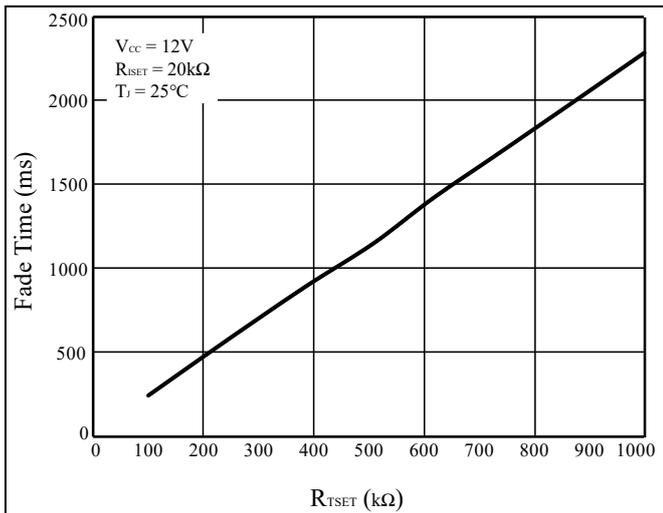


Figure 19 Fade Time vs. R_{TSET}

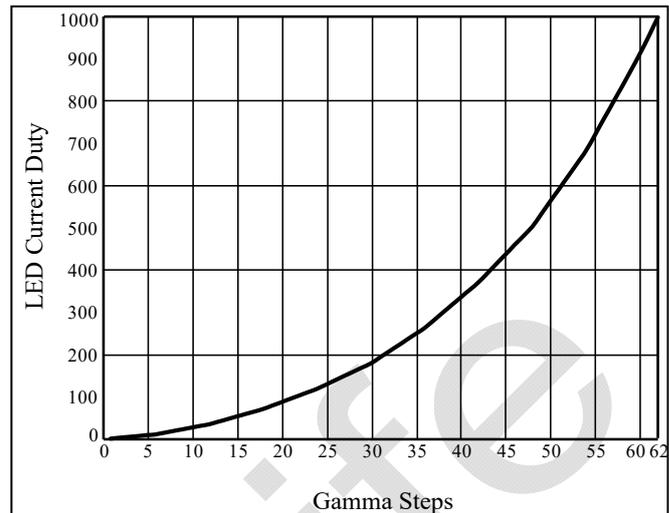


Figure 20 Gamma Correction (63 Steps)

GAMMA CORRECTION

In order to perform a better visual LED breathing effect we recommend using a gamma corrected value to set the LED intensity. This results in a reduced number of steps for the LED intensity setting, but causes the change in intensity to appear more linear to the human eye.

Gamma correction, also known as gamma compression or encoding, is used to encode linear luminance to match the non-linear characteristics of display. Gamma correction will vary the step size of the current such that the fading of the light appears linear to the human eye. Even though there may be 1000 linear steps for the fading algorithm, when gamma corrected, the actual number of steps could be as low as 63.

Table 1 63 Gamma Steps Correction

C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	C(7)
0	2	4	6	8	10	12	16
C(8)	C(9)	C(10)	C(11)	C(12)	C(13)	C(14)	C(15)
20	24	28	32	36	42	48	54
C(16)	C(17)	C(18)	C(19)	C(20)	C(21)	C(22)	C(23)
60	66	72	80	88	96	104	112
C(24)	C(25)	C(26)	C(27)	C(28)	C(29)	C(30)	C(31)
120	130	140	150	160	170	180	194
C(32)	C(33)	C(34)	C(35)	C(36)	C(37)	C(38)	C(39)
208	222	236	250	264	282	300	318
C(40)	C(41)	C(42)	C(43)	C(44)	C(45)	C(46)	C(47)
336	354	372	394	416	438	460	482
C(48)	C(49)	C(50)	C(51)	C(52)	C(53)	C(54)	C(55)
504	534	564	594	624	654	684	722
C(56)	C(57)	C(58)	C(59)	C(60)	C(61)	C(62)	
760	798	836	874	914	956	1000	

FAULT DETECTION

An output shorted to GND fault is detected if the output voltage on a channel drops below the low voltage threshold V_{SCD} and remains below the threshold for t_{FD} . The channel (OUT) will reduce its output current to 20% of I_{SET} . When short condition is removed, output current will recover to original value.

When the ISET pin is shorted to GND and output current is larger than limit value, about 260mA, the output current will be clamped. Once the short fault condition is recovered, the output current will recover to original value.

OVERTEMPERATURE PROTECTION

The device features an integrated thermal rollback feature which will reduce the output current of channel in a linear fashion if the silicon temperature exceeds 130°C (Typical). In the event that the die temperature continues to increase, the device will enter thermal shutdown if the temperature exceeds 155°C.

THERMAL ROLLOFF

The output current of channel will be equal to the set value so long as the die temperature of the IC remains below 130°C (Typical). If the die temperature exceeds this threshold, the output current of the device will begin to reduce at a rate of 3%/°C.

The roll off slope is related to ISET value. When $I_{SET}=20mA$, the roll off slope is about 3.7%. When $I_{SET}=200mA$, the roll off slope is about 2.2%.

THERMAL SHUTDOWN

In the event that the die temperature exceeds 155°C, the output channel will go to the 'OFF' state. At this point, the IC presumably begins to cool off. Any attempt to toggle the channel back to the source condition before the IC cooled to < 135°C will be blocked and the IC will not be allowed to restart.

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THERMAL CONSIDERATIONS

The package thermal resistance, $R_{\theta JA}$, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The $R_{\theta JA}$ is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt ($^{\circ}C/W$). The junction temperature, T_J , can be calculated by the rise of the silicon temperature, ΔT , the power dissipation, P_D , and the package thermal resistance, $R_{\theta JA}$, as in Equation (3):

$$P_D = V_{CC} \times I_{CC} + (V_{CC} - V_{OUT}) \times I_{OUT} \quad (3)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times R_{\theta JA} \quad (4)$$

Where V_{CC} is the supply voltage, V_{OUT} is the voltage of OUT pin and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (5):

$$P_{D(MAX)} = \frac{125^{\circ}C - 25^{\circ}C}{R_{\theta JA}} \quad (5)$$

So,
$$P_{D(MAX)} = \frac{125^{\circ}C - 25^{\circ}C}{50.98^{\circ}C / W} \approx 1.96W$$

Figure 21, shows the power derating of the IS32LT3174 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

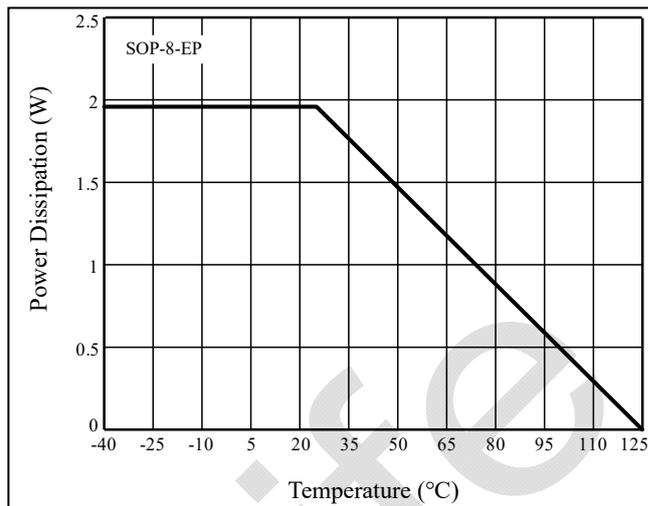


Figure 21 Dissipation Curve

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a copper area of a few square millimeters on each side of the board directly under the IS32LT3120 (SOP-8-EP package) must be used. Multiple thermal vias, as shown in Figure 22, will help to conduct heat from the exposed pad of the IS32LT3120 to the copper on each side of the board. The thermal resistance can be further reduced by using a metal substrate or by adding a heat sink.

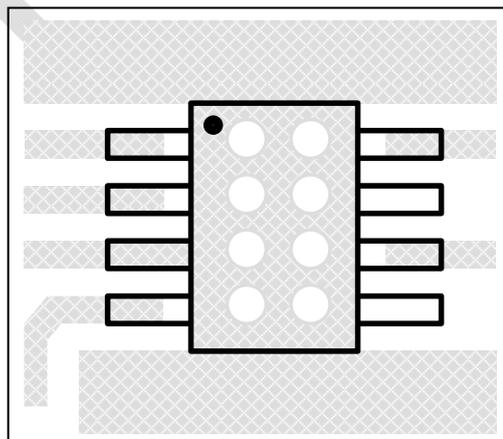


Figure 22 Board Via Layout For Thermal Dissipation

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CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (T _{smin}) Temperature max (T _{smax}) Time (T _{smin} to T _{smax}) (t _s)	150°C 200°C 60-120 seconds
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.
Liquidous temperature (T _L) Time at liquidous (t _L)	217°C 60-150 seconds
Peak package body temperature (T _p)*	Max 260°C
Time (t _p)** within 5°C of the specified classification temperature (T _c)	Max 30 seconds
Average ramp-down rate (T _p to T _{smax})	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

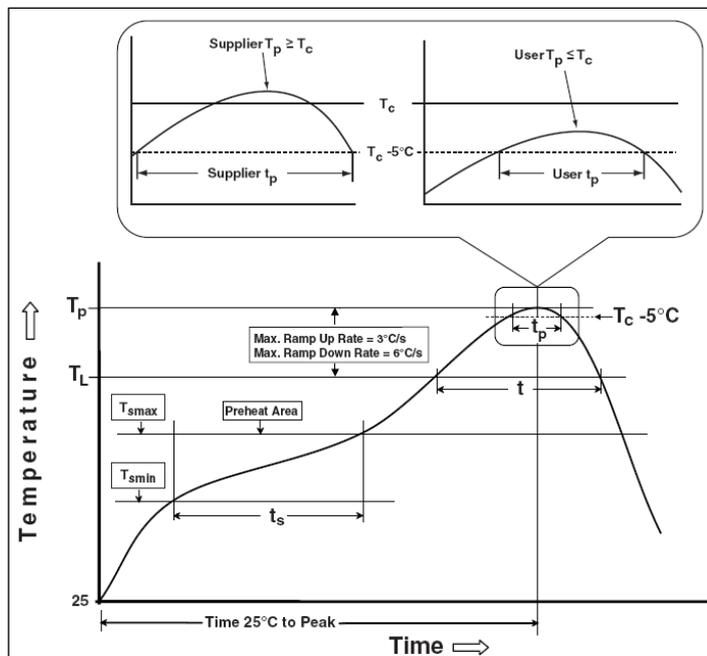
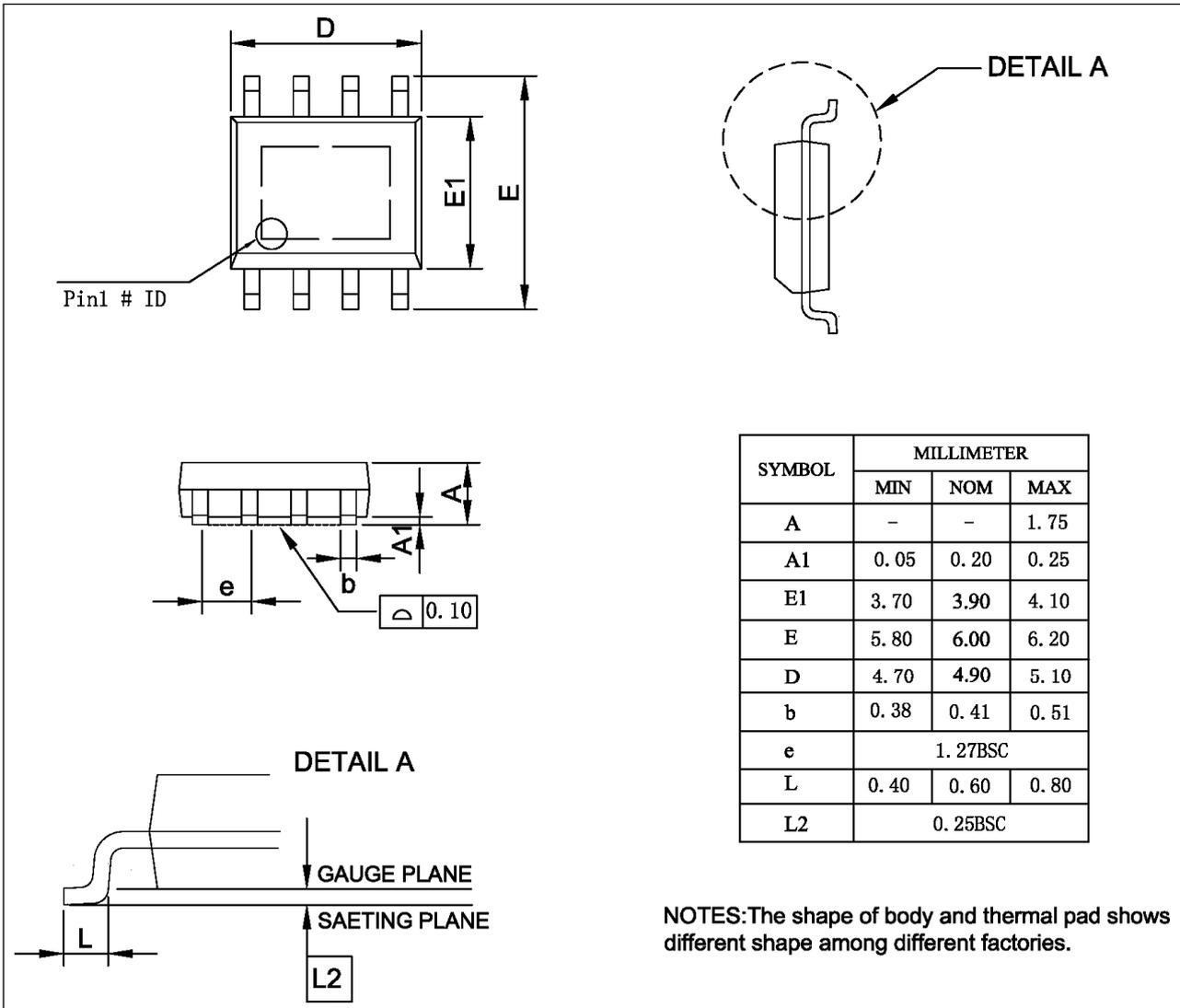


Figure 22 Classification Profile

IS32LT3174

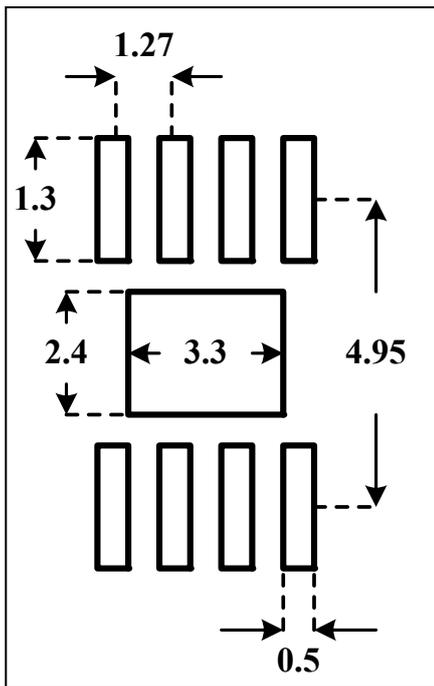
PACKAGE INFORMATION

SOP-8-EP



IS32LT3174

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2016.06.14
B	Add NRND watermark	2022.06.14
C	Change watermark to EOL	2022.08.26