# Quad Driver for GaAs FET or PIN Diode Switches and Attenuators

#### Features

- High Voltage CMOS Technology
- Four Channel
- Positive Voltage Control
- CMOS device using TTL input levels
- Low Power Dissipation
- Low Cost Lead-Free SOIC-16 Plastic Package
- Halogen-Free "Green" Mold Compound
- RoHS\* Compliant

#### Description

The MADR-009190-000100 is a four channel driver used to translate TTL control inputs into gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to 2 V (relative to GND) to optimize the intermodulation products of FET control devices at low frequencies. For driving PIN diode circuits, the outputs are nominally switched between +5 V & -5 V. The actual driver output voltages will be lower when driving large currents due to the resistance of the output devices.



#### Pin Configuration<sup>2</sup>

Pin No.	Function	Pin No.	Function
1	$V_{EE}$	9	Output A1
2	V <sub>CC</sub>	10	Output B1
3	C4	11 Output A2	
4	C3	12	Output B2
5	C2	13	Output A3
6	C1	14	Output B3
7	V <sub>OPT</sub>	15	Output A4
8	Ground	16	Output B4

2. The bottom of the die should be isolated for part number MADR-009190-000DIE and MADR-009190-00GDIE

\* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

1. Reference Application Note M513 for reel size information.

Package

Bulk Packaging 100 piece waffle pack

1000 piece reel

100 piece gel pack

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#### Ordering Information<sup>1</sup>

Part Number

MADR-009190-000100

MADR-009190-000DIE MADR-009190-0001TR

MADR-009190-00GDIE

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#### DC Characteristics over Guaranteed Operating Range

Symbol	Parameter	Test Conditions	Units	Min.	Тур.	Max.
V <sub>IH</sub>	Input High Voltage	Guaranteed High Input Voltage	V	2.0	_	_
V <sub>IL</sub>	Input Low Voltage	Guaranteed Low Input Voltage	V	_	_	0.8
V <sub>OH</sub>	Output High Voltage	I <sub>он</sub> = -0.5 mA	V	V <sub>OPT</sub> - 0.1	_	_
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +0.5 mA	V	_	_	V <sub>EE</sub> + 0.1
I <sub>IN</sub>	Input Leakage Current (per input)	$V_{IN} = V_{CC}$ or GND, $V_{EE} = min$ , $V_{CC} = max$ , $V_{OPT} = min$ or max	nA	-250	_	250
I <sub>OH</sub>	DC Output Current - High (per output)	$V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $V_{OPT}$ = +5.0 V	mA	-35	_	_
I <sub>OL</sub>	DC Output Current - Low (per output)	$V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $V_{OPT}$ = +5.0 V	mA	_	_	35
I <sub>OH_SPIKE</sub>	Peak Spike Output Current (Rising Edge) (per output)	$V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $V_{OPT}$ = +5.0 V, $C_{L}$ = 25 pF	mA	_	35	_
I <sub>OL_SPIKE</sub>	Peak Spike Output Current (Falling Edge) (per output)	$V_{CC}$ = +5.0 V, $V_{EE}$ = -5.0 V, $V_{OPT}$ = +5.0 V, $C_L$ = 25 pF	mA	_	50	_
I <sub>CC</sub>	Quiescent Supply Current		μΑ	_	_	20
$\Delta I_{\rm CC}$	Additional Supply Current (per TTL input pin)	$V_{CC}$ = max, $V_{IN}$ = $V_{CC}$ -2.1 V	mA	_		1.0
I <sub>EE</sub>	Quiescent Supply Current		μΑ	_	_	20
I <sub>OPT</sub>	Quiescent Supply Current		μΑ	_	_	20
R <sub>NFET</sub>	Output Resistance NFET On (to V <sub>EE</sub> )	V <sub>CC</sub> = +5.0 V, V <sub>EE</sub> = -5.0 V, V <sub>OPT</sub> = +5.0 V, V <sub>OUT</sub> = -4.9 V +25°C, Note 3	Ω	_	40	_
R <sub>pfet</sub>	Output Resistance PFET On (to V <sub>OPT</sub> )	V <sub>CC</sub> = +5.0 V, V <sub>EE</sub> = -5.0 V, V <sub>OPT</sub> = +5.0 V, V <sub>OUT</sub> = +4.9 V +25°C, Note 3	Ω	_	45	_

3. See plot of R<sub>NFET</sub> and R<sub>PFET</sub> for variations over temperature for driving 4.99k and 82 ohm resistive load. (Note that this corresponds to 1 mA and 33 mA currents at +25°C).

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#### AC Characteristics Over Guaranteed Operating Range<sup>4</sup>

Symbol	Symbol Parameter Unit	Unit	Typical performance			
Symbol		Unit	-40°C	+25°C	+85°C	
T <sub>PLH</sub>	Propagation Delay	ns	20	22	25	
T <sub>PHL</sub>	Propagation Delay	ns	20	22	25	
T <sub>TLH</sub>	Output Transition Time (Rising Edge)	ns	5	6	8	
T <sub>THL</sub>	Output Transition Time (Falling Edge)	ns	5	6	8	
T <sub>skew</sub>	Delay Skew		2	2	2	
PRF (max.)	x.) 50% Duty Cycle		DC	_	10	
C <sub>IN</sub>	Input Capacitance		5	5	5	
C <sub>PDC</sub>	Power Dissipation Capacitance <sup>5</sup>	pF	50	50	50	
C <sub>PDE</sub>	Power Dissipation Capacitance <sup>5</sup>	pF	100	100	100	

4.  $V_{CC}$  = 4.5 V,  $V_{OPT}$  = 0 V,  $V_{EE}$  = min or max,  $C_L$  = 25 pF, input LOGIC1 = 3 V, LOGIC0 = 0 V,  $T_{RISE}$ ,  $T_{FALL}$  = 6 ns.

5. Total Power Dissipation is calculated by the following formula: PD =  $V_{CC}^2 fC_{PDC} + V_{EE}^2 fC_{PDE}$ .

#### **Truth Table**

Input	Outputs			
Cn	An	Bn		
Logic "0"	V <sub>EE</sub>	V <sub>OPT</sub>		
Logic "1"	V <sub>OPT</sub>	V <sub>EE</sub>		

#### **Handling Procedures**

Please observe the following precautions to avoid damage:

#### **Static Sensitivity**

Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

#### Output Resistance vs. Temperature<sup>6</sup>



6. Output resistance were measured under the condition of  $V_{CC}$  = +5 V,  $V_{OPT}$  = +5 V, and  $V_{EE}$  = -5 V, with load resistors from outputs to ground.

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Symbol	Parameter	Unit	Min.	Тур.	Max.
V <sub>cc</sub>	Positive DC Supply Voltage	V	4.5	5.0	5.5
V <sub>EE</sub>	Negative DC Supply Voltage	V	-10.5	-5.0	-4.5
V <sub>OPT</sub> <sup>10,11</sup>	Optional DC Output Supply Voltage	V	0	_	V <sub>CC</sub>
V <sub>OPT</sub> - V <sub>EE</sub>	Negative Supply Voltage Range		4.5	Note 10,11	16.0
V <sub>CC</sub> - V <sub>EE</sub>	Positive to negative Supply Range		9.0	10.0	16.0
T <sub>OPER</sub>	Operating Temperature		-40	+25	+85
I <sub>OH</sub>	I <sub>OH</sub> DC Output Current - High		-35	_	_
I <sub>OL</sub>	DC Output Current - Low	mA	—	—	35
T <sub>RISE</sub> , T <sub>FALL</sub>	Maximum Input Rise or Fall Time		_	_	500

#### Guaranteed Operating Ranges (for driving FET or PIN devices)<sup>7,8,9</sup>

7.

Unused logic inputs must be tied to either GND or V<sub>CC</sub>. MACOM recommends that V<sub>CC</sub> be powered on before V<sub>EE</sub>, and powered off after V<sub>EE</sub>. 8.

9. 0.01 µF decoupling capacitors are required on the power supply lines.

10. V<sub>OPT</sub> is grounded in most cases when FETs are driven. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies, V<sub>OPT</sub> can be increased to between 1 and 2 V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current that is on the GaAs MMICs will increase when positive controls are applied.

11. When this driver is used to drive PIN diodes,  $V_{OPT}$  is often set to +5 V, with  $V_{EE}$  set to -5 V.



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#### Absolute Maximum Ratings<sup>12</sup>

Symbol	Parameter	Unit	Min.	Max.
V <sub>cc</sub>	Positive DC Supply Voltage		-0.5	7.0
Icc	$\begin{array}{l} \mbox{Positive DC Supply Current} \\ (-0.5 \ \mbox{V} \leq V_{\rm IN} \leq 0.8 \ \mbox{V}; \ 2.0 \ \mbox{V} \leq V_{\rm IN} \leq V_{\rm CC} \ +0.5 \ \mbox{V}; \ \mbox{V}_{\rm CC} \ - \ \mbox{V}_{\rm IN} \leq 7.0 \ \mbox{V} \ ) \end{array}$	mA		20
$V_{EE}$	Negative DC Supply Voltage	V	-11.0	0.5
I <sub>EE</sub>	Negative DC Supply Current (per Output) <sup>13</sup>	mA	-50	_
V <sub>OPT</sub>	Optional DC Output Supply Voltage	V	-0.5	V <sub>CC</sub> +0.5
I <sub>OPT</sub>	Optional DC Output Supply Current (per Output) <sup>13</sup>		_	50
V <sub>OPT</sub> - V <sub>EE</sub>	Output to Negative Supply Voltage Range	V	-0.5	18.0
$V_{CC}$ - $V_{EE}$	Positive to Negative Supply Voltage Range		-0.5	18.0
V <sub>IN</sub>	DC Input Voltage	V	-0.5 Note 14	V <sub>CC</sub> +0.5
Vo	DC Output Voltage	V	$V_{\text{EE}} - 0.5$	V <sub>OPT</sub> + 0.5
$P_D^{15}$	Power Dissipation in Still Air	W		1
T <sub>OPER</sub>	Operating Temperature	°C	-55	125
T <sub>STG</sub>	Storage Temperature	°C	-65	150
ESD	ESD Sensitivity	kV	2.0	_

12. All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.

13. The maximum  $I_{EE}$  and  $I_{OPT}$  are specified under the condition of  $V_{CC}$  = +5.5 V,  $V_{EE}$  = -5.5 V,  $V_{OPT}$  = +5.5 V, and the total power dissipation is within 1 W in still air.

14. If  $V_{CC} \ge 6.5$  V, then the minimum for  $V_{IN}$  is  $V_{CC}$  - 7.0 V. 15. Derate -7 mW/°C from 65°C to 85°C.

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#### Switches and Attenuators

Switching Waveforms



#### Equivalent Output Circuit for An and Bn Outputs (33 mA load at 25°C)



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#### Typical Application for a SPDT Switch<sup>16</sup>



16. Only one section of MADR-009190 is shown. The other three sections will have equivalent performance.

#### **Description of Circuit**

The MADR-009190 provides four pairs of complementary outputs that are each capable of driving a maximum of  $\pm 35$  mA into a load. In addition, with proper capacitor selection (C3 & C4) used in parallel with the current setting resistor (R1 & R2), additional spiking current can be achieved.

To achieve the Non-Inverting and Inverting complementary voltages, each output is switched between two internal FETs. The FETs are connected to  $V_{OPT}$  for the positive output and  $V_{EE}$  for the negative output.  $V_{OPT}$  and  $V_{EE}$  are adjustable for various configurations and have the following limitations:  $V_{EE}$  can be no more negative than -10.5 volts;  $V_{OPT}$  can be no more positive than +5.5 volts and  $V_{OPT}$  must always be less than or equal to  $V_{CC}$ . Increasing  $V_{OPT}$  beyond  $V_{CC}$  will prevent the device from switching states when commanded to by the logic input. The most common configuration is to drive  $V_{EE}$  at -5.0 volts with  $V_{CC}$  and  $V_{OPT}$  tied together at +5.0 volts.

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#### Lead-Free, SOIC-16<sup>†</sup>



Reference Application Note M538 for lead-free solder reflow recommendations. Plating is 100% matte tin over copper.

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#### **Die Outline**



#### Pad Configuration<sup>17,18</sup> Die Size: 1325 x 1735 μm (nominal)

Pad No.	X (µm) nominal	Y (µm) nominal	Pad Size (µm) X x Y	Pad Function
0	0	0	Lower left edge of die	N/A
1	482.95	1489	85 x 85	Vee
2	217.85	1534.6	85 x 85	Vcc
3	200.45	1407.9	85 x 85	C4
4	200.45	1114.2	85 x 85	C3
5	200.45	820.45	85 x 85	C2
6	200.45	526.8	85 x 85	C1
7	200.45	229.35	85 x 85	Vopt
8	395.6	157.95	85 x 85	GND
9	777.55	181.5	132 x 94	A1
10	1126.35	181.75	132 x 94	B1
11	1126.35	436.85	132 x 94	A2
12	1126.35	691.95	132 x 94	B2
13	1126.35	947.05	132 x 94	A3
14	1126.35	1202.15	132 x 94	B3
15	1126.35	1457.3	132 x 94	A4
16	767.9	1553.5	132 x 94	B4
17	1325	1735	Upper right edge of die	N/A

17. All X,Y dimensions are at bond pad center.

18. Die thickness is 8.0 mils.

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