

SX1233SKA

USER GUIDE



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1 Introduction

The SX1233 is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. The advanced feature set, including state of the art packet engine greatly simplifies system design whilst the high level of integration reduces the external BOM to a handful of passive decoupling and matching components. It is intended for use as high-performance, low-cost FSK and OOK RF transceiver for robust frequency agile, half-duplex bi-directional RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

The SX1233 is intended for applications over a wide frequency range, including the 433 MHz and 868 MHz European and the 902-928 MHz North American ISM bands. Coupled with a link budget in excess of 135 dB, the advanced system features of the SX1233 include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIOs which greatly enhance system flexibility whilst at the same time significantly reducing MCU requirements.

The SX1233 complies with both ETSI and FCC regulatory requirements and is available in a 5x5 mm QFN 24 lead package

The SX1233-33SKA is a USB based evaluation tool designed to allow simple and easy evaluation of the suitability of the SX1233 for a given application. The low component count reference design implemented in the SM1233 reference design is illustrated below in Figure 1.

It is recommended that this user guide be read in conjunction with the SX1233 datasheet (http://www.semtech.com/images/datasheet/sx1233.pdf)





Figure 1: SM1233 with Antenna Diversity Application Schematic



2 Getting Started

2.1 Evaluation Kit Contents

The SX1233SKA evaluation kit consists of:

- 1 x SM1233EXXXB module
- 1 x SM12XX <-> USB-Bridge module
- 1 x ¼ wave monopole antenna
- Installation CD or insert sheet
- 1 x Mini USB cable



Figure 2: SM1233 Module Mounted on USB Bridge

2.2 Installation

- 1. Put the CDROM in your computer and browse the contents of the CD, open the "sx1233starterkitsetup.exe" manually. It can be found in the \Installers sub directory of the CD-ROM
- 2. If the evaluation kit is supplied with an insert sheet, follow the instruction on the insert sheet and download the latest version of the software from the weblink provided
- 3. Follow the on-screen installation guidelines until the process is completed. Please note that .NET Framework 3.5 and the FTDI USB driver will be automatically installed if not detected on your computer
- 4. Connect the SX1233SKA board to the PC via the USB interface. The SM1233 module and USB bridge are powered via the USB
- 5. Launch "SX1233SKA" from the Start menu
- 6. Click on "Connect" button in toolbar or in File menu
- 7. SX1233SKA is now installed and ready to be used

2.3 SX1233SKA Overview

The SX1233SKA features the SM1233 reference design and is also interfaced via the FTDI USB Bridge to the USB type 'A' interface of a host PC.

Transmission and reception is indicated by a pair of LEDs on the USB Bridge.

3 SX1233 Quick Start Guide

It is recommended that this user guide is read in conjunction with the SX1233 datasheet.

- 1. Plug the SX1233SKA into the USB port of the computer. The USB power LED on the bridge should be illuminated
- 2. Run the SX1233 User Interface software: Start > All Programs > SX1233SKA > SX1233SKA
- The SX1233SKA should connect automatically to the User Interface Software. If not, click on the USB connect button, located in the top left hand corner of the window toolbar, as illustrated in Figure 4, below
- 4. Once connected the SX1233SKA shows the default configuration of the SX1233 register settings upon power-up, as illustrated in Figure 3. If the EVK is not connected, the GUI screen is grayed out and an error message is displayed in the bottom left hand corner of the status bar.

4 SX1233SKA Software Description

4.1 Overview

Figure 3 illustrates the SX1233SKA graphical user interface (GUI). Each of the numbered captions corresponds to a proceeding chapter within the sections which corresponds to the description of that GUI feature.





Figure 3: SX1233SKA GUI Overview

4.2 Menu Tool Bar

The Menu toolbar contains four drop down menus, File Menu, Action Menu, Tools Menu and Help Menu.

4.2.1 File Menu

Connect / Disconnect allows for the connection or disconnection of the USB bridge from the host PC. This functionality may also be accessed through the short cut buttons of the Window Toolbar (see Section 4.3).

Open Config... allows for the opening of SX1233SKA configuration files (.cfg). This is implemented through a standard Windows file dialog box and may also be accessed through the short cut buttons of the Window Toolbar.

Save Config allows for SX1233SKA configuration files (.cfg) to be saved. This is implemented through a standard Windows file dialog box. The default file name is the last config file saved.



Save Config as... prompts for a new file name before saving, allowing for multiple configuration files to be saved and may also be accessed through the short cut buttons of the Window Toolbar.

Exit closes the application.

File	
-\$₽	Disconnect
2	Open Config
	Save Config
ø	Save Config As
	Exit

Figure 4: File Menu Options

4.2.2 Action Menu

Reset resets the SX1233 configuration registers to the recommended default values.

Refresh reads the status of the all registers.

Show registers toggles the SX1233 Registers display window and may also be accessed through the short cut buttons of the Window Toolbar. The register display window indicates the status of SX1233 configuration registers as detailed in the SX1233 datasheet. Refer to Section for further information.

Monitor ON allows the GUI to constantly scan the status of the Irq registers RegIrqFlags1 and RegIrgFlags2 at addresses 0x27 and 0x28 respectively, and displays the status on the right hand side of the GUI (see Section 4.6 for further details). Monitor OFF disables the monitor function.



Figure 5: Action Menu Options

4.2.3 Tools Menu

RSSI analyzer provides a graphical representation of the signal level at the antenna port measured within the RX filter channel bandwidth, RxBw, at the programmed RF frequency. Refer to See Section 7.4 for further details.



Spectrum Analyzer provides a simple spectrum analyzer function based upon RSSI level within the programmable RX filter channel bandwidth, RxBw. Please refer to Section 7.5 for further details.

	Тос	ols
		RSSI analyser
		Spectrum analyser

Figure 6: Tools Menu Options

4.2.4 Help Menu

Help provides an online description of GUI commands

User's Guide... opens a PDF version of this document.

About... provides details of the GUI revision. The latest version of the SX1233 GUI can be downloaded from the Semtech website.

Help	
🕜 Help	
User	s Guide
Abou	t SX1231 Evaluation Kit

Figure 7: Help Menu Options

4.3 Window Toolbar

The Windows Toolbar provides three buttons that provide shortcuts to some of the functions accessed from the File drop-down menu.







Open Config button opens a Windows file dialog box to allow access to a previously saved SX1233SKA configuration file (.cfg). Note that saved configuration files are designed to be a useful tool for embedded software development. The file can be opened in any text editor or within a spreadsheet to display the programmed register name, address and contents, as illustrated below in Figure 9.

D 5X123	Notepad	
Ele Edit	elp	
Type REG REG REG REG REG REG REG REG REG REG	Address[Hex] 0x00 0x01 0x01 0x02 0x03 0x06 0x07 0x08 0x08 0x09 0x012 0x041 0x12 0x12 0x14 0x15 0x14 0x15 0x18 0x14 0x21	 tex]

Figure 9: Example Configuration File Text Editor Output

Save Config button saves and will prompt if overwriting an existing configuration file.

Connect / Disconnect button allows the user to manage manually connection and disconnection of the kit.

Reset resets the SX1233 configuration registers to the recommended default values.

Refresh reads the status of all registers.

Register Window Toggle toggles the SX1233 Registers display window and may also be accessed through the short cut buttons of the Window Toolbar. The register display window indicates the status of SX1233 configuration registers as detailed in the SX1233 datasheet. Refer to Section 6 for further information.

IRQ Monitor Toggle toggles the scanning of the status of Irq registers *RegIrqFlags1* and *RegIrqFlags2* at addresses 0x27 and 0x28 respectively, and displays the status on the right hand side of the GUI (see Section 4.6 for further details).

Help provides an online description of GUI commands.



4.4 Status Bar

The Status Bar provides details of the SX1233 revision version and current user configuration file. For further information concerning the IC revision, please refer to the SX1233 datasheet.



Figure 10: Status Bar

4.5 Operating Modes Control Box

The Operating Mode control box allows the user to change the operating mode of the SX1233 by clicking on the radio button corresponding to the desired mode. Note that the transition between modes is applied as soon as the radio button is accessed.

When the SX1233 is configured to RX operating mode LED 2 on the USB Bridge is illuminated. When the SX1233 is configured to TX mode both LED 2 and LED 3 are illuminated.

 Sleep Standby Synthesizer Receiver Transmitter 	Operating mode
	🚫 Sleep
O Receiver O Transmitter	💿 Standby 🛛 🔿 Synthesizer
	🔘 Receiver 🛛 🔿 Transmitter

Figure 11: Operating Modes Control Window

4.6 Irq Status Indicator

The Irq Status Flag indicator provides an indication of the status of the Irq registers. When the indicator next to the Irq description is illuminated, the Irq condition is true.

Please refer to the SX1233 datasheet for further information and a more detailed description of the Irq register flags.



ring flags
ModeReady
RxReady
TxReady
PIILock
Rssi
Timeout
AutoMode
SyncAddressMatch
FifoFull
FifoNotEmpty
FifoLevel
FifoOverrun
PacketSent
PayloadReady
CrcOk
LowBat

Figure 12: Irq Status Indicator

4.7 Antenna Switch Control Box

The Antenna Switch Control Box allows users to select the RF path between the SX1233 pins and the SMA connectors of the board; as illustrated in figure 13. Practically, RX input and TX outputs could be connected to either SMA connector according to the user's selection. Pins 18 and 20 of the POD_IN header allow external control of the switch logic.

Antenna switch control Selection: Pin PA_BOOST <=> RF_PA Pin RFIO <=> RF_IO <> Pin PA_BOOST <=> RF_IO < Pin RFIO <=> RF_IO < Pin RFIO <=> RF_PA
--

Figure 13: Antenna Switch Control Window



5 Configuration Registers Tabs

Unless otherwise stated all registers are updated as soon as they are written. It is recommended to cycle through Standby Mode when changing the contents of configuration registers.

5.1 Common Configuration Registers Tab

The Common Configuration Registers tab is illustrated on the following page in Figure 14. Please refer to the SX1233 for a full description of the configuration register functions.

General		Listen mode	
RF frequency:	915'000'000 🔅 Hz	Listen mode:	O ON OFF
Bitrate:	4'800 🕼 bps	Listen resolution idle:	4'100 💉 μs
Fdev:	+/- 5'005 😂 Hz	Listen resolution Rx:	64 🖌 🖌
Sequencer:	💿 ON 🔘 OFF	Listen criteria:	
Bit synchronizer / data mod	e		○ > RssiThreshold & SyncAddress detected
	ON · Packet handler	Listen end:	Rx & Mode after IRQ 😪
	🔘 ON - Continous	Listen idle time:	1'004.500 😒 ms
	OFF- Continous	Listen Rx time:	2.048 😒 ms
Modulation		Antenna switch control	
Modulation:	📀 FSK (OOK		
Modulation shaping:	💿 OFF		⊙ Pin PA_BOOST <=> RF_PA
	🔘 Gaussian filter, BT = 1.0	Selection:	Pin RFIO <=> RF_IO < → Pin PA_BOOST <=> RF_IO
	🔘 Gaussian filter, BT = 0.5		Pin RFIO <=> RF_PA
	🚫 Gaussian filter, BT = 0.3		
Osoillatore		Battery management	
X0 Frequency:	32'000'000 😒 Hz	Low battery detector:	O DN ③ OFF
RC oscillator calibration:	Calibrate	Low battery threshold trim:	1.835 🖌 V
RC oscillator calibration stat	us: 🗿	Low battery indicator:	۵

Figure 14: Common Configuration Register Tab

Configuration register value entries can be selected from the drop down menus within the tab or entered manually within the tab fields. Note that an invalid register entry will be highlighted by an orange background and the GUI will automatically flag a warning exclamation. A valid register entry that leads to an incorrect operating setting will result in that entry to be highlighted in red. Hovering a mouse or cursor over the warning provides an explanation for the flag, as illustrated in Figure 15.

Values entered manually that do not coincide with an exact configuration will be automatically updated by the GUI to the next valid register configuration and write that value to the appropriate configuration register.



General					
RF frequency:		915,000,000	-	Hz	
Bitrate:		4,800	*	bps	
Fdev:	+/-	1,160	*	Hz	•
Sequencer:		💿 ON 🔘 OFF			The modulation index is out of range. The valid range is [0.5, 10]
General					
RF frequency:		915,000,000	*	Hz	
Bitrate:		4,800	*	bps	
Fdev:	+/-	488	* v	Hz	•
Sequencer:		💿 ON 🔘 OFF			The frequency deviation is out of range. The valid range is [600, 300000]

Figure 15: Dialog Box Error Messages

5.1.1 Modulation Mode Window

Clicking on the OOK radio button within the Modulation window will access the modulation shaping options for the OOK modulation mode.

Modulation		Modulation	
Modulation:	💿 FSK 🔿 OOK	Modulation:	🔿 FSK 💿 OOK
Modulation shaping:	OFF	Modulation shaping:	OFF
	🔘 Gaussian filter, BT = 1.0		Filtering with fCutOff = BR
	🔘 Gaussian filter, BT = 0.5		Filtering with fCutOff = 2 * BR
	🔘 Gaussian filter, BT = 0.3		



5.2 Transmitter Configuration Register Tab

The Transmitter Configuration Register Tab is illustrated below in Figure 17. Please refer to the SX1233 datasheet for a full description of the configuration register functions. Configuration register value entries can be selected from the drop down menus within the tab or entered manual within the tab fields. If values are entered manually that do not coincide with an exact configuration, the GUI will automatically update the displayed value to the next valid register configuration and write that value to the appropriate configuration register.

It should be noted that the output power settings are the nominal values determined by the configuration registers and does not refer to measured output power. Please refer to the Application Information within the SX1230 datasheet for further information concerning measured output power vs. programmed power.



Power Amplifier			
PA0 -> Transmits			
○ PA1 -> Transmits			
🔘 PA1 + PA2 -> Tra	ansmits on pin PA_BOO	ST	
PA ramp:	40	🖌 με	
Output power			
	13	🗢 dBm	
Overload current protection	L		
	💿 ON O OFI	-	
Trimming:	95	🗢 mA	

Figure 17: Transmitter Configuration Register Tab

5.3 Receiver Configuration Register Tab

The Transmitter Configuration Register Tab is illustrated below. Please refer to the SX1233 for a full description of the configuration register functions.

Configuration register value entries can be selected from the drop down menus within the tab or entered manual within the tab fields. If values are entered manually that do not coincide with an exact configuration, the GUI will automatically update the displayed value to the next valid register configuration and write that value to the appropriate configuration register.

		5.3.3
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Receiver Lna sensitivitu AFC low beta: O ON 💿 OFF 0 50 DCC frequency: 207 🗘 Hz Input impedance: ohms 200 AFC low beta offset: 0 * Hz 5,208 🗘 Hz Rx filter bandwidth: Sensitivity boost: 🔘 ON 💿 OFF AFC auto clear: 🔿 ON 💿 OFF AFC auto: 🔘 ON 💿 OFF AFC bandwidth AFC: Start Clear 0 Hz DCC frequency: 249 🗘 Hz DAGC: 💿 ON 🔘 OFF Read 0 Hz FEI: 25.000 🗘 Hz Bx filter bandwidth: 5.3.5 5.3.1 -Timeout Bx start: ms Threshold type: Peak ~ Timeout threshold: 0 \$ ms Peak threshold step: 0.5 🗘 dB Auto threshold: 💿 ON 🔿 OFF Peak threshold dec: Once per chip ~ Threshold: dBm Avg threshold cutoff: 5.3.4 -117.0**a** dBr Value 😂 dB Fixed threshold: 6 5.3.2 Restart Rx 💿 Auto 🔘 Manual Phase Reference Threshold 1 Threshold 2 Threshold 3 Threshold 4 Threshold 5 AGC -111 -95 -88 -77 -68 -57 -> Pin [dBm] G2 G1 G3 G4 G5 G6 Gain: 💿 Auto 🔘 Manual

Figure 18: Receiver Configuration Register Tab

5.3.1 Rx Bandwidth

The Rx Bandwidth, RxBw, window is illustrated below. For optimum performance in FSK mode when operating with a modulation index \geq 2, the DCC frequency is recommended to be approximately 4% of the receiver bandwidth, RxBw. The GUI will automatically set the appropriate DCC frequency based upon the setting of RX filter bandwidth.

- Rx bandwidth		
DCC frequency:	414	🗘 Hz
Rx filter bandwidth:	10,417	🗘 Hz
AFC bandwidth		
DCC frequen <mark>cy:</mark>	497	🗘 Hz
Rx filter bandwidth:	50,000	🗘 Hz

Figure 19: Rx Bandwidth Window

For operation with low modulation index signals, it is recommended that the user follows the recommendations for setting the correct DCC bandwidth that can be found in the SX1233 datasheet.

5.3.2 LNA Gain Window

The LNA gain window provides the status of the configured LNA gain. The gain can be configured automatically or manually. In automatic mode the LNA gain is set based upon the RSSI value. In manual mode, the gain should be set according to the expected signal power.

Note that the AGC reference threshold is set according to:

AgcRef = [-174 + NF + 10*log(2*RxBw) + DemodSNR + FadingMargin] dBm



Figure 20: LNA Gain Window

5.3.3 AFC / FEI

The AFC / FEI (Frequency Error Indicator) window is illustrated below. Note that when AFC is activated (either AFC auto "ON" or manually), the RF frequency in the General window of the Common Configuration Register Tab does not update, although a measure of frequency error can be obtained by clicking on the FEI Read button to verify correct AFC operation.

Enabling AFC low beta implements a double AFC function to offset the local oscillator of the SX1233 to ensure that the central tone at f_0 associated with low modulation index signals is not unduly attenuated by the cut-off frequency of the DCC.

Please refer to the optimized set up for low modulation index systems section of the SX1233 datasheet for further details.

AFC / FEI				
AFC low beta:	🔿 ON	💿 OFF		
AFC low beta offset:	0	*	Hz	
AFC auto clear:	🔿 ON	📀 OFF		
AFC auto:	🔘 ON	💿 OFF		
AFC: Start Clear	0		۲	Hz
FEI: Read	0		0	Hz

Figure 21: AFC / FEI Window

5.3.4 RSSI

The RSSI window provides access to the RSSI timeout and timeout threshold functions and enable either automatic or manual RSSI detection threshold values to be programmed. Note that the RSSI threshold (which should not be confused with the LNA or AGC threshold) can be calculated from and equates to the effective noise floor of the receiver for a given filter bandwidth.

RSSIthres = [-174 + NF + 10*log(2*RxBw) + DemodSNR] dBm



ſ	RSSI		
	Timeout Rx start:	0	ms
	Timeout threshold:	0	ms
	Auto threshold:	💿 ON OFF	
	Threshold:	-116.0	dBm
	Value:	-127.5 🥥	dBm
	Phase: Restart Rx	💿 Auto i 🔘 Manual	

Figure 22: RSSI Window

5.3.5 Continuous-Time Digital AGC

The AGC dynamic range can be enhanced in V2c silicon (chip version 2.3) with the default mode of operation of DAGC enabled. Note that the DAGC mode of operation is automatically configured by the GUI depending upon whether AFC low beta is enabled (see section 5.3.3).

Pease refer to the SX1233 datasheet for further information on the implementation of the continuous-time DAGC function.

- DAGC	
DAGC:	💿 ON 🔘 OFF

Figure 23: DAGC Window

5.4 Irq & Mapping Configuration Register Tab

The Irq & Mapping Configuration Register Tab is illustrated in Figure 24. Please refer to the SX1233 for a full description of the irq and mappings for each mode of operation of the SX1233.

Configuration register value entries can be selected from the drop down menus besides each DIO listed.

Note that when necessary the GUI will automatically re-configure DIO mappings (i.e. Packet Handler operation).

Please refer to Table 1 and Table 2, below, for the available DIO mappings of the SX1233 in continuous and packet mode, respectively.

Mode	DIOx	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
	Mapping						

	00	-	-	-	-	-	-
Sleep	01	-	-	-	-	-	-
Sleep	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	-	-	-	-	ModeReady
	00	ClkOut	-	-	-	-	-
Standby	01	-	-	-	-	-	-
Stanuby	10	LowBat	LowBat	AutoMode	-	-	LowBat
	11	ModeReady	-	-	-	LowBat	ModeReady
	00	ClkOut	-	-	-	-	PIILock
FS	01	-	-	-	-	-	-
FS	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	PIILock	-	-	PIILock	ModeReady
	00	ClkOut	Timeout	Rssi	Data	Dclk	SyncAddr
RX	01	Rssi	RxReady	RxReady	Data	RxReady	Timeout
	10	LowBat	SyncAddr	AutoMode	Data	LowBat	Rssi
	11	ModeReady	PIILock	Timeout	Data	SyncAddr	ModeReady
	00	ClkOut	TxReady	TxReady	Data	Dclk	PIllock
тх	01	ClkOut	TxReady	TxReady	Data	LowBat	TxReady
	10	LowBat	LowBat	AutoMode	Data	LowBat	LowBat
	11	ModeReady	PIILock	TxReady	Data	PIILock	ModeReady

Table 1: Continuous Mode DIO Mappings

Mode	DIOx Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
	00	-	-	FifoFull	FifoNotEmpty	FifoLevel	-
Sleep	01	-	-	-	-	FifoFull	-
Sleep	10	LowBat	LowBat LowBat LowBat FifoNotEmpty		LowBat		
	11	ModeReady	-	-	AutoMode	-	-
	00	Clkout	-	FifoFull FifoNotEmpty FifoLevel -		-	
Standby	01	-	-	-	-	FifoFull	-
Stanuby	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
	00	Clkout	-	FifoFull	FifoNotEmpty	FifoLevel	-
FS	01	-	-	-	-	FifoFull	-
13	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PIILock	PIILock	AutoMode	PIILock	PIILock
	00	Clkout	Timeout	FifoFull	FifoNotEmpty	FifoLevel	CrcOk
RX	01	Data	Rssi	Rssi	Data	FifoFull	PayloadReady
	10	LowBat	RxReady	SyncAddr	LowBat	FifoNotEmpty	SyncAddr
	11	ModeReady	PIILock	PIILock	AutoMode	Timeout	Rssi
	00	Clkout	ModeReady	FifoFull	FifoNotEmpty	FifoLevel	PacketSent
тх	01	Data	TxReady	TxReady	Data	FifoFull	TxReady
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PIILock	PIILock	AutoMode	PLLlock	PIILock

Table 2: Packet Mode DIO Mappings



IRQ & Map Device status Bit Synchronizer: ON Data mode: Packet Operating mode: Receiver DIO mapping DI05: ClkOut Y Timeout DIO4: * FifoFull ¥ DI03: FifoNotEmpty DI02: * FifoLevel DI01: * DI00: CrcOk * - Clock out 🖌 Hz OFF Frequency:

Figure 24: Irq & Mapping Configuration Register Tab

5.5 Packet Handler Configuration Register Tab

The Packet Handler Configuration Register Tab is shown below. Please refer to the SX1233 for a full description of the packet engine message format and operation of the SX1233.

5.5.1		Packet	Handler					
0.0.1	Preamble size:	3		bytes A	ddress based filtering:	📀 OFF	Node 🔿 Node or Broadcast	
	Sync word:	💿 ON 🔿 OFF		N	ode address:	0	0x00	
	FIFO fill condition:	💿 Sync address 🛛 🔘) Always	B	roadcast address:	0	\$ 0x00	
	Sync word size:	4		bytes D	C-free:	📀 OFF	Manchester 🔘 Whitening	
	Sync word tolerance:	0		bits Ci	RC calculation:	📀 ON	◯ OFF	
	Sync word value:	01-01-01-01		C	RC auto clear:	📀 ON	O OFF	
	Packet format:	🔘 Variable 🛛 💿 Fixe	d	A	ES:	🔿 ON	⊙ OFF	
	Payload length:	20 🗢 0x14		bytes _{Al}	ES key:	00-0	00-00-00-00-00-00-00-00-00-00-00-00-00-	
	Intermediate mode enter:	None (Auto Modes Of	FF) N	Z T:	x start:	🔘 Fifol	Level 💿 FifoNotEmpty	
	Intermediate mode exit:	None (Auto Modes Of	FF) 💊	E FI	IFO Threshold:	15	\$	
	Intermediate mode:	Sleep	1	< In	iter packet Rx delay:	0.208	ms	
	1			_				
5.5.2	Packet						Device status	
	Preamble	Sync	Length	Node Addre	ss Message	CRC	Bit Synchronizer: ON	
	55-55-55	01-01-01-01				AD-F8	Data mode: Packet	5.5.3
	Message						Operating mode: Receiver	5.5.5
		HEXADECIMAL	4 20 50	61 79 Se	ASCII mtech Test Pav		Start Log	
	6C 6F 61 64			10	ad		Rx packets: 0	
						~		
	0							1

Figure 25: Packet Handler Configuration Register Tab



5.5.1 Sync Word

For correct packet mode operation, the sync word needs to be set to at least one byte. Note that 0x00 can not be set as for the first byte of the sync word. The GUI will prompt with an error message should the user attempt to set 0x00 in the first byte of the sync word.

5.5.2 AutoMode Operation

Auto Modes defines the enter conditions to start the packet handler and exit conditions to terminate packet handler operation, as defined in the SX1233 datasheet.

5.5.3 Packet Log

Clicking on the Log button within the Control Window enables the payload logging function, available in both TX and RX modes whenever the Packet Handler is enabled.

5 Packet Log
Status Bar Max samples: 10 Browse Start Close

Figure 26: Packet Logger Window

In the Packet Logger window enter the number of packets to be logged and press the Start button. Then press the Start button in the Control Window of the main Packet Handler Tab to start packet transmission or reception. When the status bar indicates full, the log can be saved by clicking on the Browse button.

The log file can be viewed in Notepad or opened in Excel as a .CSV file

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1					and the second se	1.11.01.11	5/2011 at 05:46	and the second for the second	10.00	J					ľ	ALC: N		20.1.22		han dia mai		-
2	#						Preamble Size		Length	Node Address	Maeeana										CRC	
3		46:52.3		11001	10			01-01-01-01	14		53-65-6D-7	74-65	63-68	20-54	1-65-7	3-74-	20-50-	61-79	9-6C-P	F-61-6		1
4	t	46:52.4			10	1		01-01-01-01	14		53-65-6D-1											
5		46:52.5			10	2	3	01-01-01-01	14		53-65-6D-											3
6		46:52.6	Τx		10	3	3	01-01-01-01	14		53-65-6D-7	74-65	-63-68-	20-54	1-65-7	3-74-	20-50-	61-79	9-60-6	F-61-6	AD-F8	3
7.		46:52.7	Tx		10	4	3	01-01-01-01	14		53-65-6D-7	74-65	63-68	20-54	4-65-7	3-74-	20-50-	61-79	9-6C-8	6F-61-6	4 AD-F8	3
8		46:52.8			10	5	-	01-01-01-01	14		53-65-6D-7	74-65	-63-68	20-54	4-65-7	3-74-	20-50-	-61-79	9-60-6	6F-61-6		
9		46:53.0			10	6		01-01-01-01	14		53-65-6D-7											
10		46:53.1			10	7		01-01-01-01	14		53-65-6D-											
11		46:53.2			10	8	-	01-01-01-01	14		53-65-6D-											_
12	-	46:53.3	Тх		10	9	3	01-01-01-01	14		53-65-6D-7	74-65	63-68	20-54	4-65-7	3-74-	20-50	61-79	3-6C-6	67-61-6	4 AD-F8	3
13																						
•	• 1	► ► \\sx	1233-	pkt /							•										,	
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Figure 27: Packet Log CSV File Format

Packet Log Parameter	Description
Time	Local (CPU) timestamp in MM:SS.S format for TX / RX packets
Mode	SX1233 Packet Mode
RSSI	Indicated RSSI level (RX mode only)
Pkt Max	Number of repeated packets set in GUI Control Window (0 = infinite)
Pkt #	Transmitted or received packet number
Preamble Size	Size of transmitted or received preamble sequence
Sync	Sync Address
Length	Payload length of TX / RX packet
Node Address	node Address (optional)
Message	Transmitted / received packet (can be viewed in GUI Message Window)
CRC	Transmitted / received CRC (optional)

Table 3: Packet Log Descriptors

5.5.4 Packet Handler GUI Limitations

When operating the packet handler via the SKA GUI, the user should be aware of the following limitations associated with the GUI:

- Minimum Preamble Size = 2 bytes
- Maximum Packet Length = 66 bytes (64 bytes of data + Length byte + Address byte)

5.6 Temperature Configuration Register Tab

The Temperature Configuration Register Tab is illustrated below in Figure 29. Note that user is prompted to calibrate the SX1233 temperature sensor by clicking on the Calibrate button to access the temperature calibration dialog box.



Figure 28: Temperature Calibration Dialog Box

When the temperature sensor has been calibrate the temperature, as computed by the SX1233, will be displayed, as illustrated in Figure 29.





Figure 29: Calibrated Temperature Sensor Tab



6 Registers Display Window

As outlined in Section 4.2.3 the SX1233 GUI has a show registers utility that, when enabled from either the Menu or Windows toolbar, provides details of the status of all configuration registers that are documented in the SX1233 datasheet.

Whenever the contents of a register are changed in the main GUI window, the corresponding register displays the new contents of the register(s), highlighting changed contents in red for a period of approximately 5 seconds before reverting back to black.

The register window is displayed below in Figure 30. It can be noted that in this example, the contents of RegOpMode at Addr 0x01 have changed to 0x10, indicating that the SX1233 has been set to Receiver Mode operation.

Register	Addr	Value	Register	Addr	Value	Register	Addr	Value	Register	Addr	Value	Register	Addr	Value
RegFifo	0x00	0.00	Reserved14	0x14	0x40	ReglrqFlags2	0x28	0x00	RegFifoThresh	0x3C	0x8F	RegTestLna	0.58	0x1B
RegOpMode	0x01	0x10	Reserved15	0x15	0xB0	RegRssiThresh	0x29	0xE4	RegPacketConfig2	0x3D	0x02	RegTestDagc	0x6F	0x30
RegDataModul	0x02	0x00	Reserved16	0x16	0x7B	RegRxTimeout1	0x2A	0x00	RegAesKey1	0x3E	0x00	RegTestAic	0x71	0x00
RegBitrateMsb	0x03	0x1A	Reserved17	0x17	0x9B	RegRxTimeout2	0x28	0x00	RegAesKey2	0x3F	0x00	1		
RegBitrateLsb	0x04	0x0B	RegLna	0x18	0x88	RegPreambleMsb	0x2C	0x00	RegAesKey3	0x40	0x00			
RegFdevMsb	0x05	0x00	RegRxBw	0x19	0x55	RegPreambleLsb	0x2D	0x03	RegAesKey4	0x41	0x00			
RegFdevLsb	0x06	0x52	RegAfcBw	0x1A	0x88	RegSyncConfig	0x2E	0x98	RegAesKey5	0x42	0x00			
RegFrfMsb	0x07	0xE4	RegOokPeak	0x1B	0x40	RegSyncValue1	0x2F	0x01	RegAesKey6	0x43	0x00			
RegFrfMid	0x08	0xC0	RegOokAvg	0x1C	0x80	RegSyncValue2	0x30	0x01	RegAesKey7	0x44	0x00			
RegFrfLsb	0x09	0x00	RegOokFix	0x1D	0x06	RegSyncValue3	0x31	0x01	RegAesKey8	Dx45	0x00			
Reg0sc1	0x0A	0x41	RegAfcFei	0x1E	0x10	RegSyncValue4	0x32	0x01	RegAesKey9	0x46	0x00			
RegAfcCtrl	0x0B	0x40	RegAfcMsb	0x1F	0x00	RegSyncValue5	0x33	0x01	RegAesKey10	0x47	0x00			
RegLowBat	0x0C	0x02	RegAfcLsb	0x20	0x00	RegSyncValue6	0x34	0x01	RegAesKey11	0x48	0x00			
RegListen1	0x0D	0x92	RegFeiMsb	0x21	0x00	RegSyncValue7	0x35	0x01	RegAesKey12	0x49	0x00			
RegListen2	0x0E	0xF5	RegFeiLsb	0x22	0x00	RegSyncValue8	0x36	0x01	RegAesKey13	Ox4A	0x00			
RegListen3	0x0F	0x20	RegRssiConfig	0x23	0x00	RegPacketConfig1	0x37	0x10	RegAesKey14	0x4B	0x00			
RegVersion	0x10	0x23	RegRssiValue	0x24	0xC8	RegPayloadLength	0x38	0x42	RegAesKey15	0x4C	0x00			
RegPaLevel	0x11	0x9F	RegDioMapping1	0x25	0x00	RegNodeAdrs	0x39	0x00	RegAesKey16	0x4D	0x00	1		
RegPaRamp	0x12	0x09	RegDioMapping2	0x26	0x07	RegBroadcastAdrs	0x3A	0x00	RegTemp1	Ox4E	0x01			
RegOcp	0x13	0x1A	RegirgFlags1	0x27	0xD8	RegAutoModes	0x3B	0x00	RegTemp2	Ox4F	0x8C			

Figure 30: SX1233 Registers Display Window



7 Advanced Operating Modes

7.1 Packet Communications Test

To configure the SX1233 to enable a wireless packet communications transfer, follow the procedure outlined below:

7.1.1 Transmitter Mode Configuration

- 1. Ensure that the SX1233 is in Standby operating Mode
- 2. Configure the SX1233 Common and Transmitter Configuration Registers
- 3. Configure the Packet Handler Registers for the payload you wish to transmit. The payload can be entered within the Message Window in either hexadecimal or ASCII format. Note that the packet can be configured with Address and / or Broadcast nodes enabled or disabled; DC-free mechanisms, CRC and / or AES may also be selected. The only limitation is that he maximum payload size for the purposes of GUI operation is 66 bytes
- 4. Click on the Transmitter radio button from within the Operating Mode Window and set the Repeat value from within the Control Window of the Packet Handler Tab. It is recommended for initial analysis that Repeat value is set to "0" (packet transmission repeat until manually stopped)
- 5. Click on the Start button within the Control Window of the Packet Handler Tab to start the Transmitter
- 6. The TX packet counter will commence to increment as the SX1233 repeatedly transmits the payload

7.1.2 Receiver Mode Configuration

- 1. Ensure that the SX1233 is in Standby operating Mode
- 2. Configure the SX1233 Common and Receiver Configuration Registers. The Common configuration should be identical to that of the SX1233 configured as the transmitter. The Receiver filter BW configuration should be consistent with the signal parameters. It is recommended that the configuration of the transmitter module is used as a template
- 3. Configure the Packet Handler Registers for the payload you wish receive. Note that the packet can be configured with Address and / or Broadcast nodes enabled or disabled; DC-free mechanisms, CRC and / or AES may also be selected. The packet handler parameters must be identical for those selected for the transmitter for correct operation. The only limitation is that he maximum payload size for the purposes of GUI operation is 66 bytes
- 4. Click on the Receiver radio button from within the Operating Mode Window and set the Repeat value from within the Control Window of the Packet Handler Tab
- 5. Click on the Start button within the Control Window of the Packet Handler Tab to start the Receiver
- 6. The RX packet counter will commence to increment for each valid packet reception

7.2 Test Mode Window

The Test Mode window is accessed by depressing the <CTRL>+<ALT>+<T> keys of the PC keyboard simultaneously, and is illustrated below in Figure 31.

This window allows the user to write to and read from the contents of individual configuration register addresses. Note that address and data are entered in hexadecimal format.

The Antenna switch control dialog box enables control of the antenna diversity switch for the SX1233 antenna diversity reference design



5 Test	
- Registers	
	Address Data
	0x00 0x00
	Write Read
Antena swite	ch control
Switch:	🔿 Auto 💿 Manual 🔘 OFF
Selection:	O Pin PA_BOOST <=> RF_PA Pin RFIO <=> RF_IO ✓ Pin PA_BOOST <=> RF_IO ✓ Pin PA_BOOST <=> RF_PA Pin RFIO <=> RF_PA
	.:

Figure 31: Test Mode Window

7.3 Verification Mode

When no SX1233SKA is connected to the PC, launching the application results in the GUI display being grayed out and the user is unable to enter data.

By depressing the <CTRL>+<ALT>+<N> keys of the PC keyboard simultaneously, the user can write to the configuration registers to verify propose settings, as well as load and save configuration files (*.cfg).

7.4 RSSI Analyzer

The RSSI Analyzer can be enabled via the Menu Tool Bar. With the SX1233 configured in Receiver operating mode the RSSI analyzer displays the real-time sampled RSSI measured in the receiver channel bandwidth. The vertical axis (indicated RSSI level) can be scaled with the click-wheel of a scrolling mouse

This data can be saved as a RSSI log file by selecting an appropriate Max sample length within the RSSI Analyzer window and clicking on the Start button. When the status bar indicates full, the log file can be saved by clicking on the Browse button and can be viewed in Notepad or opened in Excel as a .CSV file.

An example of the RSSI Analyzer display is illustrated in Figure 32, indicating a packet transmission typically 10 dB above the receiver noise floor.





Figure 32: RSSI Analyzer Window

7.5 Spectrum Analyzer

The Spectrum Analyzer can be enabled via the Menu Tool Bar. With the SX1233 configured in Receiver operating mode the spectrum analyzer displays the sampled spectrum based upon RSSI measured within the programmable receiver channel or "resolution" bandwidth. Center frequency, frequency span and LNA gain are all configurable. The vertical axis (Power) can be scaled with the click-wheel of a scrolling mouse

An example of the RSSI Analyzer display is illustrated in Figure 33.



Figure 33: RSSI Analyzer Window



8 Compatibility with Earlier Silicon Revisions

The SX1233 GUI is backwards compatible with Rev 2.1 Silicon (SX1233 datasheet Revision 2.0). The GUI automatically detects the silicon revision number, displaying the chip version in the status bar at the bottom of the GUI.

Configuration Register Tabs are automatically updated to display register contents pertinent to the chip version.

Semtech's policy of continual improvement may result in information contained within this User Guide not being concurrent with the revision of software included on the installation CD

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Contact information

Semtech Corporation Advanced Communication and Sensing Products Division 200 Flynn Road, Camarillo, CA 93012 Phone: (805) 498-2111 Fax: (805) 498-3804 E-mail: sales@semtech.com Support_RF@semtech.com Internet: http://www.semtech.com