

# M27V160

## 16 Mbit (2Mb x8 or 1Mb x16) Low Voltage UV EPROM and OTP EPROM

## **Features**

- 3V to 3.6V Low Voltage in Read Operation
- Access Time: 100 ns
- Byte-wide or Word-wide Configurable
- 16 Mbit Mask ROM Replacement
- Low Power Consumption
  - Active Current: 30 mA at 8 MHz
  - Standby Current: 60 µA
- Programming Voltage: 12.5V ± 0.25V
- Programming Time: 50 µs/word
- Electronic Signature
  - Manufacturer Code: 20h
  - Device Code: B1h
- obsolete Product(s).



# Contents

1	ummary description	5
2	evice description	8
	1 Read mode	8
	2 Standby mode	8
	3 Two-line output control	9
	4 System considerations	9
	5 Programming	9
	6 Presto III programming algorithm	10
	7 Program Inhibit	10
	8 Program Verify	10
	9 Electronic Signature	11
	10 Erasure operation (applies to UV EFROM)	11
3	aximum ratings	12
4	C and AC parameters	13
5	ackage mechanical data	18
	1 42-pin Ceramic Frit-seal DIP with window (FDIP42WB)	
	2 12-pin Plastic DIP, 600 mils width (PDIP42)	19
	42-lead Shrink Plastic DIP, 600 mils width (SDIP42)	20
<u> </u>	4 44-lead Square Plastic Leaded Chip Carrier (PLCC44)	21
002	5 44-lead Plastic Small Outline, 525 mils body width (SO44)	22
6	art Numbering	23
005	evision history	24



## List of tables

	Table 1.	Signal descriptions	
	Table 2. Table 3.	Operating Modes	
	Table 3. Table 4.	Absolute Maximum Ratings	
	Table 5.	Read Mode DC Characteristics	
	Table 6.	Programming Mode DC Characteristics	. 13
	Table 7.	AC Measurement Conditions	
	Table 8.		
	Table 9. Table 10.	Read Mode AC Characteristics       Programming Mode AC Characteristics	
	Table 10.	FDIP42WB package mechanical data	
	Table 12.	PDIP42 package mechanical data	
	Table 13.	SDIP42 package mechanical data	
	Table 14.	PLCC44 package mechanical data	
	Table 15. Table 16.		. 22
	Table 17.	Document revision history	. 23
		*(5)	
		ete Product(s) obsole	
		P1 .(S)	
	1	Sto Yue	
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	-01		
	NS I		
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57

# List of figures

Logic Diagram5DIP Connections6SO Connections7PLCC Connections7Programming Flowchart10AC Testing Input Output Waveform14AC Testing Load Circuit14Word-Wide Read Mode AC Waveforms16Byte-Wide Read Mode AC Waveforms16BYTE Transition AC Waveforms17Programming and Verify Modes AC Waveforms17
FDIP42WB package outline
ate Product(s) obsolete ate Product(s)



## 1 Summary description

The M27V160 is a low voltage 16 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for microprocessor systems requiring large data or program storage. It is organised as either 2 Mbit words of 8 bit or 1 Mbit words of 16 bit. The pin-out is compatible with a 16 Mbit Mask ROM.

The M27V160 operates in the read mode with a supply voltage as low as 3V. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

The FDIP42W (window ceramic frit-seal package) has a transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written rapidly to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27V160 is offered in PDIP42, SDIP42, PLCC44 and SO 44 prockages.

In order to meet environmental requirements, ST offers the M27V160 in COPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering cor. the same also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® sub cifications are available at: www.st.com.

See *Figure 1: Logic Diagram* and *Tak le i* Signal descriptions for a brief overview of the signals connected to this device.





Signal	Description
A0-A19	Address Inputs
Q0-Q7	Data Outputs
Q8-Q14	Data Outputs
Q15A–1	Data Output / Address Input
Ē	Chip Enable
G	Output Enable
BYTEV <sub>PP</sub>	Byte Mode / Program Supply
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground
NC	Not Connected Internally

Table 1. Signal descriptions

#### Figure 2. DIP Connections





Figure 3. SO Connections

57

## 2 Device description

*Table 2* lists the operating modes of the M27V160. A single power supply is required in the read mode. All inputs are TTL compatible except for  $V_{PP}$  and 12V on A9 for the Electronic Signature.

Mode	Ē	G	<b>BYTE</b> V <sub>PP</sub>	A9	Q15A–1	Q14-Q8	Q7-Q0
Read Word-wide	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Х	Data Out	Data Out	Data Out
Read Byte-wide Upper	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Х	V <sub>IH</sub>	Hi-Z	Data Out
Read Byte-wide Lower	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	Х	V <sub>IL</sub>	Hi-Z	Data Out
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	Х	Х	Hi-Z	Hi-Z	Hi-Z
Program	V <sub>IL</sub> Pulse	V <sub>IH</sub>	V <sub>PP</sub>	Х	Data In	L'at 🛛 In	Data In
Verify	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>PP</sub>	Х	Data Out	Data Out	Data Out
Program Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>PP</sub>	Х	Hi-Z	Hi-Z	Hi-Z
Standby	V <sub>IH</sub>	Х	Х	X	Hi-Z	Hi-Z	Hi-Z
Electronic Signature	V <sub>IL</sub>	V <sub>IL</sub>	VIH	V <sub>ID</sub>	Code	Codes	Codes

Table 2.Operating Modes (1)

1.  $X = V_{IH}$  or  $V_{IL}$ ,  $V_{ID} = 12V \pm 0.5V$ .

## 2.1 Read mode

The M27V160 has two organisations, Word-wide and Byte-wide. The organisation is selected by the signal level on the BYTEV<sub>PP</sub> pin. When BYTEV<sub>PP</sub> is at V<sub>IH</sub> the Word-wide organisation is selected and the Q15A–1 pin is used for Q15 Data Output. When the BYTEV<sub>PP</sub> pin is at V<sub>IL</sub> the Byte-wide organisation is selected and the Q15A–1 pin is used for the Address input A–1. When the memory is logically regarded as 16 bit wide, but read in the Byte-wide organisation, then with A–1 at V<sub>IL</sub> the lower 8 bits of the 16 bit data are selected.

The M27V160 has two control functions, both of which must be logically active in order to obtain data at the outputs. In addition the Word-wide or Byte- wide organisation must be selected.

Chip Enable  $(\overline{E})$  is the power control and should be used for device selection. Output Enable  $(\overline{G})$  is the output control and should be used to gate data to the output pins independent of device selection. Assuming that the addresses are stable, the address access time  $(t_{AVQV})$  is equal to the delay from  $\overline{E}$  to output  $(t_{ELQV})$ . Data is available at the output after a delay of  $t_{GLQV}$  from the falling edge of  $\overline{G}$ , assuming that  $\overline{E}$  has been low and the addresses have been stable for at least  $t_{AVQV}$ - $t_{GLQV}$ .

## 2.2 Standby mode

The M27V160 has a standby mode which reduces the active current from 20mA to 20µA with low voltage operation  $V_{CC} \leq 3.6V$ , see Read Mode DC Characteristics table for details. The M27V160 is placed in the standby mode by applying a CMOS high signal to the



 $\overline{E}$  input. When in the standby mode, the outputs are in a high impedance state, independent of the  $\overline{G}$  input.

### 2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines,  $\overline{E}$  should be decoded and used as the primary device selecting function, while  $\overline{G}$  should be made a common connection to all devices in the array and connected to the READ line from the system control bus initial ensures that all deselected memory devices are in their low power standby riode and that the output pins are only active when data is required from a particular nemery device.

### 2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the supplies to the devices. The supply current I<sub>CC</sub> has three segments of importance to the system designer: the standby current, the active current and the transient peaks that are produced by the falling and rising edges of  $\overline{E}$ . The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device outputs. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor is used on every device between V<sub>CC</sub> and V<sub>SS</sub>. This should be a high frequency type of low inherent inductance and should be placed as close as possible to the device. In addition, a 4.7µF electrolytic capacitor should be used between V<sub>CC</sub> and V<sub>SS</sub> for every eight cavices. This capacitor is to overcome the voltage drop caused by the inductive effects  $\gamma$  PCB traces.

2.5

### Programming

The M27V160 has been designed to be fully compatible with the M27C160. As a result the M27V160 can be programmed as the M27C160 on the same programming equipments applying 12.75V on V<sub>PP</sub> and 6.25V on V<sub>CC</sub> by the use of the same PRESTO III algorithm. When delivered (and after each erasure for UV EPROM), all bits of the M27V160 are in the '1' state. Data is introduced by selectively programming '0's to the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27V160 is in the programming mode when V<sub>pp</sub> input is at 12.5V,  $\overline{G}$  is at V<sub>IH</sub> and  $\overline{E}$  is pulsed to V<sub>IL</sub>. The data to be programmed is applied to 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V<sub>CC</sub> is specified to be 6.25V ± 0.25V.



## 2.6 Presto III programming algorithm

The Presto III Programming Algorithm allows the whole array to be programed with a guaranteed margin in a typical time of 52.5 seconds. Programming with Presto III consists of applying a sequence of 50µs program pulses to each word until a correct Verify occurs (see *Figure 5.*).

During programing and verify operation a Margin Mode circuit is automatically activated to guarantee that each cell is programed with enough margin. No overprogram pulse is applied since the Verify in Margin Mode at  $V_{CC}$  much higher than 3.6V provides the necessary margin to each programmed cell.





## 2.7

2.8

## Program Inhibit

Programming of multiple M27V160s in parallel with different data is also easily accomplished. Except for  $\overline{E}$ , all like inputs including  $\overline{G}$  of the parallel M27V160 may be common. A TTL low level pulse applied to a M27V160's  $\overline{E}$  input and V<sub>PP</sub> at 12.5V, will program that M27V160. A high level  $\overline{E}$  input inhibits the other M27V160s from being programmed.

## Program Verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\overline{E}$  at V<sub>IH</sub> and  $\overline{G}$  at V<sub>IL</sub>, V<sub>PP</sub> at 12.5V and V<sub>CC</sub> at 6.25V.





### 2.9 Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C  $\pm$  5°C ambient temperature range that is required when programming the M27V160. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27V160, with V<sub>PP</sub> = V<sub>CC</sub> = 5V.

Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V<sub>IL</sub> to V<sub>IH</sub>. All other address lines must be held at V<sub>IL</sub> during Electronic Signature mode.

Byte 0 (A0 =  $V_{IL}$ ) represents the manufacturer code and byte 1 (A0 =  $V_{IH}$ ) the device identifier code. For the STMicroelectronics M27V160, these two identifier bytes are given in *Table 3* and can be read-out on outputs Q7 to Q0. Note that the M27V160 and N27C160 have the same identifier bytes.

Identifier	A0	Q15 and Q7	Q14 and Q6	Q13 and Q5	Q12 and Q1	011 Unri Q3	Q10 and Q2	Q9 and Q1	Q8 and Q0	Hex Data
Manufacturer's Code	$V_{IL}$	0	0	í,	0	0	0	0	0	20h
Device Code	$V_{\text{IH}}$	1	υ	Q	1	0	0	0	1	B1h

Table 3. Electronic Signature

## 2.10 Erasure operation (applies to UV EPROM)

The erasure charactalistics of the M27V160 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27V160 in about 3 years, while it would take approximately 1 week to take erasure when exposed to direct sunlight. If the M27V160 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27V160 window to prevent unintentional erasure. The recommended erasure procedure for M27V160 is exposure to short wave ultraviolet light which has a wavelength of 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm<sup>2</sup>. The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000  $\mu$ W/cm<sup>2</sup> power rating. The M27V160 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure.



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#### **Maximum ratings** 3

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Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature <sup>(2)</sup>	-40 to 125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-50 to 125	°C
T <sub>STG</sub>	Storage Temperature	-65 to 150	°C
V <sub>IO</sub> <sup>(3)</sup>	Input or Output Voltage (except A9)	-2 to 7	V
V <sub>CC</sub>	Supply Voltage	-2 to 7	V
V <sub>A9</sub> <sup>(3)</sup>	A9 Voltage	-2 to 13.5	51
V <sub>PP</sub>	Program Supply Voltage	-2 to 14	V

#### Absolute Maximum Ratings (1) Table 4.

Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress refrigs only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality 1.

. sr SU. sr SU Minimum DC voltage on Input or Output is -0.5V with priss b's undershoot to -2.0V for a period less than 20ns. Maximum DC voltage on Output is V<sub>CC</sub> +0.5V with prissible overshoot to V<sub>CC</sub> +2V for a period less than 20ns.



## 4 DC and AC parameters

 $T_A = 0$  to 70°C or -40 to 85°C;  $V_{CC} = 3.3V \pm 10\%$ ;  $V_{PP} = V_{CC}$ 

Symbol	Parameter	Test Condition	Min.	Max.	Unit
ILI	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	μA
I <sub>LO</sub>	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	μΑ
	Supply Current	$\label{eq:E} \begin{split} \overline{E} = V_{IL}, \ \overline{G} = V_{IL}, \ I_{OUT} = 0 m A, \\ f = 8 M Hz, \ V_{CC} \leq 3.6 V \end{split}$		30	mA
Icc	Supply Current	$\label{eq:E} \begin{split} \overline{E} = V_{IL}, \ \overline{G} = V_{IL}, \ I_{OUT} = 0 m A, \\ f = 5 M Hz, \ V_{CC} \leq 3.6 V \end{split}$		20	mA
I <sub>CC1</sub>	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$	2	1	mA
I <sub>CC2</sub>	Supply Current (Standby) CMOS	$\overline{E} > V_{CC} - 0.2V,  V_{CC} \le 3.6V$	00	60	μA
I <sub>PP</sub>	Program Current	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
V <sub>IL</sub>	Input Low Voltage	1ete	-0.3	0.2V <sub>CC</sub>	V
V <sub>IH</sub> <sup>(2)</sup>	Input High Voltage	<u> </u>	0.7V <sub>CC</sub>	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage	i <sub>OL</sub> = 2.1mA		0.4	V
V <sub>OH</sub>	Output High Voltage TTL	I <sub>OH</sub> = -400μA	2.4		V

 Table 5.
 Read Mode DC Characteristics <sup>(1)</sup>

1.  $V_{CC}$  must be applied simultaneously ' with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Maximum DC voltage on Ou our is  $V_{CC}$  +0.5V.

# $T_A = 25 \text{ °C}; V_{CC} = 3.25V \pm 0.25V; V_{PP} = 12.5V \pm 0.25V$

## Table 3 Programming Mode DC Characteristics <sup>(1)</sup>

	Symbol	Parameter	Test Condition	Min	Max	Unit
de		Input Leakage Current	$0 \le V_{IN} \le V_{CC}$		±1	μΑ
S	I <sub>CC</sub>	Supply Current			50	mA
$O_{\mathcal{P}}$	Ipp	Program Current	$\overline{E} = V_{IL}$		50	mA
16	V <sub>IL</sub>	Input Low Voltage		-0.3	0.8	V
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	V <sub>IH</sub>	Input High Voltage		2.4	V <sub>CC</sub> + 0.5	V
O <sub>2</sub>	V <sub>OL</sub>	Output Low Voltage	$I_{OL} = 2.1 \text{mA}$		0.4	V
	V <sub>OH</sub>	Output High Voltage TTL	I <sub>OH</sub> = -2.5mA	3.6		V
	V <sub>ID</sub>	A9 Voltage		11.5	12.5	V

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .



#### Table 7. AC Measurement Conditions

Parameter	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 20ns
Input Pulse Voltages	0 to 3V	0.4V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

 $T_A = 25 \text{ °C}, f = 1 \text{ MHz}$ 

#### Table 8. Capacitance <sup>(1)</sup>

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C <sub>IN</sub>	Input Capacitance (except BYTEV <sub>PP</sub> )	$V_{IN} = 0V$		10	۶F
	Input Capacitance (BYTEV <sub>PP</sub> )	$V_{IN} = 0V$		1:20	pF
C <sub>OUT</sub>	Output Capacitance	$V_{OUT} = 0V$	21	12	pF

1. Sampled only, not 100% tested.

### Figure 6. AC Testing Input Output Waveform







## $T_A$ = 0 to 70°C or –40 to 85°C; $V_{CC}$ = 3.3V $\pm$ 10%; $V_{PP}$ = $V_{CC}$

 Table 9.
 Read Mode AC Characteristics <sup>(1)</sup>

					M27V160						
Symbol	Alt	Parameter	Test Condition	-100 <sup>(2)</sup>		-120		-150		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Valid to Output Valid	$\overline{E} = V_{IL},  \overline{G} = V_{IL}$		100		120		150	ns	
t <sub>BHQV</sub>	t <sub>ST</sub>	BYTE High to Output Valid	$\overline{E} = V_{IL},  \overline{G} = V_{IL}$		100		120		150	ns	
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$		100		120		150	ns	
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$		50		60	Ċ	60	ns	
t <sub>BLQZ</sub> <sup>(3)</sup>	t <sub>STD</sub>	BYTE Low to Output Hi-Z	$\overline{E} = V_{IL},  \overline{G} = V_{IL}$		45		59	2-	50	ns	
t <sub>EHQZ</sub> <sup>(3)</sup>	t <sub>DF</sub>	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	0	45	C	.j0	0	50	ns	
t <sub>GHQZ</sub> <sup>(3)</sup>	t <sub>DF</sub>	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	0	+5	0	50	0	50	ns	
t <sub>AXQX</sub>	t <sub>OH</sub>	Address Transition to Output Transition	$\overline{E} = V_{IL}, \overline{G} = \bigvee_{IL}$	5		5	20	5		ns	
t <sub>BLQX</sub>	t <sub>OH</sub>	BYTE Low to Output Transition	$\overline{E} = V_{IL},  \overline{C} = V_{IL}$	5	.0.	5		5		ns	

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Speed obtained with High Speed measurement conditions.

3. Sampled only, not 100% tested.

## $T_A = 25 \text{ °C}$ : $V_{Cl}$ : = 6.25V ± 0.25V; $V_{PP} = 12.5V \pm 0.25V$

### Table 10. Programming Mode AC Characteristics <sup>(1)</sup>

Symbol	٨."	Parameter	Test Condition	Min.	Max.	Unit
tavel	t <sub>AS</sub>	Address Valid to Chip Enable Low		2		μs
t <sub>uvel</sub>	t <sub>DS</sub>	Input Valid to Chip Enable Low		2		μs
t <sub>VPHAV</sub>	t <sub>VPS</sub>	V <sub>PP</sub> High to Address Valid		2		μs
t <sub>VCHAV</sub>	t <sub>VCS</sub>	V <sub>CC</sub> High to Address Valid		2		μs
<b>t</b> ELEH	t <sub>PW</sub>	Chip Enable Program Pulse Width		45	55	μs
t <sub>EHQX</sub>	t <sub>DH</sub>	Chip Enable High to Input Transition		2		μs
t <sub>QXGL</sub>	t <sub>OES</sub>	Input Transition to Output Enable Low		2		μs
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid			120	ns
t <sub>GHQZ</sub> (2)	t <sub>DFP</sub>	Output Enable High to Output Hi-Z		0	130	ns
t <sub>GHAX</sub>	t <sub>AH</sub>	Output Enable High to Address Transition		0		ns

1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .

2. Sampled only, not 100% tested.





Figure 8. Word-Wide Read Mode AC Waveforms







Note: Chip Enable  $(\overline{E})$  and Output Enable  $(\overline{G}) = V_{IL}$ .



### Figure 11. Programming and Verify Modes AC Whateiorms

57

# 5 Package mechanical data

## 5.1 42-pin Ceramic Frit-seal DIP with window (FDIP42WB)



Figure 12. FDIP42WB package outline

Table 11. FDIP42WE	package mechanical	da/a
--------------------	--------------------	------

	0h.el		millimeters	50	0	inches	
	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.
	А			5.71	0.		0.225
	A1	0.50	G	1.78	0.020		0.070
	A2	3.90		5.08	0.154		0.200
	В	0.40	<b>(</b>	0.55	0.016		0.022
	B1	0.27		1.52	0.050		0.060
	6	0.22	G	0.31	0.009		0.012
	D	Å		54.81			2.158
	D2	1-10	50.80	-	_	2.000	-
	E	20	15.24			0.600	
SO	E1	14.50		14.90	0.571		0.587
$\partial Q^2$	е	2.29		2.79	0.090		0.110
	eA	15.40		15.80	0.606		0.622
	eВ	16.17		18.32	0.637		0.721
SO.	К	9.32		9.47	0.367		0.373
$\gamma$	K1	11.30		11.55	0.445		0.455
U	L	3.18		4.10	0.125		0.161
	S	1.52		2.49	0.060		0.098
	α	4°		15°	4°		15°
	N		42			42	

#### 42-pin Plastic DIP, 600 mils width (PDIP42) 5.2

### Figure 13. PDIP42 package outline



#### Table 12. PDIP42 package mechanical data

Cumb al		millimeters			inches		
Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	
A	_		5.08	-	0	0.200	
A1	0.25			0.010		_	
A2	3.56		4.06	0.140		0.160	
В	0.38		0.53	0.015		0.021	
B1	1.27	S	1.65	0.050		0.065	
С	0.20		0.36	0.008		0.014	
D	52.21		52.71	2.055		2.075	
D2	-00-	50.80	_	_	2.000	_	
		15.24	-	-	0.600	_	
E1	13.59		13.84	0.535		0.545	
e1	797	2.54	_	_	0.100	_	
eA	× 00-	14.99	_	_	0.590	_	
eB	15.24		17.78	0.600		0.700	
CL	3.18		3.43	0.125		0.135	
	0.86		1.37	0.034		0.054	
α	0°		10°	0°		10°	
N		42			42		



#### 42-lead Shrink Plastic DIP, 600 mils width (SDIP42) 5.3

### Figure 14. SDIP42 package outline



#### Table 13. SDIP42 package mechanical data

	Cumhal	millimeters			inches		
	Symbol -	Min.	Тур.	Max.	Min.	Тур.	Max.
	А			5.08		(O)	0.200
	A1	0.51			0.020		
	A2	3.05	3.81	4.57	0.120	0.150	0.180
	b	0.38	0.46	0.56	0.015	0.018	0.022
	b2	0.89	1.)2	1.14	0.035	0.040	0.045
	С	0.23	0.25	0.38	0.009	0.010	0.015
	D	36.2	36.83	37.08	1.440	1.450	1.460
	е	<u> </u>	1.78	-	_	0.070	_
		15.24	(S)	16.00	0.600		0.630
	E1	12.70	13.72	14.48	0.500	0.540	0.570
10	eA	700	15.24			0.600	
cO'	eB	00		18.54			0.730
-105		2.54	3.30	3.56	0.100	0.130	0.140
JUSON	S		0.64			0.025	
	N		42			42	

## 5.4 44-lead Square Plastic Leaded Chip Carrier (PLCC44)

### Figure 15. PLCC44 package outline





### Table 14. PLCC44 package mechanical data

		T EOOTT publicage moonamour dat					
	Symbol		millimeters	100	0	inches	
	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.
	А	4.200		4.570	0.1654		0.1799
	A1	2.290	G	3.040	0.0902		0.1197
	A2	3.650		3.700	0.1437		0.1457
	В	0.351		0.533	0.0130		0.0210
	B1	0.361		0.812	0.0260		0.0320
	<u>رب</u>		G	0.101			0.0040
	с	Å	0.510			0.0201	
	D	17.400		17.650	0.6850		0.6949
	D1	16.510		16.662	0.6500		0.6560
S	D2	14.990		16.000	0.5902		0.6299
00	D3	-	12.700	-	-	0.5000	_
	E	17.400		17.650	0.6850		0.6949
	E1	16.510		16.660	0.6500		0.6559
NSU!	E2	14.990		16.000	0.5902		0.6299
OV C	E3	_	12.700	-	_	0.5000	_
V	е	-	1.270	-	-	0.0500	-
	N		44			44	

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## 5.5 44-lead Plastic Small Outline, 525 mils body width (SO44)



Figure 16. SO44 package outline



Table 15.	SO44	nackage	mechanical data
		package	meenamear uata

Symbol	millimeters			inches		
Symbol	Min.	Тур.	Max	Min.	Тур.	Max.
A		(	2.80	10		0.1102
A1	0.10			0.0039		
A2	2.20	2.30	2.40	0.0866	0.0906	0.0945
b	0.35	0.40	0.50	0.0138	0.0157	0.0197
С	C 1L	0.15	0.20	0.0039	0.0059	0.0079
СР	10		0.08			0.0030
50	28.00	28.20	28.40	1.1024	1.1102	1.1181
E	13.20	13.30	13.50	0.5197	0.5236	0.5315
EH	15.75	16.00	16.25	0.6201	0.6299	0.6398
е	<u> </u>	1.27	-	-	0.0500	-
		0.80			0.0315	
α			8°			8°
N		44			44	

X



## 6 Part Numbering

#### Table 16. Ordering Information Scheme



6 = -40 to 85 °C

- 1. High Speed, see AC Characteristics section for further information.
- 2. Packages option available on request. Please contact STMicroelectronics local Sales Office.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.



# 7 Revision history

#### Table 17. Document revision history

	Date	Revision	Changes
	10-Mar-2000	1	First Issue
	23-Apr-2001	2	PLCC44 package added
	19-Jul-2001	3	SDIP42 package added
	21-Mar-2002	4	SO44 package mechanical and data clarified
	12-Apr-2006	5	Converted to new template. Added ECOPACK® information. Removed "On-board Programming" section. Removed Tape & Reel Packing option.
obsole obsole	ste Pro	duct	obsolete Product(s) obsolete Product(s)



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25/25